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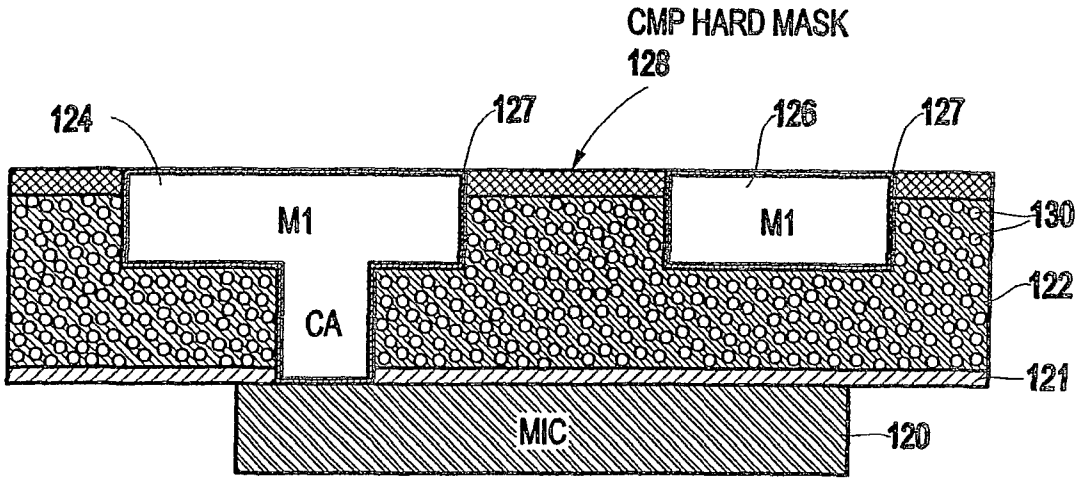
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(54) Title: POST CMP POROGEN BURN OUT PROCESS



(57) Abstract: A method and structure for forming an integrated circuit structure is disclosed that forms at least one first layer (120) comprising logical and functional devices and forms at least one interconnection layer above the first layer. The interconnection layer is adapted to form electrical connections between the logical and functional devices. The interconnection layer is made by first forming a dielectric layer (122). The dielectric layer (122) includes a first material and a second material, wherein the second material is less stable at manufacturing environmental conditions (e.g., the processing conditions discussed below) than the first material. The "second material" comprises a porogen and the "first material" comprises a matrix polymer. The invention then forms conductive features (124, 126) in the dielectric layer (122) and removes (e.g., by heating) the second material from the dielectric layer to create air pockets in the interconnection layer where the second material was positioned.

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