IMPROVED HIGH K-DIELECTRICS USING NICKEL SILICIDE

TECHNICAL FIELD

This application pertains to a transistor with a gate electrode having a high-K gate dielectric with a nickel silicide layer and method of making the same.

BACKGROUND ART

Standard gate semiconductor structures such as transistors and memory units are well known in the semiconductor device industry. Typically, to form a standard gate electrode, first a gate dielectric layer comprising silicon dioxide is formed on an active surface of a semiconductor substrate between isolation regions and then a polysilicon layer is formed on the dielectric layer. The layers of materials are then etched in a controlled manner to define the borders of the gate electrode. Source and drain regions are formed by doping the active surface of the substrate by ion doping by well know techniques. Dielectric sidewall spacers are formed on the side surfaces of the gate electrode to complete the device.

As both the vertical and lateral device dimensions decrease into the deep sub-micron range such as that associated with the formation of ultra-large scale integration (ULSI) devices, problems arise such as junction leakage and increased sheet resistance of the contact areas to the source and drain regions. To overcome these problems, the use of self-aligned, highly electrically conductive refractory metal silicides, i.e., "salicides" (derived from Self-ALIgned-siliCIDE), has become commonplace in the manufacture of IC semiconductor devices comprising, e.g., MOS type transistors. Salicide processing involves deposition of a metal that forms an intermetallic compound with silicon (Si). The metal does not react with silicon oxides, nitrides, or oxynitrides under normal processing conditions. Refractory metals commonly employed in salicide processing include platinum (Pt), titanium (Ti), nickel (Ni), and cobalt (Co), each of which forms very low resistively phases with Si, e.g., $PtSi_2$, $TiSi_2$, NiSi, and $CoSi_2$. In practice, the refractory metal is deposited in a uniform thickness over all exposed surface features of a Si wafer, preferably by means of physical vapor deposition ("PVD") process, e.g., sputtering from an ultra-pure target utilizing an ultra-high vacuum, multi-chamber DC magnetron sputtering system. Upon thermal processing, e.g., a rapid thermal annealing ("RTA") performed in an inert atmosphere, the refractory metal layer reacts with underlying Si to form an electrically conductive refractory metal silicide layer on the top surface of the polysilicon gate electrode as well as on the exposed surfaces of the substrate where source and drain regions are formed. Unreacted portions of the refractory metal layer, e.g., on the dielectric sidewall spacers and the silicon oxide isolation regions, are removed, as by a wet chemical etching process.

Also associated with the fabrication of ULSI devices, the thickness of the silicon dioxide dielectric for the gate electrode is rapidly approaching a thickness of 40 Å or less. At this thickness, the use of silicon dioxide as a gate dielectric is limited because direct tunneling may occur through the gate dielectric to the channel region, wherein current leaks from the gate electrode and the channel region. Such leakage of current causes an increase in power consumption. Because of this problem, alternative methods have been sought to reduce leakage current.

One such method is to use high-K dielectrics for gate dielectric materials. A high-K dielectric is any dielectric material having a dielectric constant greater than silicon dioxide that is 3.8. The dielectric constant of the high-K dielectric is preferably greater than 5.0, and more preferably, greater than 20.0. However, the use of

high-K dielectrics for gate dielectric materials is disadvantageous because the high processing temperatures required for forming the salicide layer causes the dielectric to decompose due to the reaction of the dielectric with silicon in the semiconductor substrate and the polysilicon in the gate.

It has been discovered that by forming nickel silicide, the aforementioned problems are overcome. Lower temperatures are required to form nickel silicide, than for the other refractory metals. Also, Ni as opposed to other refractory metals such as Ti diffuses into Si, which helps to limit bridging between the metal silicide layer on the gate electrode and a metal silicide layer on the associated source/drain regions. Further, the formation of nickel silicide requires less Si than other refractory metals, such as Ti or Co. Nickel silicide also exhibits almost no line width dependence on sheet resistance. Advantageously, nickel silicide is normally annealed in a one step process, rather than the more complex process required in $TiSi_2$ and $CoSi_2$ salicide technology. Finally, nickel silicide exhibits lower film stress, i.e., causes less wafer distortion than conventional Ti or Co silicides.

DISCLOSURE OF THE INVENTION

An object of this invention is to provide for the formation of a self-aligned metal silicide on the gate, source and drain electrodes without deterioration of the high-K dielectric of the gate electrode. Another object is to provide for a nickel-silicide on a gate electrode including a high-K dielectric. A further object is to provide for a nickel silicide layer on the gate electrode being included a high-K dielectric material. Other objects, features and advantages of this invention will become apparent upon reading the following detailed description and referring to the accompanying drawing.

BRIEF DESCRIPTION OF THE DRAWINGS

The various novel features of this invention, along with the foregoing and other objects as well as the invention itself both as to its organization and method of operation, may be more fully understood from the following description of the illustrated embodiments when read in conjunction with the accompanying drawings, wherein;

Fig. 1 depicts a partial cross-sectional view of a semiconductor topography wherein a high-K dielectric layer is formed between two shallow trench isolation regions.

Fig. 2 depicts a partial cross-sectional view of a semiconductor topography wherein the gate electrode is formed between two shallow trench isolation regions.

Fig. 3 depicts a partial cross-sectional view of a semiconductor topography wherein the semiconductor is treated with ions to form extension regions.

Fig. 4 depicts a partial cross-sectional view of a semiconductor topography wherein spacers are formed on the sidewalls of the gate electrode.

Fig. 5 depicts a partial cross-sectional view of a semiconductor topography wherein the semiconductor is treated with ions to form the deep preamorphous ion implantation.

Fig. 6 depicts a partial cross-sectional view of a semiconductor topography wherein a nickel layer is form over the semiconductor.

Fig. 7 depicts a partial cross-sectional view of a semiconductor topography wherein nickel silicide is formed.

Fig. 8 depicts a partial cross-sectional view of a semiconductor topography wherein regions not forming nickel silicide are removed.

MODES FOR CARRYING OUT THE INVENTION

This invention relates to a method of making a semiconductor having a gate electrode which includes a high-K dielectric and a method of forming the semiconductor without decomposition or deterioration of the high-K dielectric. The high-dielectric layer is used to replace the conventional silicon dioxide gate dielectric to reduce gate tunneling leakage. The method is illustrated in Figs. 1-8.

The first step of the inventive method is shown in Fig. 1. A silicon based substrate 11 is provided. The substrate may be silicon wafer or silicon wafer bonded to insulator substrate, or epitaxally grown silicon. Preferably, the substrate is monocrystalline silicon wafer having one conductivity type (P or N). The substrate includes a plurality of separate well regions 13, each region comprising a field oxide (FOX) isolation region, a region formed by local oxidation of silicon (LOCOS), or a shallow trench isolation (STI) region. The STI is formed by the conventional method which is etching a shallow trench in the substrate, thermally oxidizing the trench, filling the oxidized trench with silicon dioxide deposited by chemical vapor deposition (CVD) and then chemically or mechanically polishing the surface. The STI is formed to a preferred depth of between 0.10 and 1.0 μm.

A high-K dielectric layer 12 is formed between two shallow trench isolation regions 13. A high-K dielectric layer is defined as a dielectric having a dielectric constant greater than that of silicon dioxide (dielectric constant of 4.2). In the present invention, the high-K dielectric is a material selected from the group consisting of silicon nitride having a dielectric constant between 6.0 and 8.0 (preferably 7.5), silicon oxynitride having a dielectric constant between 3.9 and 7.5, barium strontium titanate having a dielectric constant from about 20 to 200, tantalum pentoxide (Ta_2O_5) having a dielectric constant between 20 and 200, halfnium oxide (20 and 40), halfnium silicate having a dielectric constant between 10 and 20, zirconium oxide (20 and 40) zirconium silicate having a dielectric constant between 20 and 40, aluminum oxide, and lead zinc niobate. The preferred high-K dielectrics are halfnium and zirconium oxides and their silicates. The thickness of the high-K layer 12 is selected layer ranges from about 20Å to about 200 Å, preferably from about 30 Å to about 100 Å thick.

While the high-K dielectric layers are thicker than the comparable SiO_2 dielectric layers, it will be appreciated that, for example, a 16Å thick layer of tantalum oxide having a dielectric constant of 25 is equivalent to 4.0Å of SiO_2 having a dielectric constant of 4.2 and a 80Å layer of silicon nitride having a dielectric constant of 8.0 is equivalent to a 40Å of SiO_2. The high-K dielectric is patterned by forming a photoresist mask pattern (not shown) over the high-K dielectric layer and then etching the dielectric layer, for example with CHF_3 and argon or by conventional anisotropic plasma etching or wet etching techniques to form high-K dielectric layer 12.

In the second step of the invention is the formation of the polysilicon gate electrode as illustrated in Fig. 2. A blanket layer of polysilicon (not shown) is deposited on the high dielectric layer using CVD method. A layer of photoresist (not shown) is formed on the polysilicon layer. The photoresist is patterned and polysilicon layer 14 is selectively etched to form the gate electrode. The remaining photoresist (not shown) is removed and

the structure as shown in Fig. 2 is the result. The thickness of the polysilicon layer is between about 500 Å and about 3000 Å, and preferably between about 800 Å and about 1300 Å.

The third step of the inventive method is shown in Fig. 3. This step involves forming the source and drain extension regions. The regions are first impregnated by a preamorphous ion implantation process to form an α-silicon layer. This layer is further bombarded with ions (shown in Fig. 3 by the arrows) by an extension ion implantation process to form source and drain extension regions 16 and 17, respectively. The upper surface 15 of the polysilicon gate electrode 14 is also doped by ion implantation. Arsenic or phosphorous containing ions or n-type dopant are employed if it is desired to form an NMOS device or boron containing ions are employed if it is desired to form a PMOS device. By way of illustration only, n-type source and drain extension regions having a shallow-depth of from about 100 to about 500 Å and a doping of from about 1 x 10^{18} to about 1 x 10^{20} da/cm^3 may be formed in crystalline Si by implanting arsenic containing ions at a dosage of from about 1 x 10^{14} to about 1 x 10^{15} da/cm^2 and energies of from about 1 to about 10 (KeV).

The fourth step of the inventive method is shown is to form silicon nitride spacers 18 on each side of the polysilicon gate electrode/high-K dielectric 15 and 12. Referring to Fig. 4, sidewall spacers 18 comprised of silicon nitride are formed on the surfaces of sidewalls of the gate electrode/gate dielectric layer stack 15/12. Typically, the sidewall spacers are formed by a conventional process comprising the steps of depositing a blanket layer of silicon nitride covering all exposed surface portions of the substrate 11 as well as all exposed surfaces of the various features formed therein or thereon, including, *inter alia*, the opposing sidewall surfaces and top surface 15 of polysilicon layer 14 and then subjected to an anisotropic etching process, e.g., plasma etching in a fluorine-containing plasma, for selectively removing the laterally extending portions thereof and forming the sidewall spacers 18. The thickness of the silicon nitride is selected so as to provide tapered sidewall spacers 18 having a desired width profile.

In the fifth step of the inventive method, the formation of the source and drain regions, which was started by forming extensions 16 and 17, respectively, is completed as shown in Fig. 5 by implanting additional dopant into the source and drain regions 19 and 20. Following the formation of the sidewall spacers 18, a pair of deeper, more heavily-doped source and drain regions 19 and 20 are formed, as by a "main implant" ion implantation process utilizing the sidewall spacers 18 as implantation masks, generally within the portions of substrate 11 where the shallow-depth, lightly-doped source and drain extension regions 16 and 17 were previously formed. As shown in Fig. 5, the more heavily-doped source and drain regions 19 and 20 formed by the "main implant" process extend beyond the depth of source and drain extension regions 16 and 17, except at the portions of the latter regions underlying the sidewall spacers 18. By way of illustration only, according to conventional practice, typical arsenic implantation conditions for forming source and drain regions 19 and 20 of a Si wafer-based NMOS transistor having a peak arsenic n-type dopant concentration of from about 1 X 10^{18} to about 1 x 10^{20} da/cm^3 at a depth of from about 800 to about 1200 Å below the surface of the Si wafer include dosages of from about 5 x 10^{14} to about 5 x 10^{15} da/cm^2 and energies of from about 20 to about 50 (KeV).

With reference to Fig. 6, in the next step, a blanket layer 21 of Ni by a PVD process such as DC sputtering, to cover all exposed surfaces of the thus-formed structure. The conversion of Ni to NiSi may be accomplished by means of a one-step thermal process, typically RTA performed at temperatures of from about 350° to about 750°C, for example, in a nitrogen-containing inert atmosphere at 550°C for about 40 sec. to yield the structure shown in Fig. 8. Nickel silicides 22 and 24 are formed over the source and drain regions,

respectively, and a silicide layer 23 forms on the surface of the polysilicon gate. The thickness of nickel silicides 22 and 24 is from about 200 Å to about 500 Å while the thickness of silicide layer 23 is from about 200 Å to about 500 Å. The unreacted portions of the Ni layer 21 formed over the sidewall spacers 18 and STI regions 13 are selectively removed, for example, by etching with a 2:1 H_2SO_4/H_2O_2 mixture at a temperature of about 100° C. The structure in Fig. 8 can then undergo further processing for contact formation to the source/ drain regions and the gate electrode.

The foregoing is considered as illustrative only of the principles of the invention. Further, since numerous modifications and changes will readily occur to those skilled in the art, it is not desired to limit the invention to the exact construction and operation shown and described, and accordingly, all suitable modifications and equivalence thereof may be resorted to, falling within the scope of the invention claimed.

CLAIMS

WHAT IS CLAIMED IS:

1. A process for forming a semiconductor structure comprising the steps of:

forming a substrate (11) having an active surface between two isolation regions (13);

forming on said surface a gate electrode (14) having sidewalls and comprising a layer of high-K dielectric (12) on said surface and a polysilcon layer (14) on said high-K dielectric (12);

forming spacers (18) on said sidewalls of said gate electrode (14);

depositing a layer of nickel (21) on the polysilcon (14), the sidewalls of the gate electrode (14) and on the surface of the precursor over the active regions (19, 20);

forming nickel silicide (22, 24) by reacting nickel (21) with silicon; and

removing unreacted nickel (21).

2. The process of claim 1 wherein the high-K dielectric (12) is halfnium oxide, halfnium silicate, zirconium oxide and zirconium silicate.

3. The process of claim 1 wherein the spacers (18) comprise silicon nitride.

4. A semiconductor comprising a gate electrode (14) on a surface of a semiconductor substrate between two active regions (19, 20), the gate electrode (14) having sidewalls and comprising a layer of high-K dielectric (12) on the surface of the semiconductor substrate and a polysilcon layer (14) on said high-K dielectric (12), spacers (18) on the sidewalls of said gate electrode (14), and a nickel silicide layer (22, 24) on said active regions (19, 20) and on said polysilicon layer (14).

5. The semiconductor of claim 4 wherein the high-K dielectric (12) is Ta_2O_5.

6. The semiconductor of claim 4 wherein the spacers (18) comprise silicon nitride.