METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE HAVING DIFFERENT METAL SILICIDE PORTIONS

TECHNICAL FIELD

Generally, the present invention relates to the field of fabrication of integrated circuits, and, more particularly, to semiconductor devices having metal-silicide portions on semiconductor regions to reduce the sheet resistance of the semiconductor regions. Furthermore, the present invention relates to a method of manufacturing these semiconductor devices.

BACKGROUND ART

In modern ultra-high density integrated circuits, device features are steadily decreasing to enhance device performance and functionality. Shrinking the feature sizes, however, entails certain problems that may partially offset the advantages obtained by the reduced feature sizes. Generally, reducing the feature sizes of, for example, a transistor element, leads to a decreased channel resistance in the transistor element and thus results in a higher drive current capability and enhanced switching speed of the transistor. In decreasing the features sizes of these transistor elements, however, the increasing electrical resistance of conductive lines and contact regions, *i.e.*, of regions that provide electrical contact to the periphery of the transistor element, becomes a dominant issue since the cross-sectional area of these lines and regions decreases with decreasing feature sizes. The cross-sectional area, however, determines, in combination with the characteristics of the material comprising the conductive lines and contact regions, the resistance of the respective line or contact region.

The above problems may be exemplified for a typical critical feature size in this respect, also referred to as a critical dimension (CD), such as the extension of the channel of a field effect transistor that forms below a gate electrode between a source region and a drain region of the transistor. Reducing this extension of the channel, commonly referred to as channel length, may significantly improve device performance with respect to fall and rise times of the transistor element due to the smaller capacitance between the gate electrode and the channel and due to the decreased resistance of the shorter channel. Shrinking of the channel length, however, also entails the reduction in size of any conductive lines, such as the gate electrode of the field effect transistor, which is commonly formed of polysilicon, and the contact regions that allow electrical contact to the drain and source regions of the transistor, so that consequently the available cross-section for charge carrier transportation is reduced. As a result, the conductive lines and contact regions exhibit a higher resistance unless the reduced cross-section is compensated by improving the electrical characteristics of the material forming the lines and contact regions, such as the gate electrode, and the drain and source contact regions.

It is thus of particular importance to improve the characteristics of conductive regions that are substantially comprised of semiconductor material such as silicon. For instance, in modern integrated circuits, the individual semiconductor devices, such as field effect transistors, capacitors and the like, are primarily based on silicon, wherein the individual devices are connected by silicon lines and metal lines. While the resistivity of the metal lines may be improved by replacing the commonly used aluminium by, for example, copper, process engineers are confronted with a challenging task when an improvement in the electrical characteristics of silicon-containing semiconductor lines and semiconductor contact regions is required.

With reference to Figures 1a and 1b, an exemplary process for manufacturing an integrated circuit containing, for example, a plurality of MOS transistors, will now be described in order to illustrate the problems involved in improving the electrical characteristics of silicon-containing semiconductor regions in more detail.

In Figure 1a, a semiconductor structure 100 includes a substrate 101, for example, a silicon substrate, in which a first semiconductor element 110 and a second semiconductor element 130 are formed. The first semiconductor element 110 may, as depicted in Figure 1a, represent a field effect transistor of a first conductivity type, such as an n-channel transistor, and the second semiconductor element 130 may represent a field effect transistor of a second conductivity type, such as a p-channel transistor. The first semiconductor element 110 comprises shallow trench isolations (STI) 113 that are formed of an insulated material, such as silicon dioxide, and that define an active region 112 in the substrate 101. A gate electrode 115 is formed over a gate insulation layer 118 that separates the gate electrode 115 from the active region 112. Spacer elements 116 made of, for example, silicon dioxide or silicon nitride, are located at the sidewalls of the gate electrode 115. In the active region 112, source and drain regions 114 are formed and exhibit an appropriate dopant profile required to connect to a conductive channel that builds up between the drain and the source region during operation of the first semiconductor element 110.

The second semiconductor element 130 comprises substantially the same parts as the first semiconductor element 110 and corresponding parts are denoted by the same reference numerals except for a "leading 13" instead of a "leading 11." As previously noted, the second semiconductor element 130 may differ from the first semiconductor element 110 in, for example, type of conductivity, that is, type and concentration of dopants provided in the active regions 112 and 132, lateral extension of the gate electrode, also referred to as gate length, cross-sectional area, and the like. Moreover, it should be noted that although the first and second semiconductor elements 110 and 130 in Figs. 1a and 1b are depicted as transistor elements, the first and second semiconductor elements 110 and 130 may represent any silicon-containing region that is used for charge carrier transportation. For example, relatively long polysilicon lines may connect semiconductor elements on different locations of a single chip area and these polysilicon lines may be regarded as first and second semiconductor elements 110, 130, the electrical characteristics of which are to be improved so as to obtain an enhanced device performance with respect to signal propagation delay.

Again referring to Figure 1a, in particular the gate length of the first and second semiconductor elements 110 and 130 determines the channel length of these devices and, therefore, as previously pointed out, significantly affects the electrical characteristics of the first and second semiconductor elements 110 and 130, whereby a reduced gate length will result in an increased resistance of the gate electrodes 115, 135 owing to the reduction of the cross-sectional area of the gate electrodes 115, 135.

A typical process flow for forming the semiconductor structure 100 may comprise the following steps. After formation of the shallow trench isolations 113 and 133 by well-known photolithography techniques, implantation steps are performed to create a required dopant concentration in the active regions 112 and 132. Subsequently, the gate insulation layers 118 and 138 are formed according to design requirements. Thereafter, the gate electrodes 115 and 135 are formed by patterning, for instance a polysilicon layer, by means of sophisticated photolithography and trim etch methods. Then, a further implantation step for forming so-called source and drain extensions within the source and drain regions 114 and 134 is performed and the spacer elements 116 and 126 are formed by deposition and anisotropic etching techniques. The spacer elements 116 and 126 are used as an implantation mask for a subsequent implantation step in which dopant particles are implanted into the source and drain regions 114 and 134 to create the required high dopant concentrations in those regions. It is to be noted that the dopant concentration varies in Figure 1a in the horizontal direction, *i.e.*, in the length direction of the gate electrodes 115, 135, as well as in the vertical direction, which will hereinafter be referred to

as depth direction. Although the dopant profile of the source and drain regions 114 and 134 is depicted as a region having a sharp boundary, in reality the dopant profile varies continuously due to the nature of the implantation process and the subsequent annealing steps that are performed for activating the implanted atoms and for curing the crystalline damage caused by the implantation step. Usually, the dopant profile has to be selected in conformity with other parameters of the first and second semiconductor elements 110 and 130. For example, a short gate length, and thus a short channel length, requires a "shallow" dopant profile in order to avoid the so-called "short channel effect." Accordingly, the peak concentration in the depth direction may be located a few hundred nanometers below the surface of the drain and source regions 114 and 134. Moreover, p-channel transistors may require a different dopant profile than an n-channel transistor element.

As previously noted, the cross-section of the gate electrodes 115 and 135, which may be considered as polysilicon lines, as well as the contact area on top of the source and drain regions 114 and 134, significantly influence the electrical characteristics of the first and second semiconductor elements 110 and 130. Since, generally, these device areas primarily contain a semiconductor material such as silicon in crystalline, polycrystalline and amorphous form, these areas, although they usually include dopants, exhibit a relatively high resistance compared to, for example, a metal line. Consequently, these areas are treated to enhance the conductivity of these regions, thereby improving the overall performance of the devices.

To this end, according to Figure 1a, a metal layer 140 is deposited over the first and second semiconductor elements 110 and 130. Typically, the metal layer 140 comprises titanium, cobalt or other refractory metals. Subsequently, a first heat treatment, for example, a rapid thermal annealing, is carried out to initiate a chemical reaction between the silicon in the source and drain regions 114, 134, the gate electrodes 115, 135 and the metal contained in the metal layer 140. If, for example, the metal layer 140 substantially comprises cobalt, an average temperature of the first heat treatment may be set to about 400°C to create a meta-stable cobalt silicon compound exhibiting a relatively high resistivity. Since the silicon contained in the spacer elements 116, 136 and the shallow trench isolations 113, 133 is chemically bound in the form of dioxide or nitride, the metal of the metal layer 140 does not substantially react with the material of the spacer element 115, 136 and the shallow trench isolations 113, 133. After the first heat treatment, the material of the metal layer 140 that has not reacted with the underlying material is removed by, for example, a selective wet etching process. Thereafter, a second heat treatment is performed, for example, a second rapid annealing step with a temperature higher than in the first annealing step, to convert the meta-stable metal-silicon compound into a metal silicide. In the above example, when cobalt is used, a cobalt disilicide is formed in the second annealing step. The metal silicide shows a significantly lower resistance than the meta-stable metal-silicon compound as well as a significantly lower resistance, by a factor of about 5-10, than the sheet resistance of the doped polysilicon.

Figure 1b schematically shows the finally obtained first and second semiconductor elements 110 and 130 having formed on the respective source and drain regions 114, 134 and the gate electrodes 115, 135 a metal silicide region 141.

Although the metal silicide regions 141 significantly improve the electrical characteristics of the first and second semiconductor elements 110 and 130, there is still room for improvement since, in the conventional process flow, the metal silicide regions 141 have to be formed so as to meet the requirements of the first semiconductor element 110 and the second semiconductor element 130, so that optimizing the characteristics of the silicide regions 141 of the first semiconductor element 110 compromises the effect of the silicide regions 141 of the second semiconductor element 130, and vice verse.

It is thus desirable to have a semiconductor and a method of forming the same in which the characteristics of the conductive semiconductor regions may be individually optimized for different semiconductor elements.

The present invention is directed to a method that may solve, or at least reduce, some or all of the afore-mentioned problems.

DISCLOSURE OF INVENTION

The present invention is generally related to a method of manufacturing a semiconductor device in which silicon-containing regions receive a metal silicide portion to enhance the electrical properties of these regions, wherein the type of material and/or a thickness of the metal silicide portion is individually adjusted to meet the requirements of different semiconductor regions in view of the electrical resistance.

According to one illustrative embodiment of the present invention, a method of forming a semiconductor device comprises providing a substrate having formed thereon a first and a second conductive silicon-containing region and forming a first resist mask for covering a second conductive silicon-containing region while exposing the first conductive silicon-containing region. Moreover, a first metal layer of a predefined thickness is deposited over the substrate and the first resist mask is removed. Furthermore, the method includes forming a second resist mask for covering the first conductive silicon-containing region and exposing the second conductive silicon-containing region. Thereafter, a second metal layer of a second predefined thickness is deposited over the substrate and then the second resist mask is removed. Additionally, the method includes a heat treatment of the substrate to form a first silicide layer on the first conductive silicon-containing region and a second silicide layer on the second conductive silicon-containing region.

According to a further embodiment, a method of forming a semiconductor device comprises forming a plurality of conductive silicon-containing regions on a substrate. Thereafter, a plurality of different metal layers are sequentially deposited on the substrate using a deposition mask such that each of the plurality of conductive silicon-containing regions is covered by substantially a single metal layer, wherein the metal layers differ from each other by their type of material and/or their layer thickness. The method further comprises annealing the substrate at a first average temperature for a first time interval to form a metal silicon compound on each of the conductive silicon-containing regions and selectively removing excess metal from the substrate. Additionally, the method includes annealing the substrate at a second average temperature for a second time interval to convert the metal silicon compound into a metal silicide portion, wherein at least one of the first and second average temperatures and the first and second time intervals are controlled to adjust a thickness of the metal silicide portions.

According to a further illustrative embodiment, a semiconductor device comprises at least one first conducive silicon-containing region and at least one second conductive silicon-containing region, wherein the first and second conductive silicon-containing regions are formed in a common layer. Moreover, the semiconductor device comprises a first metal silicide portion formed on the first conductive silicon-containing region and a second metal silicide portion formed in the second conductive silicon-containing region, wherein at least one of the first and second metal silicide portions contains a noble metal.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

Figures 1a and 1b show schematic cross-sectional views of a first and second semiconductor element having a silicide portion formed in conductive areas, wherein the first and second semiconductor elements are manufactured in accordance with a typical prior art process; and

Figures 2a-2f schematically show cross-sectional views of a semiconductor structure during various manufacturing stages, which is formed in accordance with one illustrative embodiment of the present invention.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

MODE(S) FOR CARRYING OUT THE INVENTION

Illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

With reference to Figures 2a-2f, illustrative embodiments of the present invention will now be described, wherein, as previously pointed out, two or more different conductive silicon-containing regions receive a silicide portion, the type of material and/or the thickness of which are correspondingly designed to improve the electrical conductivity of these regions. For example, if it is necessary to obtain a similar signal propagation delay for long silicon lines connecting two different die areas, wherein one of the silicon lines exhibits a larger cross-sectional area than the other one, according to the present invention, different silicide portions are formed on these silicon lines to improve the overall characteristics and to substantially compensate for the different cross-sectional areas. The same applies to different types of transistor elements, such as n-channel transistors and p-channel transistors, that, in general, have a different dopant profile and also a different barrier height that experiences a charge carrier at the interface between the silicided portion and the doped silicon-containing region. In this case, the present invention also allows one to appropriately form corresponding silicide portions in the devices to individually optimize the performance of the devices. Similarly, short channel devices generally require a different type of silicide portion than do long channel devices since, for example, in long channel devices the peak dopant concentration is located more deeply in the drain and source regions than in short channel devices which require relatively shallow junctions. The present invention allows one to individually adjust the overlap of the silicided portion at a depth at which the peak dopant concentration is approximately located so as to obtain a minimum transition resistance for charge carriers, especially when the barrier height of the metal silicide is also selected in conformity with the type of dopants prevailing in the active regions of the transistor devices. Consequently, although in the following detailed description a first and second semiconductor element representing a complimentary transistor pair is referred to, the present invention is to cover all aspects in which silicon-containing regions are required to receive individually adapted silicide portions to improve the performance of the individual semiconductor region or to improve the overall performance of the semiconductor device.

In Figure 2a, a semiconductor structure 200 comprises a substrate 201, for example, a silicon substrate or any other substrate appropriate for the formation of semiconductor elements. In the substrate 201, a first semiconductor element 210 comprises an active region 212 defined by shallow trench isolations 213. A gate electrode 215 is separated from the active region 212 by a gate insulation layer 218. Spacer elements 216 of an insulating material, such as silicon dioxide or silicon nitride, are formed adjacent to the sidewalls of the gate electrode 215. In the active region 212, source and drain regions 214 are formed.

The semiconductor structure 200 further includes a second semiconductor element 230 comprising substantially the same components as the first semiconductor element 210. Thus, corresponding parts are denoted by the same reference numerals except for a leading "23" in stead of a leading "21." It should be borne in mind that, although depicted as being quite similar, the first and the second semiconductor elements 210 and 230 differ from each other in the sense as pointed out above. Moreover, on the second semiconductor element 230, a resist mask 250 is formed.

A typical process flow for forming the semiconductor structure 200 may be quite similar to the processing as described with reference to Figures 1a and 1b and, thus, the description of these process steps is omitted. The resist mask 250 may be formed by means of conventional photolithography wherein, however, any overlay considerations are of no great concern since the precise location of the resist mask 250 on the shallow trench isolations 233 is not critical.

Figure 2b schematically shows the semiconductor structure 200 with a first metal layer 240 deposited over the semiconductor structure 200. The first metal layer 240 may comprise any refractory metal or compound of metals that is suitable to provide for the required characteristics of the metal silicide to be formed in the silicon-containing regions 214 and 215. Suitable metals may include cobalt, titanium, nickel, tungsten and combinations thereof. In one particular embodiment, the first metal layer 240 may comprise a noble metal such as platinum, palladium, gold and the like. A thickness of the first metal layer 240 and the composition thereof is selected such that in a subsequent annealing step an interdiffusing of silicon and metal atoms takes place and a metal silicide portion may form having a required penetration depth, *i.e.*, a required thickness, and a required barrier height to yield a minimum transition resistance for the charge carriers. For example, a cobalt layer may be deposited with a thickness of 30 to 80 nm. In Figure 2b, the first metal layer 240 covers a surface of the resist mask 250, whereas sidewall portions 252 of the resist mask 250 remain substantially uncovered. To this end, a deposition technique may be employed that allows one to minimize the coverage of the sidewall portions 252 with metal. For instance, a physical vapor deposition (PVD) technique, such as sputter deposition, may be used wherein process parameters are adjusted so that atoms and ions sputtered off of a target hit the semiconductor structure 200 in a substantially perpendicular direction. Consequently, the deposition of the first metal layer 240 at the sidewall portions 252 is minimized. Hitting the semiconductor structure 200 substantially perpendicularly may be obtained by using a collimator in the sputter deposition chamber in the vicinity of the substrate 201 to "guide" the ions and atoms approaching the substrate 201. The required directionality of the incoming ions and atoms may also be obtained by adjusting the magnetic and electrical fields within the sputter deposition chamber to obtain a minimal step coverage.

Figure 2c schematically shows the semiconductor structure 200 with the resist mask 250 and the overlaying first metal layer 240 removed. Removing the resist mask 250 and, thus, portions of the first metal layer 240 over the second semiconductor element 230 may be achieved by a selective wet etching process using a chemical agent having a significantly higher etch rate for the resist mask 250 than for the first metal layer 240.

Depending on the degree of coverage of the sidewall portions 252 with metal of the first metal layer 240, the predefined thickness of the initially deposited first metal layer 240 may accordingly be selected so that in the subsequent etching process the thickness of the first metal layer 240 over the first semiconductor element 210 does not remain under a required minimum thickness. If, for example, removing the resist mask 250 takes about 60 seconds and an etch rate of the first metal layer 240 is approximately 10 nm per minute, the initial layer thickness is selected to about 10 nm thicker than at least that required for forming a metal silicide meeting the design requirements. By "underetching" the resist mask 250 from the sidewall portions 252, the mechanical integrity of the first metal layer 240 on top of the resist mask 250 is attacked and the individual parts that split off the first metal layer 240 will be purged away during the process of etching the resist mask 250. Even if the sidewall portions 252 are slightly covered by metal, the resist mask 250 can be removed, although at a prolonged etching time because the metal layer thickness at the sidewall portions is considerably smaller than the thickness of the first metal layer 240 at substantially horizontal surface portions of the substrate 201. Typically, the metal layer thickness at the sidewall portions 252 will not exceed about 10% of the horizontal surface portions. Thus, the first semiconductor element 210 receives a first metal layer 240 that is configured to provide for the required characteristics of a silicide portion to be formed.

In Figure 2d, a second photoresist mask 255 is formed over the first semiconductor element 210 and a second metal layer 242 is blanket-deposited over the semiconductor structure 200. Regarding the formation of the second photoresist mask 255, the same criteria apply here as pointed out with reference to the photoresist mask 250. The same is true for the deposition method for forming the second metal layer 242. Also, in this case, sidewall portions 257 of the second photoresist mask 255 are substantially uncovered or at least significantly less covered by metal than the surface portions of the semiconductor substrate 200. Regarding the composition and the thickness of the second metal layer 242, the same criteria as given above apply in this case.

In one embodiment, a plurality of different semiconductor elements may be provided, wherein in subsequent masking steps in each of the plurality of semiconductor elements a different metal layer is deposited. For example, additionally to the resist masks 250 and 255, a further resist mask (not shown) may be provided, wherein the resist masks 250, 255 and the further resist mask are designed such that a third metal layer may be deposited on a third semiconductor element (not shown). This masking sequence may be repeated with suitably designed masks so that a plurality of different metal layers may be deposited on a corresponding plurality of different types of semiconductor elements that are individually optimized to provide for the required silicide portions in these semiconductor elements.

Figure 2e schematically shows the first and second semiconductor elements 210 and 230 having the first metal layer 240 and the second metal layer 242, respectively. The first and second metal layers 240 and 242 comprise a material and exhibit a thickness, both of which are targeted, when transformed into a metal silicide, to optimize the characteristics of the first and second semiconductor elements 210, 230. In particular, the first metal layer 240 and/or the second metal layer 242 may comprise at least one noble metal.

Subsequently, a heat treatment is performed, for example, a rapid thermal annealing step, to initiate the chemical reaction between the metal in the first and second metal layers 240, 242 and the silicon contained in the regions 214, 234 and 215, 235. In one embodiment, after a first rapid thermal annealing step with a first temperature for a first time interval, diffusion of the atoms of the regions 214, 234, 215, 235 and of the atoms of the first and second metal layers 240, 242 takes place so that a continuous reaction between the silicon and the metal is maintained. The degree of diffusion, and thus of metal-silicon compound, depends on the type of

material, the temperature and the duration of the annealing process. Generally, metals having a higher melting temperature tend to show a lower diffusion activity. Thus, the thickness of the metal-silicon compound may be partially adjusted by controlling the first average temperature and the first time interval. Subsequently, excess metal from the surface of the semiconductor structure 200 is removed and a second rapid thermal annealing step may be performed with a second temperature for a second time interval. Typically, the second average temperature is higher than the first temperature to obtain a stable metal silicide having a relatively low electrical resistance. The second average temperature and the second time interval may be controlled to obtain the required sheet resistance in each of the regions 214, 215, 234, 235. It is to be noted that although the first and second metal layers 240, 242 differ from each other, the sheet resistance in the first and second semiconductor elements 210 and 230 may nevertheless be individually adjusted in a common heat treatment since the reaction characteristics of the materials comprising the first and second metal layers 240, 242 are well known and may be selected to yield the desired sheet resistance. Between the first and the second rapid thermal annealing step, the excess metal of the first and second metal layers 240, 242 may be removed by a selective etch process, wherein advantageously metal and metal compounds do not need to be selectively removable with respect to each other. Thus, the non-reacted metal of the first and the second metal layer 240, 242 may be removed in a common etching process. Moreover, no additional heat treatment, compared to the previously described conventional processing, is required and, thus, a "thermal budget" is not incurred.

Figure 2f schematically shows the finally-obtained semiconductor structure 200, wherein the first semiconductor element 210 comprises first silicide portions 241, the composition and/or the thicknesses of which are adapted to provide for the required sheet resistance in the silicon-containing semiconductor regions 214 and 215. Similarly, the second semiconductor element 230 comprises second silicide portions 243 adapted to meet the specific requirements of the second semiconductor element 230. As previously noted, the first silicide portions 241 and/or the second silicide portions 243 may comprise a noble metal such as platinum, palladium, gold and the like, in combination with refractory metals such as cobalt, titanium, zirconium, tungsten and the like. Moreover, the thickness of the first and second silicide portions 241, 243, that is the degree of "penetration" of the silicide in the depth direction into the region 214, 215, 234 and 235, is adjusted to obtain the required sheet resistance. If, for example, the first semiconductor element represents a p-channel transistor in which the peak concentration of p-type dopants is located at a depth of approximately 200 nm, the thickness, *i.e.*, the penetration, of the silicide portion may be adjusted to about 180-220 nm. Similar considerations apply to an n-channel transistor, which generally exhibits a shallow dopant profile.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. For example, the process steps set forth above may be performed in a different order. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

CLAIMS

1. A method of forming a semiconductor device, the method comprising:

providing a substrate 201 having formed thereon a first and a second conductive silicon-containing region;

forming a first resist mask 250 for covering the second conductive silicon-containing region and exposing the first conductive silicon-containing region;

depositing a first metal layer 240 of a first predefined thickness over the substrate 201;

removing the first resist mask 250;

forming a second resist mask 255 for covering the first conductive silicon-containing region and exposing the second conductive silicon-containing region;

depositing a second metal layer 242 of a second predefined thickness over the substrate 201;

removing the second resist mask 255; and

heat-treating the substrate 201 to form a first silicide portion 241 in the first conductive silicon-containing region and a second silicide portion 243 in the second conductive silicon-containing region.

2. The method of claim 1, wherein depositing the first metal layer 240 includes controlling the metal deposition such that a step coverage of the first resist mask 250 is minimized.

3. The method of claim 2, wherein the step coverage is minimized by employing a vapor deposition technique in which metal particles hit the substrate 201 substantially perpendicularly.

4. The method of claim 3, wherein a collimator is used to adjust the directionality of metal particles hitting the substrate 201 .

5. The method of claim 2, wherein the step coverage is minimized by sputter depositing the first metal layer 240 while controlling the directionality of the metal particles so as to be substantially perpendicular to the surface of the substrate.

6. The method of claim 1, wherein depositing the second metal layer 242 includes controlling the metal deposition such that a step coverage of the second resist mask 255 is minimized.

7. The method of claim 6, wherein the step coverage is minimized by employing a vapor deposition technique in which metal particles hit the substrate 201 substantially perpendicularly.

8. The method of claim 6, wherein the step coverage is minimized by employing a physical vapor deposition technique including a collimator in the vicinity of the substrate 201.

9. The method of claim 6, wherein the step coverage is minimized by sputter depositing the second metal layer 242 while controlling the directionality of the metal particles so as to be substantially perpendicular to the surface of the substrate 201.

10. The method of claim 1, wherein the substrate 201 comprises at least one third conductive silicon-containing region, and wherein the method further includes:

forming a third resist mask to cover the first and second metal layers and to expose the third conductive silicon-containing region;

depositing a third metal layer; and

removing the third resist mask, wherein during the heat treatment a third silicide portion is formed in the third conductive silicon-containing region.

11. The method of claim 1, wherein at least one of a type of metal and layer thickness of the first 240 and second 242 metal layers, temperature and duration of the heat treatment are selected to attain a first and a second sheet resistance in the first 241 and second 243 silicide portions such that the first and second sheet resistances are within corresponding predefined ranges, respectively.

12. The method of claim 1, wherein at least one of the first 240 and second 242 metal layers comprises at least one of cobalt, titanium, tantalum, zirconium, nickel, tungsten and a combination thereof.

13. The method of claim 1, wherein at least one of the first 240 and second 242 metal layers comprises one of platinum, palladium and gold.

14. A method of forming a semiconductor device, the method comprising:

forming a plurality of conductive silicon-containing regions on a substrate 201 ;

sequentially depositing a plurality of different metal layers 240, 242 on the substrate 201 using a plurality of deposition masks 250, 255 such that each of the plurality of conductive silicon-containing regions is substantially covered by one of the plurality of metal layers 240, 242, the metal layers differing from each other by at least one of type of material and layer thickness;

annealing the substrate 201 at a first average temperature for a first time interval to form a metal silicide portion on each of the plurality of conductive silicon-containing regions;

removing excess metal that has not reacted with the underlying material; and

annealing the substrate 201 at a second average temperature for a second time interval, wherein at least one of the first and second average temperatures and the first and second time intervals are controlled to adjust a thickness of the metal silicide portions.