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(54) A CHARGE-COUPLED LINEAR IMAGING DEVICE

(71) We, FAIRCHILD CAMERA AND INSTRUMENT CORPORATION, a Corporation duly organized and existing under the laws of the State of Delaware, United States of America, of 464 Ellis Street, Mountain View, California 94042, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to imaging devices and in particular to a linear imaging device using charge coupled device technology.

W. S. Boyle and G. E. Smith describe the basic concept of charge coupled semiconductor devices in an article published in the April 1970 Bell System Technical Journal, page 587, entitled "Charge Coupled Semiconductor Devices".

As described by Boyle and Smith,, a charge coupled device (hereinafter called a "CCD") consists of a metal-insulator-semiconductor (MIS) structure in which minority carriers are stored in a "spatially defined depletion region" also called a "potential well", at the surface of the semiconductor material. This charge is moved along the surface by moving the potential energy minimum. This potential energy minimum will be a maximum voltage (where the word voltage is used in its conventional sense) when the charge carriers are electrons and a minimum voltage when the charge carriers are holes. A paper on page 593 of the same Bell System Technical Journal by Amelio et al entitled "Experimental Verification of the Charge Coupled Device Concept" describes experiments carried out to demonstrate the feasibility of the charge coupled device concept.

As discussed by Boyle and Smith, charge coupled devices are potentially useful as shift registers, delay lines, and in two dimensions, as imaging or display devices.

A CCD linear imaging array of the prior art detected a linear image by generating charge beneath each electrode in the CCD array proportional to the intensity of the im-

pinging light. To read out the detected image, the generated charge representing the detected image is shifted along the detecting array by selectively varying the potentials on the electrodes. One problem with this type of linear imaging array is that the detected image is degraded by the continuous impinging of light on the array while the image is being read out. One way of improving the quality of the detected image is to increase the speed of reading out the charge. The speed of read out, however, is limited by the frequency response of the circuit.

In accordance with the present invention there is provided a linear imaging array comprising: a line of light-sensitive elements including a plurality of transparent electrodes formed on the top surface of a layer of insulation formed over a semi-conductor material, said elements being sensitive to infrared, visible, or ultraviolet radiation;

a first CCD shift register located on one side of the said line of light-sensitive elements;

a second CCD shift register located on the other side of said line of light-sensitive elements, said shift registers being covered with an opaque material;

means for transferring charge packets generated in said line of light-sensitive elements to appropriate positions in said first shift register and said second shift register;

first means for shifting said charge packets along said first and second shift registers; and means for receiving said charge packets at the end of said first and second shift registers.

This invention overcomes some of the difficulties of the prior art CCD linear imaging arrays. In particular, this invention overcomes the degradation of the detected image by the continuous impingement of light on the detecting array while the charge representing the image is being read out of the array.

In one embodiment of this invention, the light-sensitive elements as well on each shift register are all CCD linear arrays. The CCD linear array, usually includes a buried channel to give to the arrays a much better dynamic range than is obtained without such a chan-

nel. In another embodiment of this invention, only the shift registers are CCD linear arrays.

If desired, a preamplifier is incorporated on the same semi-conductor chip with the light-sensitive elements and shift registers to give a better signal-to-noise ratio than heretofore obtained.

When the light sensitive elements comprise charge coupled devices, the electrodes (often called "gates") of the charge coupled devices are transparent to give a greater average quantum efficiency than obtainable with opaque gates.

FIG. 1 shows a cross-sectional view of a buried channel charge coupled device;

FIGS. 2a and 2b show top and cross-sectional views of a linear imaging array constructed according to this invention;

FIG. 3 shows schematically a plan view of the functional arrangement of the linear imaging array shown in FIG. 2a;

FIG. 4 shows an alternative output circuit for processing the signals transmitted by the transport arrays 34a and 34b in FIG. 3;

FIG. 5 shows in block diagram form, one output circuit for processing the signals generated by the detected charge; and

FIGS. 6a through 6j show waveforms of use in explaining the operation of the structure of this invention.

FIG. 1 shows a charge coupled device comprising a semiconductor substrate 11 in which is formed buried channel 14. As shown in FIG. 1, substrate 11 is of P type conductivity. It should be understood, however, that the conductivity type of the various regions to be described in device 10 can be reversed and thus the following description is not to be interpreted as limiting the disclosed invention to the conductivity types described. Also, while the CCD devices employed in the embodiments of this invention described in this specification have a buried channel such as channel 15, if desired, this buried channel can be omitted.

While substrate 11 will be described as consisting of silicon semiconductor material, it should be noted that this invention can be used with any semiconductor material in which a charge coupled device can be formed.

The structure shown in FIG. 1 has insulation 15 formed over the top surface of substrate 11. Typically, insulation 15 is an oxide of semiconductor material 11 and when material 11 is silicon, comprises a silicon oxide. Overlying the top surface of silicon oxide layer 15 in a repetitive serially-spaced manner are electrodes 16a, 16b, 16c, 16d, 16e and 16f, comprising polycrystalline silicon doped with a selected impurity, the electrodes being separated from adjacent electrodes by regions of resistive undoped polycrystalline silicon. In addition, an output

electrode (often called a "gate") is shown just to the right of electrode 16f. While only six electrodes are shown on the structure of FIG. 1, it should be understood that different numbers of electrodes, as desired, can be used in a charge coupled device. Electrodes 16a through 16f are contacted by output leads 17a through 17f. Depending upon the type of operation desired, output leads 17a through 17f can be connected so that the CCD device operates as a three or more phase system. P+ type regions 12a and 12b represent in cross section a closed channel stop region. This channel stop region, typically formed by diffusion, decreases the sensitivity of the device to leakage currents and forms a closed path around that portion of the surface of device 10 beneath which the charge generated by incident light is stored and transferred. Region 13, of N+ type conductivity, forms with substrate 11 an output diode for receiving charge transmitted along the charge coupled device and for producing an output signal in response thereto. Lead 19 contacts regions 13.

A layer 14 of opposite conductivity type to the predominant conductivity of substrate 11 is formed in the top surface of substrate 11 beneath oxide layer 15. Preferably, layer 14 is formed using ion implantation techniques. The thickness of this layer at the completion of all high-temperature processing steps is, in one embodiment, 4,999 angstroms. Layer 14 provides a buried potential well which allows minority carriers (minority with respect to the predominant carrier in P type substrate 11) to be stored and transferred in the buried layer in the bulk semiconductor material near the interface of semiconductor substrate 11 and insulation 15 rather than at this interface. The structure shown in FIG. 1 will not be described in further detail, but is described here to illustrate the cross section of a portion of one type of CCD linear array used in one embodiment of this invention.

FIG. 2a shows a top view of a linear imaging array constructed using charge coupled device technology in accordance with the principles of this invention. Neither FIG. 2a nor the other figures are drawn to scale; rather, many of the features shown in the figures are distorted for illustrative convenience.

A linear array of light-sensitive elements 32-1 through 32-14 extends along the middle of the structure shown in FIG. 2a. These light-sensitive elements, shown in plan view FIG. 2a, are arranged in two groups; a first group comprising the odd-numbered light-sensitive elements 32-1, 32-3, 32-5, etc. all read out to the left of FIG. 2a and an even-numbered group of light-sensitive elements 32-2, 32-4, 32-6, etc. all read out to the right of FIG. 2a. In

the embodiment shown in FIGS 2a and 3, light-sensitive elements 32 comprise a linear array of charge-coupled devices, with the light-sensitive regions of semiconductor material covered by a single electrode rather than a corresponding plurality of electrodes as in a typical CCD shift register. As will be seen shortly, the charge generated in such a linear imaging array is first shifted out of the imaging array substantially perpendicular to the array before being further processed. A plurality of electrodes, properly connected to yield this result, could be used in place of single electrodes, if desired.

For the purpose of this specification the word "light" means any electromagnetic radiation which produces free charge in the depletion region of semiconductor material. Typically "light" includes infrared, visible and ultraviolet radiations.

While the light-sensitive elements 32—1, 32—2, 32—3 etc. in general comprise depletion regions formed in underlying semiconductor material as part of a charge coupled device, these elements can be photodiodes.

A channel stop 31 (FIGS. 2a and 2b) is formed around three sides of each light-sensitive element 32—i (where i is an integer with a value given by $1 \leq i \leq K$ and K is the maximum number of light-sensitive elements 32) in such a manner that the channel stop forms a continuous region from one end of the light-sensitive elements 32 to the other, twisting in a serpentine fashion so as to be on three sides of each light-sensitive element. Thus, the channel stop forms a "U-shape" around each light-sensitive element, with the U being located on its side, and the legs of the U pointing either to the right or the left of FIG. 2a (when the drawing is properly oriented to be read) depending upon whether the light-sensitive element is an even-numbered element or odd-numbered element, respectively. The channel stop region 31, of like conductivity type to the predominant conductivity type of the semiconductor material in which the light-sensitive elements 32 are formed, effectively isolates each light-sensitive element 32—i from adjacent light-sensitive elements 32—(i-1) and 32—(i+1) and thus substantially defines the area of each light-sensitive element 32—i. While in FIG. 2a K equals 14, K can, in general, equal any appropriate number, depending on design requirements.

A pair of transfer gates 33a and 33b control the transfer of charge from the odd-numbered light-sensitive elements 32—1, 32—3, 32—5 . . . and the even-numbered light-sensitive element 32—i. While in FIG. . . . respectively. To the left and right of transfer gates 33—1 and 33—2 respectively are located electrodes (shown schematically as areas 34a and 34b, respectively) such as electrodes 16a through 16f (FIG. 1) to form

transport arrays 34a and 34b which in one embodiment of this invention comprise two charge coupled device analog shift registers. These transport arrays covered with an opaque material such as aluminum are parallel to, and on either side of, light-sensitive elements 32.

To provide proper direction to the charge packets being transferred from elements 32 to transport arrays 34a and 34b, the channel stop region can include the "L"-shaped extensions 31—1, 31—2, etc. shown in FIG. 2a. These extensions give to the charge packets the directions shown by the arrows in FIG. 3.

FIG. 3 shows the layout of the elements shown in FIG. 2a and described above. Light-sensitive elements 32 contain charge generated by incident radiation. The charge generated in light-sensitive area 32—1 is transferred by appropriate adjustment of the potentials on the leads labeled ϕ_n , connected to gate 36), ϕ_x (connected to transfer gates 33—1, 33—2 etc.) and ϕ_v (connected to gates 34—1, 34—7, 34—13 etc., which are part of electrode string 34a and also to electrodes 34—2, 34—8, 34—14 etc. which are part of electrode string 34b) to the appropriate location in transport array 34a. To transfer charge from the odd-numbered light sensing elements 32—1, 32—3 . . . (hereinafter called the "odd elements") the potential on the ϕ_n lead is raised, the potential on the ϕ_x lead is held at a neutral level and the potential of the ϕ_v lead 35—1 is raised to a maximum level thereby causing charge generated and stored in light sensitive element 32—1 to transfer to a region underlying gate 24—1. Simultaneously, the charge generated and stored in light sensitive element 32—3 is transferred from this element to the region beneath electrode 34—7. Similar transfers of charge occur simultaneously from all the odd elements.

In a similar fashion, and at the same time, charge stored in light sensitive element 32—2 is transferred to the region beneath gate 34—2 in response to the same arrangement of potentials. Simultaneously, the charges stored in all the other even-numbered, light-sensitive elements 32—4, 32—6 etc. in line 32 (hereinafter called the "even elements") are transferred to the regions of semiconductor material beneath gates 34—8, 34—14 etc. in the right CCD analog shift register 34b.

CCD analog shift registers 34a and 34b are each identical in operation to the other. Therefore, the operation of CCD analog shift register 34a will be briefly described and it should be understood that CCD analog shift register 34b operates in an identical fashion.

FIGS. 6a through 6k show the potentials as a function of time on leads 35—1, 35—2, 35—3 and 38—1, 38—2 and 38—3. The abscissa of the curves shown in Figs. 6a

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through 6j is time, with the units of time (one such unit of time will hereinafter be called the "base period") being equal to one third the periods of the clock signals ϕ_{H1} , ϕ_{H2} and ϕ_{H3} on leads 38—1 through 38—3. Note that the periods of these clock signals are half those of the clock signals ϕ_{V1} , ϕ_{V2} and ϕ_{V3} on leads 35—1 through 35—3.

For convenience, the zero time in FIG. 6a through 6j is placed 19 base periods after the beginning of the abscissas of these curves. To transfer charge packets from the light-sensitive elements 32 (FIG. 3) into the areas beneath electrodes 34—1, 34—7, 34—(n—1), in CCD shift register 34a, and beneath electrodes 34—2, 34—8, 34—n in CCD shift register 34b, the voltage labeled ϕ_v (FIG. 3) is lowered to a minimum value (FIG. 6a) during the base periods —14 to —5 (i.e. the electron energy potential is raised to a maximum level). During the base periods —15 to about —9, the ϕ_x signal on leads 33a and 33b (FIG. 6b) is raised to its maximum voltage or minimum electron energy potential. From about —9 base periods to —8 base period the voltage level of the ϕ_x signal drops back to its low value. From —14 base period to —4 base period the ϕ_{v1} signal on lead 35—1 goes to a maximum voltage (i.e. to an electron energy minimum) (FIG. 6c). Therefore charge is transferred from the light-sensitive elements 32 through the semiconductor material beneath the gates 33—1, 33—2, 33—3, 33—4 etc. to regions of semiconductor material beneath electrodes 34—1, 34—7 etc. and 34—2, 34—8 etc. The ϕ_{v2} and ϕ_{v3} clock signals on leads 35—2 and 35—3 respectively are held at a minimum voltage (maximum electron energy) (FIGS. 6d, 6e) during the transfer of charges from the light sensitive areas 32 to the selected locations in the transport arrays 34a and 34b. At —4 base period, the ϕ_{v1} signal voltage rises abruptly to a maximum level. At the same time the ϕ_{v1} voltage begins to drop.

Therefore, the charge stored beneath, for example electrode 34—1 (FIG. 3) is transferred to beneath electrode 34—3. The charge stored beneath electrode 34—7 is prevented from being transferred to beneath electrode 34—3 by the low voltage (i.e. high electron energy) of the ϕ_{v3} signal on lead 35—3. Simultaneously, therefore, the charge beneath electrode 34—7 is transferred to beneath electrode 34—9. At —2 base period, the voltage of the ϕ_{v3} signal rises abruptly to its maximum value and simultaneously the voltage of ϕ_{v2} begins to drop gradually to its minimum value. The voltage of the ϕ_{v1} signal is now at a minimum and remains at this minimum for two base periods. Thus charge is now transferred from, for example, beneath electrode 34—3 to beneath electrode 34—5. The charge continues

to be transferred once every two base periods from beneath a given electrode 34—i to a region beneath the next following electrode 34—(i+2). Thus the charges transferred from light-sensitive elements 32 to beneath selected ones of electrodes 34 are now transferred along transport arrays 34a and 34b.

During the transfer of this charge along shift registers 34a and 34b, the voltage on transfer gates 33a and 33b is held at a low level (i.e. electron energy is held at a high level) to prevent charge being accumulated in elements 32 from being transferred into these analog shift registers. Thus, degradation of the signal due to additional radiation incident on the light-sensitive elements 32 is prevented.

It should be noted that transport arrays 34a and 34b are covered with an opaque material to prevent light incident on light-sensitive elements 32 from likewise falling on the depletion regions associated with transport arrays 34a and 34b and thereby generating additional charge which degrades the image detected by light-sensitive elements 32.

Note that while the charge is being transferred along registers 34a and 34b, charge is also being transferred along shift register 37. This charge, however, is transferred at twice the frequency as is the charge transferred along registers 34a and 34b with the result that a given charge packet is moved six electrodes along register 37 in the time necessary to move a charge packet three electrodes in registers 34a and 34b. In one embodiment register 37 is also a CCD shift register of the same type as shift registers 34a and 34b.

CCD shift register 37 is driven in such a manner that when packets of charge are located beneath electrodes 34—(n+9) and 34—(n+10) these charge packets will be transferred to beneath electrodes 37—1 and 37—4 in shift register 37. Thus as shown in FIG. 6c, the voltage on electrodes 34—(n+9) and 34—(n+10), which are connected to lead 35—3 carrying the ϕ_{v3} signal is at a high level for the first two base periods and then drops to a low level for the third and fourth base periods. This voltage remains at a low level for the fifth and sixth base periods after which it rises abruptly to a high voltage level. During the third base period, the ϕ_{H3} signal is at a high voltage (i.e. minimum electron energy). It is during this period that the voltage of the ϕ_{v1} signal on lead 35—1 begins to drop. Thus the charge stored beneath electrode 34—(n+9) transfers from beneath this electrode to beneath electrode 37—1. Simultaneously, and for the same reason, the charge beneath electrode 34—(n+10) is transferred to beneath electrode 37—4.

An analysis of FIGS. 6f, 6g and 6h shows

(14)

that the charge stored beneath electrode 37—1 and 37—4 is then transferred along shift register 37 in the same manner as are the charge packets transferred along shift registers 34a and 34b but at twice the frequency. By the time the next packets of charge are beneath electrodes 34—(n+9) and 34—(n+10) the charge packets formerly transferred from beneath these electrodes to beneath electrodes 37—1 and 37—4 have been transferred towards diode 38 and have been or will be used to generate an output signal by devices 39 and 40.

Devices 39 and 40 comprise MOS transistors wherein the gate of MOS transistor 40 is connected to the cathode of diode 38 and the source of MOS transistor 39. The drain of transistor 39 is connected to a voltage source V_{DR} . Voltage sources V_{DR} is typically between 10 to 15 volts. MOS transistors 39 and 40 are n-channel devices with the n-channel, in one embodiment, being formed by ion implantation simultaneously with the formation of the n-type layer 14 (FIGS. 1 and 2b). Transistor 39 is such that when its gate voltage, denoted ϕ_R (FIG. 6f) is high, transistor 39 is turned on, thereby charging reversed-biased diode 38 to approximately the voltage of V_{DR} . Upon dropping the gate voltage ϕ_R approximately ground, transistor 39 turns off, thereby disconnecting voltage source V_{DR} from diode 38. Diode 38, however, acts as a capacitor and thus retains the charge placed on it by source V_{DR} . Upon transfer of a packet of charge from beneath electrode 37—7 to the N type region of diode 38, the voltage across this diode drops. The cathode of diode 38 is connected to the gate of n-channel MOS transistor 40. The drop in voltage on the cathode of diode 38 lowers the gate voltage on MOS transistor 40 thereby changing the conductivity of the n-channel between the source and drain of this transistor. Accordingly, the current flowing from voltage source V_D (particularly about 10 to 15 volts) to voltage source V_s is modulated by the amount of voltage drop across diode 38. Once each three base periods, diode 38 is recharged. Therefore, each charge packet transferred from beneath electrode 37—7 to the N type region (region 33, FIG. 1) changes the voltage across diode 38 from its recharged value to some new value reflecting the magnitude of this charge. Accordingly, the change in current flowing through the channel of MOS transistor 40 (FIG. 6j) is a measure of the detected signal.

The analog CCD shift registers 34a, 34b and 37 each can be constructed as shown in cross section in FIG. 1. The channel stop region 31 (FIG. 2) winds along the array of linear light-sensitive elements 32 separating each element 32—i in essence from the adjacent elements 32—(i-1) and 32—(i+1)

and forcing the charge generated in a given element to travel in such a manner that it ends up beneath the proper electrode in shift registers 34a and 34b when the proper potentials are applied to electrode 36 (FIG. 2a) and to the transfer gates 33a and 33b and the electrodes in shift registers 34a and 34b.

The charge packets can be transferred from the light-sensitive elements 32—1 through 32—K, where K is a selected positive integer representing the maximum number of light sensitive elements, 32 one each readout period of CCD analog shift registers 34a and 34b. By "readout periods" is meant at least the time necessary for charge packets beneath electrodes 34—1 and 34—2 to reach the area beneath, for example, electrodes 34—(n+9) and 34—(n+10). Thus, transfer of additional charge into the CCD analog shift registers 34a and 34b from light sensitive elements 32 will not degrade or interfere with the charge packets previously detected and transferred.

FIGS. 4 and 5 show other techniques for processing the charge packets generated in light sensitive elements 32—1 through 32—K. In FIG. 5 the CCD sensors and registers 100 produce output charges which are detected by preamp 101. CCD sensors and registers 100 could be structures described above in conjunction with FIG. 3 for example. The output signal from sensors and registers 100 is set to preamp 101 which in one embodiment comprises diode 38 and transistors 39 and 40 shown in FIG. 3. Preamp 101 is driven by a signal from reset clock 106. In addition, dummy preamp 102 is also driven by a reset clock 106. Differential amplifier 103 then compares the output signals from preamp 101 and preamp 102 sensing the difference. Accordingly, the output signal from differential amplifier 103 has had the coherent noise resulting from clock 106 removed from this signal.

A sample and hold circuit 104 produces an output signal which is transmitted to a driver and dc level control circuit 105. The output signal from driver and dc level control 105 can be sent to monitor 107 if desired where the output signal can be used or evaluated.

FIG. 4 shows an additional technique for reading out the charge signals transmitted along transfer arrays 34a and 34b. Rather than use an additional CCD shift register 37 as shown in FIG. 3, the signals used to drive one transport array are delayed by a selected amount relative to the signals used to drive the other transport array. The output signals from the transport arrays are then transmitted directly to diodes 110 and 111 such as diode 13 (FIG. 1) or diode 38 (FIG. 3) and there used to change the voltage across these diodes. The diodes 110

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and 111 are periodically recharged by current from source V_{DR} attached to the drain of MOS transistor 112. MOS transistor 112 is periodically gated by a signal ϕ_R such as shown in FIG. 6i. The cathodes of diodes 110 and 111 are connected to the gate of MOS transistor 113. Changes in the voltage across diodes 110 and 111 as a result of the receipt of a charge packet from either transport array changes the voltage of the gate on MOS transistor 113 and thus changes the current passed from the source to drain of this transistor. This change in current represents the magnitude of the particular charge packet changing the voltage on the particular one of the diodes 110 and 111 and is used to generate an output signal.

This invention has the advantage that all the components and elements shown in FIG. 3 can be formed on one monolithic chip of semi-conductor material.

While this invention has been described as using three phase CCD analog shift registers for registers 34a, 34b and 37, two phase and even one phase register can also be used for these shift registers, if desired, CCD analog shift registers operating in the two phase mode are described in an article by R. H. Krambeck, R. H. Walden and K. A. Pickar, entitled "Implanted-Barrier Two-Phase Charge-Coupled Device", published in Applied Physics Letters, Vol. 19, No. 12, pp. 520-522, 1971.

One feature of this invention which yields an added flexibility in the design of linear imaging arrays is that the regions of the transport arrays 34a and 34b extends beyond the last element 32-K (FIG. 3) of the linear imaging array. These extensions of transport arrays 34a and 34b can thus be bent in such a manner that they properly intersect with the utilization structure designed to receive the charge from arrays 34a and 34b. This utilization structure corresponds, for example, to shift register 37 shown in FIG. 3.

WHAT WE CLAIM IS:—

1. A linear imaging array comprising:

a line of light-sensitive elements including a plurality of transparent electrodes formed on the top surface of a layer of insulation formed over a semiconductor material, said elements being sensitive to infrared, visible or ultraviolet radiation;

a first CCD shift register located on one side of the said line of light-sensitive elements;

a second CCD shift register located on the other side of said line of light-sensitive elements, said shift registers being covered with an opaque material;

means for transferring charge packets generated in said line of light-sensitive elements to appropriate positions in said first shift register and said second shift register;

first means for shifting said charge packets along said first and second shift registers, and means for receiving said charge packets at the ends of said first and second shift registers.

2. An array according to claim 1, wherein said means for receiving charge packets comprises:

a third shift register covered with an opaque material located at the ends of said first shift register and said second shift register for receiving said charge packets from said first shift register and said second shift register and

means for sensing the magnitudes of said charge packets.

3. An array according to claim 1 or 2, wherein said first means for shifting said charge packets comprises means for driving said charge packets along said first shift register and said second shift register at a first selected frequency.

4. An array according to claim 3 when dependent on claim 2, including:

second means for shifting said charge packets along said third shift register at a second frequency, said second frequency being twice said first frequency.

5. An array according to claim 2 including:

output circuitry means at the output end of said third shift register for receiving said charge packets from said third shift register and for generating output signals in proportion thereto.

6. An array according to any preceding claim, wherein said plurality of electrodes are interconnected.

7. An array according to any preceding claim, wherein said semi-conductor material is of one conductivity type and has formed in the top surface thereof a region of opposite conductivity type.

8. An array according to claim 7, wherein said region of opposite conductivity type extends through the regions of said first and second shift registers, said means for transferring, and said line of light-sensitive elements.

9. An array according to claim 7 or 8, wherein said one conductivity type is P type and said opposite conductivity type is N type.

10. An array according to any preceding claim, wherein said semi-conductor material is silicon.

11. An array according to any preceding claim, wherein said insulation is an oxide of silicon.

12. An array according to any preceding claim, wherein said electrodes comprise polycrystalline silicon doped with a selected impurity.

13. An array according to claim 12, wherein said polycrystalline silicon electrodes are

and 111 are periodically recharged by current from source V_{DR} attached to the drain of MOS transistor 112. MOS transistor 112 is periodically gated by a signal ϕ_R such as shown in FIG. 6i. The cathodes of diodes 110 and 111 are connected to the gate of MOS transistor 113. Changes in the voltage across diodes 110 and 111 as a result of the receipt of a charge packet from either transport array changes the voltage of the gate on MOS transistor 113 and thus changes the current passed from the source to drain of this transistor. This change in current represents the magnitude of the particular charge packet changing the voltage on the particular one of the diodes 110 and 111 and is used to generate an output signal.

This invention has the advantage that all the components and elements shown in FIG. 3 can be formed on one monolithic chip of semi-conductor material.

While this invention has been described as using three phase CCD analog shift registers for registers 34a, 34b and 37, two phase and even one phase register can also be used for these shift registers, if desired, CCD analog shift registers operating in the two phase mode are described in an article by R. H. Krambeck, R. H. Walden and K. A. Pickar, entitled "Implanted-Barrier Two-Phase Charge-Coupled Device", published in Applied Physics Letters, Vol. 19, No. 12, pp. 520-522, 1971.

One feature of this invention which yields an added flexibility in the design of linear imaging arrays is that the regions of the transport arrays 34a and 34b extends beyond the last element 32-K (FIG. 3) of the linear imaging array. These extensions of transport arrays 34a and 34b can thus be bent in such a manner that they properly intersect with the utilization structure designed to receive the charge from arrays 34a and 34b. This utilization structure corresponds, for example, to shift register 37 shown in FIG. 3.

WHAT WE CLAIM IS:—

1. A linear imaging array comprising:

a line of light-sensitive elements including a plurality of transparent electrodes formed on the top surface of a layer of insulation formed over a semiconductor material, said elements being sensitive to infrared, visible or ultraviolet radiation;

a first CCD shift register located on one side of the said line of light-sensitive elements;

a second CCD shift register located on the other side of said line of light-sensitive elements, said shift registers being covered with an opaque material;

means for transferring charge packets generated in said line of light-sensitive elements to appropriate positions in said first shift register and said second shift register;

first means for shifting said charge packets along said first and second shift registers, and means for receiving said charge packets at the ends of said first and second shift registers.

2. An array according to claim 1, wherein said means for receiving charge packets comprises:

a third shift register covered with an opaque material located at the ends of said first shift register and said second shift register for receiving said charge packets from said first shift register and said second shift register and

means for sensing the magnitudes of said charge packets.

3. An array according to claim 1 or 2, wherein said first means for shifting said charge packets comprises means for driving said charge packets along said first shift register and said second shift register at a first selected frequency.

4. An array according to claim 3 when dependent on claim 2, including:

second means for shifting said charge packets along said third shift register at a second frequency, said second frequency being twice said first frequency.

5. An array according to claim 2 including:

output circuitry means at the output end of said third shift register for receiving said charge packets from said third shift register and for generating output signals in proportion thereto.

6. An array according to any preceding claim, wherein said plurality of electrodes are interconnected.

7. An array according to any preceding claim, wherein said semi-conductor material is of one conductivity type and has formed in the top surface thereof a region of opposite conductivity type.

8. An array according to claim 7, wherein said region of opposite conductivity type extends through the regions of said first and second shift registers, said means for transferring, and said line of light-sensitive elements.

9. An array according to claim 7 or 8, wherein said one conductivity type is P type and said opposite conductivity type is N type.

10. An array according to any preceding claim, wherein said semi-conductor material is silicon.

11. An array according to any preceding claim, wherein said insulation is an oxide of silicon.

12. An array according to any preceding claim, wherein said electrodes comprise polycrystalline silicon doped with a selected impurity.

13. An array according to claim 12, wherein said polycrystalline silicon electrodes are



separated from adjacent electrodes by regions of resistive undoped polycrystalline silicon.

5 14. An array according to any preceding claim when dependent on claim 2, wherein said first, second and third shift registers comprise a plurality of electrodes formed on an insulating layer overlying semiconductor material of one conductivity type.

10 15. An array according to claim 14, wherein said semiconductor material is of one conductivity type and has formed in one surface adjacent and underlying said insulation, regions of opposite conductivity type.

15 16. An array according to claim 15, wherein said region of one conductivity type is of P type conductivity and said region of opposite conductivity type is of N type conductivity.

20 17. An array according to any of claims 14 to 16, wherein said electrodes in said first, second and third shift registers are selectively doped regions of polycrystalline silicon.

25 18. An array according to claim 17, wherein said electrodes in each of said first, second and third shift registers are separated by regions of undoped polycrystalline silicon.

19. An array according to claim 1, wherein said light-sensitive elements are separated

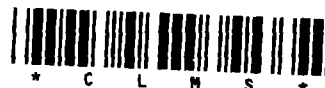
from adjacent light-sensitive elements by a heavily doped channel stop region formed in the top surface of the semiconductor material, said heavily doped channel stop regions surrounding each light-sensitive element on three sides such that every light-sensitive element has open to one of said first and second shift registers a side on which there is no channel stop region.

20. An array according to claim 19, wherein said channel stop region includes a plurality of selectively shaped extensions thereof for ensuring that said charge packets are transferred from said line of light-sensitive elements to the appropriate locations in said first and second shift registers.

21. An imaging array substantially as hereinbefore described with reference to the accompanying drawings.

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ERRATUM

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