

ABSTRACT

ZERO WAIT STATE CACHE USING NON-INTERLEAVED BANKS OF ASYNCHRONOUS STATIC RANDOM ACCESS MEMORIES.

A zero wait state system cache memory for use in computer systems. The present invention utilizes banks of non-interleaved asynchronous Static Random Access Memories with separate control lines. Zero wait state performance is achieved by correlating control signals to the cache memory relative to the clock and control signals used by the processor so that there is zero delay in the provision of the system clock signal and the cache control signals. Processor burst access to memory is supported by an internal sequencer which determines subsequent burst addresses based on an initial burst address provided by the processor.

(Figure 5)