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PATENT SPECIFICATION

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DRAWINGS ATTACHED

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COMPLETE SPECIFICATION.

Correction of Distortion in Transversal Equalisers.

We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195, Broadway, New York City, New York State, United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to the correction of the distorting effects of transmission channels of limited frequency bandwidth on digital data intelligence signals.

In the copending Application No. 39326/65 (Serial No. 1,105,958), an automatic equalisation system employing a transversal filter is described. A transversal filter is a time domain network which comprises a plurality tapped delay line, an adjustable attenuator connected to each delay line tap, and a summing circuit for combining the attenuated outputs of all taps. The adjustable attenuator described in the copending application includes reversible electronic digital counter coupled to a resistive ladder with a large number of discrete incremental steps. During a training period preliminary to message data transmission these attenuator-counters are set to optimum values in a step-by-step procedure while test pulses are transmitted through the channel.

The algorithm for setting the attenuator multiplying factors through these counters can be simply stated. After each test pulse passes through the channel and the transversal filter, the resulting output pulse is sampled at intervals equal to the reciprocal of the data transmission rate. The multiplying factor is increased by one incremental step if the output sample is negative and

decreased by one incremental step, if positive. Even with only a finite number of attenuators available for simultaneous adjustment it has been established that the resultant distortion is optimally minimised by this algorithm.

While this algorithm is basically sound, the implementation requiring a training period prior to message transmission has one inherent disadvantage. The channel characteristic, optimally equalised at the beginning of the message, may change with time. In the course of a long message such a change in channel characteristics can be significant.

According to one aspect of this invention there is provided apparatus for establishing optimum settings for the multipliers in a transversal equaliser from a message data sequence received from a distorting transmission medium, comprising means for repeatedly determining error signals as the difference between time-spaced analog samples and standardised estimates of the data sequence in message signals received by said equaliser, means for repeatedly multiplying said error signals and a plurality of standardised estimates of the data sequence occurring with, before and after said error signals, means for separately integrating repeated products from said multiplying means for the duration of a predetermined plurality of successive error signals to obtain estimates of individual time-spaced interference components of the impulse response of said transmission channel, and means responsive to periodic polarity samples of the estimates of interference components in said integrating means for adjusting step-by-step said attenuators in a direction so as to reduce said interference components over a period of time.

According to another aspect of this in-

[Price 4s. 6d.]

vention there is provided a transversal equaliser for receiving from a distorting transmission medium polarity determinant binary data signals applied at a fixed transmission rate, comprising a transversal filter having at least a delay line portion with output taps at intervals compatible with said transmission rate, an incrementally adjustable attenuator connected to each such output tap and a summing circuit for combining the attenuated outputs of all such taps, means for obtaining samples of the analog output of said summing circuit at said fixed transmission rate, means for providing pulses at standardised amplitudes as quantized estimates of the polarity of samples of the analog output of said summing circuit, means for subtracting said quantized estimates from said analog samples as interference error signals, means for multiplying each individual error signal by a plurality of said quantized estimates including effective past, present and future estimates, means for averaging a preselected plurality of corresponding successions of products from said multiplying means as estimates of individual components of the impulse response of said transmission medium, means for detecting the polarity of averages from said averaging means at preselected multiples of said transmission rate, and means responsive to the detected polarities of said averages for incrementally changing the settings of said attenuators so as to reduce present distortion.

An embodiment of this invention can continuously estimate from a correlation of samples of the output of the transversal equaliser with the received polar data sequence the polarities of intersymbol interference components of the single-pulse impulse response of the transmission channel and use these polarities to determine the direction of successive incremental adjustments of the attenuators associated with the taps of the equaliser.

The intersymbol interference components of the effective impulse response of the transmission channel are estimated in the case of polar binary data transmission by sampling the analog output of the transversal equaliser at the data transmission rate, slicing these samples to detect the received data sequence, subtracting the present standardised received data symbol from the present analog output sample to determine a present error component, correlating the present error component with past, present and future received data bits within the range of the equaliser to obtain a series of product terms corresponding to successive sampling instants, and averaging a plurality of such product terms over a number of sampling intervals. The polarity of these average values are next determined by

a slicing circuit. The attenuators at each tap of the equaliser are finally incrementally adjusted in opposition to such polarity determinations.

All equaliser components may thus be in one location at the receiver with no answer-back detectors, switches or test pulse sources required at the data transmitter.

There may also be permanent connection of the attenuator-adjusting components to the transversal equaliser.

An embodiment of this invention will now be described by way of example with reference to the accompanying drawing which shows a block diagram of an adaptive equalisation system.

In the drawing, elements 10 to 19 are exact counterparts of a data transmission system including a transversal equaliser as described in the aforesaid application. Data source 10 generates polar binary synchronous message data at baseband. Through the medium of transmission channel 11 this data is transmitted either at baseband or after modulation onto a carrier frequency to a remote location and delivered at baseband after demodulation, if needed, to a utilisation circuit or data sink 19. Should the attenuation characteristic of transmission channel 11 be other than flat with frequency or the phase characteristic be other than linear with frequency, then the message signals delivered to data sink 19, in the absence of equalisation, will be spread out in time and mutually interfering.

To obviate distortion a transversal equaliser filter is inserted between transmission channel 11 and data sink 19. The transversal filter comprises a delay line 12 having a nonreflective termination 13 and a plurality of taps, such as those designated 14A to 14E, equally spaced therealong at intervals corresponding to the reciprocal of the synchronous data symbol rate; a plurality of adjustable attenuators, such as those designated 15A to 15E, each connected at the input end to a tap on delay line 12; and a summing circuit 16 serving as a common termination for the outputs of all attenuators 15. Between the output of summer 16 and data sink 19 are sampling gate 17 actuated at appropriate sampling times and binary slicer 18 for detecting and reconstructing standardised, marking and spacing data bits. Data sink 19 is any utilisation means for digital data such as a computer, business machine or record communication device.

A transversal filter, as is well known, operates to equalise a distorting channel by adjusting the reference tap attenuator to keep the main response uniform from pulse to pulse and by adjusting the side tap attenuators to achieve a balance among and to reduce the interfering components to

minimum values at sampling instants. According to the principles enunciated in the aforesaid copending application, distortion in a transmission channel can be minimised with a transversal filter of finite length as just described by detecting the polarity of samples of the outputs at each tap and advancing or retarding by incremental amounts the attenuator settings at each tap in opposition thereto. All the output samples in that equaliser result from the impulse response of the transmission channel to single pulses specially applied to the transmission channel for test purposes. It has since been discovered that these same principles can be applied adaptively, that is, the equivalent single-pulse response components can be estimated from the message data sequence in the normal course of data transmission.

A review of equaliser fundamentals is in order at this point. Data source 10 is assumed to generate a random synchronous sequence of data symbols a_n at T second intervals in accordance with the content of a message to be transmitted. These are to be delivered to data sink 19. Any individual a_n may with equal probability be either positive or negative. Each symbol a_n would evoke in an ideal transmission channel a time sequence $x(t)$, where $t = nT$, and n can take on all integral values between plus and minus infinity. Only at $n = 0$ does $x(t)$ have a large nonzero value. At all other values of n , $x(t) = 0$. Therefore, a sequence of data symbols a_n at times nT will be noninterfering.

In passage through a practical transmission channel 11 the ideal impulse response $x(t)$ is transformed into a nonideal response $h(t)$ in which, in addition to the principal nonzero component at $n = 0$, there can be and likely are significant nonzero components of either polarity at other values of n . Therefore, a sequence of data symbols a_n at times nT will generally be mutually interfering to a greater or lesser extent.

The transversal filter delay line 12 provides a practical means for separating the principal from the interfering components of the impulse response $h(t)$ at its output taps 14A to 14E at spacings of T seconds. Attenuators 15A to 15E at each of taps 14A to 14E can individually be adjusted to multiply the tap outputs by factors in the range of plus and minus one. The main component attenuator 15C at reference tap 14C is preferably adjusted to maintain the amplitude of the principal impulse response component h_0 uniform at all times. The other attenuators are adjusted to reduce to zero the side components of response $h(t)$, $n \neq 0$, within the range of the number of taps on delay line 12. Only five taps are

shown here to avoid cluttering the drawing. The summation of the individual outputs of attenuators 15A to 15E in summer 16 when the principal response component is centred at tap 14C and the attenuators are optimally set will be h_0 plus a minimum residual component due to the finite delay line length.

In the transversal equaliser of the cited copending application the attenuator settings were made on the basis of measurements of single impulse responses $h(t)$. In the illustrated embodiment of the accompanying drawing, these attenuator settings can also be made adaptively from measurements of the superposed impulse responses $h(t)$ in a normal message data sequence. With a succession of overlapping impulse responses $h(t)$ the overall response becomes an analog signal designated $y(t)$, where any individual sample y_m is equal to the summation of the separate products of succeeding data symbols a_{m-n} and the components of the single-pulse response h_n . For a particular case at an arbitrary second sampling time the summation becomes

$$y_2 = h_{-2}a_4 + h_{-1}a_3 + h_0a_2 + h_1a_1 + h_2a_0 \quad (1)$$

This summation is found at the output of the sampling gate 17 at the arbitrarily chosen second sampling time.

The principal and largest term in equation (1) is the product h_0a_2 . The remaining terms and others not written out are error components representing the total intersymbol interference at the particular sampling instant. The first requirement for determining attenuator settings is to isolate the error terms. These are generally small in comparison with the principal term. An estimate of the data symbol is obtained by slicing the output of the sampling gate 17 at each sampling instant in binary slicer 18, a threshold circuit of conventional type. Its output is the data symbol a_m which may be positive or negative. This symbol is delivered to data sink 19 and also is available on line 29.

On the assumption that the principal component h_0 of the impulse response remains constant from symbol to symbol and the output of slicer 18 is standardised at uniform amplitudes, the signal on line 29 is equivalent to the product h_0a_2 alone. The signal on line 28 is y_2 , also containing the term h_0a_2 among others. Subtractor 29 with inputs connected to lines 28 and 29 has in its output therefore the error portion of equation (1) at the second sampling instant. Subtractor 32 can conveniently comprise an inverter having its input connected to line 29 and an operational amplifier having one input connected to the inverter and the other input connected to line

28. The output of the operational amplifier is the output of the subtractor.

From the error terms in equation (1) it can be seen that if the error terms are multiplied by a_n , the next succeeding data symbol, the term $h_{n-1}a_n$ will have the polarity sign of h_{n-1} whether a_n is positive or negative. Each of the remaining terms, however, has an equal chance of being positive or negative as its polarity is determined jointly by the sign of the interference component and the sign of the data symbol. It can therefore be deduced that if the products of present error and the next succeeding data symbol are taken continuously and averaged over a reasonable length of time the impulse response term h_{n-1} will be isolated. The remaining error terms, being random, will tend to cancel out.

Similarly, averaging the products of the present error at the output of subtractor 32 and other near data symbols will produce the other impulse response terms. The remainder of the figure shows an arrangement for taking these products and averages.

The error output of subtractor 32 is delayed in a conventional delay unit 30 by the number of sampling times between the centre tap 14C of delay line 12 and the last tap 14E. For a five-tap delay line the delay required in delay unit 30 is twice that between adjacent taps on delay line 12. The purpose of delay unit 30 is to make possible effective correlation of past and future response components.

Successive data symbol estimates in the output of slicer 18 on line 29 are stored in the individual stages 24A to 24E of a conventional shift register. The contents of these stages are advanced from right to left under the control of advance pulses on line 27. Clock 25 produces clock pulses on line 27 at intervals of T seconds in a conventional manner and its operation may be synchronised as necessary with transitions in the received signal wave.

If the data symbol stored in centre stage 24C is considered the present symbol, then those stored in stages 24A and 24B are respectively the past-past and past symbols and those in stages 24D and 24E are the next two succeeding future symbols. Since the error signal on line 31 has been delayed two time units, multiplication of this error signal and the contents of centre shift register stage 24C represents a correlation of the present data symbol and the present error signal. Averaging a succession of such products results in a good estimate of principal impulse response component h_n . Similarly it is evident that correlation of the contents of the other shift register stages with the error signal on line 31 will

yield estimates of other impulse response components.

Accordingly, conventional multipliers 23A to 23E are provided at the outputs of the corresponding shift register stages 24A to 24E. The other multiplier inputs are connected in common to lead 31 bearing the error signal. Since the quantities stored in the shift register are merely polarity indicators, the multipliers can be inverting amplifiers taken in and out of the circuit according to the polarity of the contents of the shift register stages. Averaging of successive products is accomplished in low-pass filters 22A to 22E connected to the outputs of the corresponding multipliers 23A to 23E. The low-pass filters integrate successive inputs in a well-known manner.

A plurality of binary slicers 20A to 20E provide means for determining the polarity of the estimated impulse response components. The operation of these slicers in conjunction with up-down reversible counters associated with attenuators 15A to 15E is the same as described in the copending application.

The time over which the averaging of the products of the error signals and the data symbols is made is determined by counter 26 and gate 21. Counter 26 is driven by clock 25 and produces an output at some preset number of counts. Upon the appearance of the counter output, switches 21A to 21E, indicated symbolically in detached contact form as crosses, are operated in gate 21. The contents of low-pass filters 22 are thus connected periodically to slicers 20.

The adjustment of attenuator 15C at the reference tap 14C depends on a correlation of the present error and present data symbol. Therefore, the setting of this attenuator maintains the principal component h_n of the impulse response uniform from symbol to symbol and renders valid the assumption earlier made that the output of subtractor 32 is the error signal containing only interference components of the channel impulse response.

On the other hand, the adjustments of the remaining attenuators 15 depend on correlations of the present error signal and past or future data symbols. Therefore, these attenuators automatically tend to reduce the individual intersymbol interference components at sampling intervals in the error signal to minimum values.

The time over which successive samples should be averaged and consequently the count preset in counter 26 is a complex function of the size of the incremental steps provided in attenuators 15 and the degree of distortion and noise in transmission channel 11. For transmission over the average voice telephone lines at a trans-

mission rate of 2400 symbols per second it has been found that counter 26 should be set* to count to about 20 for a five-tap equaliser as shown in the drawing. A longer delay line will provide lower residual distortion. A shorter averaging time produces wrong attenuator settings. A longer averaging time increases the settling time without any increase in accuracy. Settling time refers to the interval required to bring the equaliser from a reference condition to its optimum settings at which time all attenuators are in the random walk condition. Any change in the transmission channel characteristics with time after the initial equalisation are automatically corrected.

The principle described in relation to the adaptive estimation of impulse response components from a normal message sequence is, however, applicable as well to a multilevel data sequence. In the multilevel case provision is made for making impulse response component estimates for each slicing level. Slicer 18 becomes multilevel and furnishes quantized samples of the analog output of the equaliser. A digital-to-analog converter is added between line 29 and subtractor 32 to facilitate the determination of the error signal. A shift register 24 is required for each slicing level. Similarly the remainder of multipliers 23, filters 22, switches in gate 21 and binary slicers are also increased in number.

35 WHAT WE CLAIM IS:—

1. Apparatus for establishing optimum settings for the multipliers in a transversal equaliser from a message data sequence received from a distorting transmission medium, comprising means for repeatedly determining error signals as the difference between time-spaced analog samples and standardised estimates of the data sequence in message signals received by said equaliser, means for repeatedly multiplying said error signals and a plurality of standardised estimates of the data sequence occurring with, before and after said error signals, means for separately integrating repeated products from said multiplying means for the duration of a predetermined plurality of successive error signals to obtain estimates of individual time-spaced interference components of the impulse response of said transmission channel, and means responsive to periodic polarity samples of the estimates of interference components in said integrating means for adjusting step-by-step said attenuators in a direction so as to reduce said interference components over a period of time.

2. A transversal equaliser for receiving from a distorting transmission medium polarity determinant binary data signals

applied at a fixed transmission rate, comprising a transversal filter having at least a delay line portion with output taps at intervals compatible with said transmission rate, an incrementally adjustable attenuator connected to each such output tap and a summing circuit for combining the attenuated outputs of all such taps, means for obtaining samples of the analog output of said summing circuit at said fixed transmission rate, means for providing pulses at standardised amplitudes as quantized estimates of the polarity of samples of the analog output of said summing circuit, means for subtracting said quantized estimates from said analog samples as interference error signals, means for multiplying each individual error signal by a plurality of said quantized estimates including effective past, present and future estimates, means for averaging a preselected plurality of corresponding successions of products from said multiplying means as estimates of individual components of the impulse response of said transmission medium, means for detecting the polarity of averages from said averaging means at preselected multiples of said transmission rate, and means responsive to the detected polarities of said averages for incrementally changing the settings of said attenuators so as to reduce present distortion.

3. An equaliser according to claim 2, wherein included in the means for detecting is means for periodically slicing the outputs of the means for averaging in accordance with the polarity thereof.

4. An equaliser according to claim 2 or 3, comprising means for continuously storing a plurality of successive estimated data symbols from said detecting means, means for delaying by a fixed number of periods the samples from said sample-taking means to enable effective correlation of each error signal from said subtracting means with a plurality of successive data symbols, including symbols coincident with, and occurring before and after each said error signal, and included in the means for multiplying are a plurality of product-taking means for multiplying each error sample by plus or minus one according to the polarity of the data symbol in said storing means.

5. An equaliser according to claim 4, wherein included in the storing means is a shift register having a plurality of stages for storing said successive estimated data symbols, and comprising a plurality of polarity inverters connected in common to said delaying means and individually to a stage of said shift register, the contents of the shift register stage determining whether the common input signal is effectively multiplied by plus or minus one.

mission rate of 2400 symbols per second it has been found that counter 26 should be set* to count to about 20 for a five-tap equaliser as shown in the drawing. A longer delay line will provide lower residual distortion. A shorter averaging time produces wrong attenuator settings. A longer averaging time increases the settling time without any increase in accuracy. Settling time refers to the interval required to bring the equaliser from a reference condition to its optimum settings at which time all attenuators are in the random walk condition. Any change in the transmission channel characteristics with time after the initial equalisation are automatically corrected.

The principle described in relation to the adaptive estimation of impulse response components from a normal message sequence is, however, applicable as well to a multilevel data sequence. In the multilevel case provision is made for making impulse response component estimates for each slicing level. Slicer 18 becomes multilevel and furnishes quantized samples of the analog output of the equaliser. A digital-to-analog converter is added between line 29 and subtractor 32 to facilitate the determination of the error signal. A shift register 24 is required for each slicing level. Similarly the remainder of multipliers 23, filters 22, switches in gate 21 and binary slicers are also increased in number.

35 WHAT WE CLAIM IS:—

1. Apparatus for establishing optimum settings for the multipliers in a transversal equaliser from a message data sequence received from a distorting transmission medium, comprising means for repeatedly determining error signals as the difference between time-spaced analog samples and standardised estimates of the data sequence in message signals received by said equaliser, means for repeatedly multiplying said error signals and a plurality of standardised estimates of the data sequence occurring with, before and after said error signals, means for separately integrating repeated products from said multiplying means for the duration of a predetermined plurality of successive error signals to obtain estimates of individual time-spaced interference components of the impulse response of said transmission channel, and means responsive to periodic polarity samples of the estimates of interference components in said integrating means for adjusting step-by-step said attenuators in a direction so as to reduce said interference components over a period of time.

2. A transversal equaliser for receiving from a distorting transmission medium polarity determinant binary data signals

applied at a fixed transmission rate, comprising a transversal filter having at least a delay line portion with output taps at intervals compatible with said transmission rate, an incrementally adjustable attenuator connected to each such output tap and a summing circuit for combining the attenuated outputs of all such taps, means for obtaining samples of the analog output of said summing circuit at said fixed transmission rate, means for providing pulses at standardised amplitudes as quantized estimates of the polarity of samples of the analog output of said summing circuit, means for subtracting said quantized estimates from said analog samples as interference error signals, means for multiplying each individual error signal by a plurality of said quantized estimates including effective past, present and future estimates, means for averaging a preselected plurality of corresponding successions of products from said multiplying means as estimates of individual components of the impulse response of said transmission medium, means for detecting the polarity of averages from said averaging means at preselected multiples of said transmission rate, and means responsive to the detected polarities of said averages for incrementally changing the settings of said attenuators so as to reduce present distortion.

3. An equaliser according to claim 2, wherein included in the means for detecting is means for periodically slicing the outputs of the means for averaging in accordance with the polarity thereof.

4. An equaliser according to claim 2 or 3, comprising means for continuously storing a plurality of successive estimated data symbols from said detecting means, means for delaying by a fixed number of periods the samples from said sample-taking means to enable effective correlation of each error signal from said subtracting means with a plurality of successive data symbols, including symbols coincident with, and occurring before and after each said error signal, and included in the means for multiplying are a plurality of product-taking means for multiplying each error sample by plus or minus one according to the polarity of the data symbol in said storing means.

5. An equaliser according to claim 4, wherein included in the storing means is a shift register having a plurality of stages for storing said successive estimated data symbols, and comprising a plurality of polarity inverters connected in common to said delaying means and individually to a stage of said shift register, the contents of the shift register stage determining whether the common input signal is effectively multiplied by plus or minus one.



6. An equaliser according to any one of claims 2 to 5, wherein included in the means for averaging are low-pass filters.

5 7. A transversal equaliser substantially as herein described with reference to and as shown in the accompanying drawing.

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