CLAIMS

What is claimed is:

1. A chip package comprising:

an electronic chip having a plurality of die pads formed on a top surface thereof;

a polyimide flex layer positioned on the electronic chip, the polyimide flex layer having a plurality of vias formed therein such that each of the plurality of vias corresponds to a respective die pad;

an adhesive layer deposited between the electronic chip and the polyimide flex layer; and

a plurality of metal interconnects formed on the polyimide flex layer, each of the plurality of metal interconnects comprising:

a cover pad covering a portion of a top surface of the polyimide flex layer;

a sidewall extending down from the cover pad and through the via along a perimeter thereof; and

a base connected to the sidewall and forming an electrical connection with a respective die pad;

wherein a thickness of each of the base and the sidewall is equal to or greater than a thickness of the adhesive layer.

2. The chip package of claim 1 wherein a thickness of each of the base and the sidewall is such that a volume of a respective via is filled by the metal interconnect.

3. The chip package of claim 2 wherein the metal interconnect comprises a post interconnect.

4. The chip package of claim 1 wherein the polyimide flex layer comprises a free-standing film configured to support the electronic chip.

5. The chip package of claim 1 wherein a composition of the adhesive layer comprises an epoxy-based dielectric material, an epoxy resin, a photoacid generator, an antioxidant, and a cold catalyst corresponding to the photoacid generator.

6. The chip package of claim 1 wherein the thickness of the adhesive layer is in the range of 12 to 25 micrometers.

7. The chip package of claim 1 wherein a diameter of each of the plurality of vias is less than 45 micrometers.

8. The chip package of claim 7 wherein a thickness of the cover pad is greater than a thickness of the base and the sidewall.

9. A method of forming a chip package comprising:

providing a silicon wafer having an integrated circuit (IC) thereon and a plurality of die pads formed on a top surface thereof;

applying an adhesive layer to the top surface of the silicon wafer;

adhering the silicon wafer to a free-standing polyimide flex layer by way of the adhesive layer;

forming a plurality of vias through the free-standing polyimide flex layer and the adhesive layer, each of the plurality of vias extending to a respective one of the plurality of die pads; and

forming a plurality of metal interconnects on the free-standing polyimide flex layer such that each of the plurality of metal interconnects extends through a respective via to electrically connect to a respective die pad, wherein forming the plurality of metal interconnects comprises:

determining a desired metal interconnect thickness based on a thickness of the adhesive layer;

depositing a metal material on the free-standing polyimide flex layer and in the plurality of vias having the desired metal interconnect thickness; and

patterning and etching the metal material to form the plurality of metal interconnects having the desired thickness.

10. The method of claim 9 wherein depositing, patterning, and etching each of the plurality of metal interconnects comprises:

forming a cover pad covering a portion of a top surface of the free-standing polyimide flex layer;

forming a sidewall extending down from the cover pad and through a respective via along a perimeter thereof; and

forming a base connected to the sidewall and forming an electrical connection with a respective die pad;

wherein the sidewall and the base are formed to have the determined desired thickness.

11. The method of claim 10 wherein forming the sidewall and the base to have the determined desired thickness comprises forming the sidewall and the base to have a thickness equal to or greater than a thickness of the adhesive layer.

12. The method of claim 10 wherein forming the sidewall and the base to have the determined desired thickness comprises forming the sidewall and the base such that a respective via is completely filled with the metal material.

13. The method of claim 10 wherein forming the cover pad comprises forming a cover pad having a thickness greater than the thickness of the sidewall and base.

14. The method of claim 9 wherein adhering the silicon wafer to the free-standing polyimide flex layer comprises adhering the silicon wafer to the free-standing polyimide flex layer in a face-down orientation.

15. The method of claim 9 wherein applying the adhesive layer comprises applying an adhesive layer having a composition of an epoxy-based dielectric material, an epoxy resin, a photoacid generator, an antioxidant, and a cold catalyst corresponding to the photoacid generator.

16. The method of claim 9 wherein depositing the metal material comprises electroplating the metal material on the free-standing polyimide flex layer and in the plurality of vias.

17. A chip package comprising:

a silicon wafer having a plurality of die pads formed on a top surface thereof;

an adhesive layer deposited on the silicon wafer;

a free-standing dielectric layer affixed to the adhesive layer and having a plurality of vias formed therethrough each extending through the adhesive layer to a respective one of the plurality of die pads; and

a plurality of metal interconnects formed on the free-standing polyimide flex film such that each of the plurality of metal interconnects extends through a respective via to form an electrical connection with a respective die pad, each of the plurality of metal interconnects comprising:

a cover pad covering a portion of a top surface of the free-standing polyimide flex film;

a base forming an electrical connection with a respective die pad; and

a sidewall extending between the cover pad and the base along a perimeter of the via;

wherein each of the base and the sidewall is constructed to have a thickness equal to or greater than a thickness of the adhesive layer.

18. The chip package of claim 17 wherein each of the base and the sidewall is constructed to have a thickness such that a volume of a respective via is filled by the metal interconnect.

19. The chip package of claim 18 wherein the metal interconnect comprises a post interconnect.

20. The chip package of claim 19 wherein the thickness of the adhesive layer is in the range of 12 to 25 micrometers.

CLAIMS

1. A chip package (20) comprising:

an electronic chip (10) having a plurality of die pads (14) formed on a top surface thereof;

a polyimide flex layer (22) positioned on the electronic chip (10), the polyimide flex layer (22) having a plurality of vias (24) formed therein such that each of the plurality of vias (24) corresponds to a respective die pad (14);

an adhesive layer (23) deposited between the electronic chip (10) and the polyimide flex layer (22); and

a plurality of metal interconnects (28) formed on the polyimide flex layer (22), each of the plurality of metal interconnects (28) comprising:

a cover pad (31) covering a portion of a top surface (30) of the polyimide flex layer (22);

a sidewall (36) extending down from the cover pad (31) and through the via (24) along a perimeter thereof; and

a base (34) connected to the sidewall (36) and forming an electrical connection with a respective die pad (14);

characterized in that a thickness of each of the base and the sidewall is equal to or greater than a thickness of the adhesive layer (23) so that the metal interconnects (28) are resistant to metal fatigue and cracking that may occur based on stresses imparted thereon from a CTE mismatch between the metal forming the metal interconnects (28) and the surrounding materials forming the polyimide flex layer (22) and the adhesive (23).

2. The chip package (20) of claim 1 wherein a thickness of each of the base (34) and the sidewall (36) is such that a volume of a respective via (24) is filled by the metal interconnect (28)

3. The chip package (20) of any preceding claim wherein the metal interconnect (28) comprises a post interconnect (38).

4. The chip package (20) of any preceding claim wherein the polyimide flex layer (22) comprises a free-standing film configured to support the electronic chip (10).

5. The chip package (20) of any preceding claim wherein a composition of the adhesive layer (23) comprises an epoxy-based dielectric material, an epoxy resin, a photoacid generator, an antioxidant, and a cold catalyst corresponding to the photoacid generator.

6. The chip package (20) of any preceding claim wherein the thickness of the adhesive layer (23) is in the range of 12 to 25 micrometers.

7. The chip package (20) of any preceding claim wherein a diameter of each of the plurality of vias (24) is less than 45 micrometers.

8. The chip package (20) of any preceding claim wherein a thickness of the cover pad (31) is greater than a thickness of the base (34) and the sidewall (36).

9. The chip package (20) of any preceding claim wherein the electronic chip (10) is adhered to the polyimide flex layer (22) in a face-down orientation by way of the adhesive layer (23).