CLAIMS

Claimed:

1. A microelectronic package comprising:

an active microelectronic device in contact with a package body; and

a passive microelectronic device disposed within a cavity formed in the package body;

wherein the active microelectronic device and the passive microelectronic device are electrically connected by conductive routes formed in or on the package body.

2. The microelectronic package of claim 1, wherein the cavity extends through the package body from a first surface of the package body to a second surface of the package body.

3. The microelectronic package of claim 1 or claim 2, wherein the active microelectronic device comprises a flip-chip microelectronic device and the package body comprises a microelectronic substrate, wherein the flip-chip microelectronic device is in contact with the microelectronic substrate through a plurality of interconnects extending therebetween.

4. The microelectronic package of claim 1 or claim 2, wherein the active microelectronic device is embedded in the package body and wherein an active surface of the active microelectronic device is substantially planar to a second surface of the package body.

5. The microelectronic package of claim 4, wherein the conductive routes are formed in a redistribution layer formed on the active microelectronic device active surface and the package body second surface.

6. The microelectronic package of claim 1, wherein the package body comprises a support plate and a dielectric encapsulant, wherein a back surface of the active microelectronic device is adhered to the support plate and wherein the active microelectronic device is embedded in the dielectric encapsulant with a portion of the dielectric encapsulant extends over the active microelectronic device active surface.

7. The microelectronic package of claim 6, wherein the conductive routes are formed in a redistribution layer formed on the package body second surface.

8. The microelectronic package of claim 7, wherein the cavity extends through the redistribution layer, through the dielectric encapsulant, and partially into the support plate.

9. A method of fabricating a microelectronic package comprising:

forming an active microelectronic device;

forming a package body;

contacting the package body with the active microelectronic device;

forming conductive routes in or on the package body;

forming a cavity in the package body;

disposing a passive microelectronic device within the cavity; and

electrically connecting the active microelectronic device and the passive microelectronic device with the conductive routes.

10. The method of claim 9, wherein the forming the cavity in the package body comprises forming the cavity to extend through the package body from a first surface of the package body to a second surface of the package body.

11. The method of claim 9 or claim 10, wherein the forming the microelectronic device comprises forming a flip-chip microelectronic device, wherein forming the package body comprises forming a microelectronic substrate, and wherein the microelectronic device is in contact with the microelectronic substrate through a plurality of interconnects extending between the flip-chip microelectronic device and the microelectronic substrate.

12. The method of claim 9 or claim 10, wherein forming the package body and contacting the package body with the active microelectronic device comprises embedding the microelectronic device in the package body such that an active surface of the microelectronic device is substantially planar to a second surface of the package body.

13. The method of claim 12, wherein forming conductive routes in or on the package body comprises forming in a redistribution layer formed on the microelectronic device active surface and the package body second surface.

14. The method of claim 9, wherein forming the package body comprises forming a support plate and forming a dielectric encapsulant, wherein a back surface of the active microelectronic device is adhered to the support plate and wherein the active microelectronic device is embedded in the dielectric encapsulant with a portion of the dielectric encapsulant extending over the active microelectronic device active surface.

15. The method of claim 14, wherein forming conductive routes in or on the package body comprises forming conductive routes in a redistribution layer formed on the package body second surface.

16. The method of claim 15, wherein the forming the cavity in the package body comprises forming the cavity to extend through the redistribution layer, through the dielectric encapsulant, and partially into the support plate.

17. A computing device, comprising:

a board; and

a microelectronic package attached to the board, wherein the microelectronic package comprises:

an active microelectronic device in contact with a package body; and

a passive microelectronic device disposed within a cavity formed in the package body;

wherein the active microelectronic device and the passive microelectronic device are electrically connected by conductive routes formed in or on the package body.

18. The computing device of claim 17, wherein the cavity extends through the package body from a first surface of the package body to a second surface of the package body.

19. The computing device of claim 17 or claim 18, wherein the active microelectronic device comprises a flip-chip microelectronic device and the package body comprises a microelectronic substrate, wherein the flip-chip microelectronic device is in contact with the microelectronic substrate through a plurality of interconnects extending therebetween.

20. The computing device of claim 17 or claim 18, wherein the active microelectronic device is embedded in the package body and wherein an active surface of the active microelectronic device is substantially planar to a second surface of the package body.

21. The computing device of claim 20, wherein the conductive routes are formed in a redistribution layer formed on the active microelectronic device active surface and the package body second surface.

22. The computing device of claim 17, wherein the package body comprises a support plate and a dielectric encapsulant, wherein a back surface of the active microelectronic device is adhered to the support plate and wherein the active microelectronic device is embedded in the dielectric encapsulant with a portion of the dielectric encapsulant extends over the active microelectronic device active surface.

23. The computing device of claim 22, wherein the conductive routes are formed in a redistribution layer formed on the package body second surface.

24. The computing device of claim 23, wherein the cavity extends through the redistribution layer, through the dielectric encapsulant, and partially into the support plate.

CLAIMS

Claimed:

1. A microelectronic package comprising:

an active microelectronic device in contact with a package body; and

a passive microelectronic device disposed within a cavity formed in the package body;

wherein the active microelectronic device and the passive microelectronic device are electrically connected by conductive routes formed in or on the package body.

2. The microelectronic package of claim 1, wherein the cavity extends through the package body from a first surface of the package body to a second surface of the package body.

3. The microelectronic package of claim 1, wherein the active microelectronic device comprises a flip-chip microelectronic device and the package body comprises a microelectronic substrate, wherein the flip-chip microelectronic device is in contact with the microelectronic substrate through a plurality of interconnects extending therebetween.

4. The microelectronic package of claim 1, wherein the active microelectronic device is embedded in the package body and wherein an active surface of the active microelectronic device is substantially planar to a second surface of the package body.

5. The microelectronic package of claim 4, wherein the conductive routes are formed in a redistribution layer formed on the active microelectronic device active surface and the package body second surface.

6. The microelectronic package of claim 1, wherein the package body comprises a support plate and a dielectric encapsulant, wherein a back surface of the active microelectronic device is adhered to the support plate and wherein the active microelectronic device is embedded in the dielectric encapsulant with a portion of the dielectric encapsulant extends over the active microelectronic device active surface.

7. The microelectronic package of claim 6, wherein the conductive routes are formed in a redistribution layer formed on the package body second surface.

8. The microelectronic package of claim 7, wherein the cavity extends through the redistribution layer, through the dielectric encapsulant, and partially into the support plate.

9. A method of fabricating a microelectronic package comprising:

forming an active microelectronic device;

forming a package body;

contacting the package body with the active microelectronic device;

forming conductive routes in or on the package body;

forming a cavity in the package body;

disposing a passive microelectronic device within the cavity; and

electrically connecting the active microelectronic device and the passive microelectronic device with the conductive routes.

10. The method of claim 9, wherein the forming the cavity in the package body comprises forming the cavity to extend through the package body from a first surface of the package body to a second surface of the package body.

11. The method of claim 9, wherein the forming the microelectronic device comprises forming a flip-chip microelectronic device, wherein forming the package body comprises forming a microelectronic substrate, and wherein the microelectronic device is in contact with the microelectronic substrate through a plurality of interconnects extending between the flip-chip microelectronic device and the microelectronic substrate.

12. The method of claim 9, wherein forming the package body and contacting the package body with the active microelectronic device comprises embedding the microelectronic device in the package body such that an active surface of the microelectronic device is substantially planar to a second surface of the package body.

13. The method of claim 12, wherein forming conductive routes in or on the package body comprises forming in a redistribution layer formed on the microelectronic device active surface and the package body second surface.

14. The method of claim 9, wherein forming the package body comprises forming a support plate and forming a dielectric encapsulant, wherein a back surface of the active microelectronic device is adhered to the support plate and wherein the active microelectronic device is embedded in the dielectric encapsulant with a portion of the dielectric encapsulant extending over the active microelectronic device active surface.

15. The method of claim 14, wherein forming conductive routes in or on the package body comprises forming conductive routes in a redistribution layer formed on the package body second surface.

16. The method of claim 15, wherein the forming the cavity in the package body comprises forming the cavity to extend through the redistribution layer, through the dielectric encapsulant, and partially into the support plate.

17. A computing device, comprising:

a board; and

a microelectronic package attached to the board, wherein the microelectronic package comprises:

an active microelectronic device in contact with a package body; and

a passive microelectronic device disposed within a cavity formed in the package body;

wherein the active microelectronic device and the passive microelectronic device are electrically connected by conductive routes formed in or on the package body.

18. The computing device of claim 17, wherein the cavity extends through the package body from a first surface of the package body to a second surface of the package body.

19. The computing device of claim 17, wherein the active microelectronic device comprises a flip-chip microelectronic device and the package body comprises a microelectronic substrate, wherein the flip-chip microelectronic device is in contact with the microelectronic substrate through a plurality of interconnects extending therebetween.

20. The computing device of claim 17, wherein the active microelectronic device is embedded in the package body and wherein an active surface of the active microelectronic device is substantially planar to a second surface of the package body.

21. The computing device of claim 20, wherein the conductive routes are formed in a redistribution layer formed on the active microelectronic device active surface and the package body second surface.

22. The computing device of claim 17, wherein the package body comprises a support plate and a dielectric encapsulant, wherein a back surface of the active microelectronic device is adhered to the support plate and wherein the active microelectronic device is embedded in the

dielectric encapsulant with a portion of the dielectric encapsulant extends over the active microelectronic device active surface.

23. The computing device of claim 22, wherein the conductive routes are formed in a redistribution layer formed on the package body second surface.

24. The computing device of claim 23, wherein the cavity extends through the redistribution layer, through the dielectric encapsulant, and partially into the support plate.