

- 1 -

Printer with a universal interface

The invention relates to a printer with a universal interface, with a processor which can be connected to a storage medium as well as to data input and data output connections for external devices.

GB 2 211 971 A discloses a printer of this generic type. The processor that controls the entire printing mechanism is connected, via a bus, to an input-output port, a read-only memory (ROM) and a variable memory (RAM). The motors for the printing mechanism and the print head are connected to the input-output port, as is also an interface for an external device, such as a computer and - separately - a ROM for fonts.

With a configuration of this kind, it should be apparent that disadvantages follow from the fact that the simple printer interface offers only very limited possibilities as regards the input and output of data. In particular, it is impossible to connect external storage media to the interface, examples of such media being electronic memory boards. Memory boards of this type can contain data which render the printer capable of printing with different fonts, and in the case of the prior-art printer these boards have to be plugged into the sockets that are provided specifically for this purpose.

The problem to which the present invention is addressed is to upgrade the capabilities of printers as regards the input and output of data, to the effect that data from external storage media, e.g. memory boards, can also be read into the printer and output to the storage medium.

This problem is solved, according to the invention, by means of a common interface which is activated by the processor, and to which it is possible to connect both the storage medium and the data input and data output connections for external devices.

The essential idea is to equip the printer with a universal interface, to which it is possible to connect both storage media and circuit boards with data input and data output connections for external devices. For example, the use of memory boards enables the memory capacity of the printer to be extended, or enables different fonts to be reproduced from data which are permanently stored in a ROM. A graphics board enables the image that is to be output as hard copy to be inspected on a VDU before it is printed-out onto the print medium, so as to allow any possible faults to be detected by eye, and thus to be corrected. Lastly, the universal interface can serve as a means of connecting whatever input-output boards may be desired. In addition, such extra boards can be employed as means - as a rule provided as standard - of connecting data sources, e.g. computers, which are not connected via the interface, but are instead connected to the processor via some other location.

The advantages of the invention reside principally in the universal, all-purpose upgradeability of the printer, by reason of the fact that any desired plug-in board can

be used, selected from the range already commercially available at reasonable prices.

As a general rule, such boards have a write signal wire and a read signal wire for data input and data output connections for external devices, as well as a write signal wire and a read signal wire for storage media, so the printer interface is obviously equipped with such wires as well.

Should especially fast, so-called RISC printer processors (e.g. AMD 29200) be employed in order to achieve higher printer speeds, with an instruction set that is shorter than the set for conventional processors, the use of a multiplexer proves necessary by reason of the fact that these especially fast printer processors have only a read signal wire and a write signal wire, and do not therefore have an output connection for distinguishing between external storage media and devices of other types. The multiplexer recognizes the type of activating device from the output signal from an address decoder which is logically connected to the address bus associated with the processor, and controls the four wires of the interface in a corresponding manner (the write signal wire and the read signal wire for data input and data output connections for external devices, and the write signal wire and the read signal wire for storage media). Through the agency of the address decoder and multiplexer, the processor can, by referring to its address bus, thus switch over between the different types of external device.

In order to be able to use plug-in boards with databuses of different widths, it is further proposed that the circuit configuration should be such that the processor

can switch over from one databus width to another. It is thus possible, e.g., to employ 8-bit or 16-bit plug-in boards. In practice, the switching-over can be hardware-implemented through the agency of a buffer that is inserted into the bidirectional databus associated with the processor, this buffer being controlled by a separate output from the processor, and being capable of stopping the transmission of the high-order bits on the databus (i.e. capable of switching said databus to the high-impedance condition).

Lastly, it is recommended that the interface should be equipped with a separate baud rate generator, as a clock generator, in order to be able to operate the processor at any desired clock frequency, and especially at a frequency higher than that of its own clock generator.

In what follows, an illustrative embodiment of the invention is explained in greater detail by reference to the drawing, which is a schematic diagram of a data input and data output circuit associated with a printer.

In its basic constructional configuration, the circuit comprises a processor (1) which on the one hand controls the actual printing mechanism (25), and which, on the other hand, is supplied with the data to be printed, these being input to it via an address bus (11) and a databus (12), and said circuit further comprises an interface (20), to which different plug-in boards with storage media (26, 27) and data input and output connections (28) for external devices are connected.

The printing mechanism (25) includes the mechanical and electronic elements which are necessary for accomplishing printing, and thus comprises, as a rule, at least one

print head and a motor for feeding the print medium, which can, e.g., be paper, or labels affixed to a backing strip. The printing mechanism (25) is not detailed in the drawing, since it is adequately well known to persons with relevant technical knowledge. If the printer is of the thermal type, the processor (1) also controls the heating elements associated with the thermal print head.

The timing of the processor (1) is defined by a clock generator (5). The operator can control the processor (1), and hence the printer, by means of a data entry device (24) which can be configured as a keyboard and/or as an operator control panel.

The decisive innovation associated with the invention resides in the use, in a printer, of the interface (20) to which different plug-in boards can be connected, each via a bus (29 - 31). The interface (20) enables known and commercially available boards, of the undermentioned types, to be connected to the processor (1): boards with storage media (26, 27), boards with data input and data output connections (28) for external devices (I/O boards such as Centronics interfaces, RS 232 and RS 485 interfaces, network interfaces (Ethernet), coaxial or twinax interfaces) and graphics boards. It would of course be possible to connect more plug-in boards than the three that are shown connected to the interface (20) in the drawing.

The address bus (11) associated with the processor (1) is connected, via a unidirectionally operating section of a buffer (10), to the address bus (13) associated with the interface (20), while the databus (12) associated with the processor (1) is connected to the interface (20) by means of a bidirectional section of the buffer (10)

and an additional buffer (16) which can be caused to switch over. The address of a storage or memory device, read out by the processor (1), is consequently transmitted to the interface (20) via the unidirectional section of the buffer (10); it is obviously unnecessary to transmit an address in the opposite direction.

Data, on the other hand, can be transmitted in both directions (to and from the processor (1)), so that, e.g., it is possible to write data onto a memory board and to read data therefrom. On that side of the buffer (10) opposite the processor (1), the databus (12) associated therewith is split into two equal halves (each as a rule accommodating 8 bits), which are each transmitted on a separate bus (14, 15) in order to be able to vary the data word width by means of the switchable buffer (16), also operating bidirectionally. The switchable buffer (16), controlled by the processor (1) via the wire (17), either enables the databuses (18, 19) connected to the interface (20) to 'loop through' onto the databuses (14, 15) connected to the buffer (10), in order to transmit the width of the databus (and therefore, as a rule, 16 bits), or else provides the possibility of 'looping through' only the bits on the low-order databuses (15, 19), and of switching off the high-order databuses (14, 18), i.e. isolating them from each other in order to enable plug-in boards (26 - 28) with narrower databuses to be used on the interface (20). The information present on the wire (17) consequently corresponds to a control signal which switches the high-order bits on and off.

By reason of the fact that an RISC-type processor (1) is used, which is relatively fast and has only two outgoing control wires (2, 3), the use of a multiplexer (4) proves

necessary in order to activate the interface (20).

In the drawing, the read signal wire (2) of the processor (1) is marked RD ('read'), while the write signal wire is marked WR ('write'). If the processor (1) is reading-in data, a logic '1' is present on the read signal wire (2), while on the other hand a '1' will be present on the write signal wire (3) as soon as the processor (1) transmits data to the interface (20). In its turn, however, the interface has four signal wires (6 - 9), of which one can be set to '1' at any one time. If the processor (1) is transmitting data to an external device via the interface, the write signal wire (6), marked I/O WR, has to be set to '1', whereas if the processor (1) is reading-in data from an external device via the interface, the read signal wire, marked I/O RD, must be set to '1'. Analogously, if it is desired to write data onto a memory board connected to the interface (20), the write signal wire (8) for external storage media is set to '1'.

Lastly, the read signal wire MEMRD (9) for external memory boards assumes the '1' condition as soon as the processor (1) intends to read out data from an external memory board. In order to be able to operate the fast processor (1) with the interface, the processor activates the address decoder (21) via the address bus (11), and said address decoder recognizes, from the address present on said bus, whether, on the one hand, the processor (1) is performing an input or output operation involving a peripheral device or, on the other hand, is writing data onto or reading-out data from a storage location associated with an external storage medium. The multiplexer (4) controls the four signal wires (6 - 9) connected to the interface (20), by referring to the signal at the output (22) of the address decoder (21) and also to the signals on the read and write signal wires (2, 3)

associated with the processor (1). If the read signal wire (2) of the processor (1) is in the '1' condition, and if it can be recognized, by referring to the signal at the output (22) of the address decoder (21), that a storage operation is being performed, the multiplexer (4) sets only the MEMRD read signal wire (9) for external storage media to '1'. If the processor (1) intends to read out data from an external device, the output of the address decoder (21) changes over to the complementary logic condition, and only the I/O RD signal wire (7) is set to '1'. Correspondingly - depending on the signal at the output (22) of the address decoder (21) - the I/O WR signal wire (6) or, as the case may be, the MEMWR signal wire (8) is set to '1' if the write signal wire (3) associated with the processor (1) is in the '1' condition. It remains to be pointed out that instead of the respective read or, as the case may be, write signals being present on the wires (2, 3, 6 - 9), it is also possible for the logical complements of these signals to be present on these wires.

In addition, the interface (20) has a separate clock generator, in the form of the baud rate generator (23).

The outcome is the production of a printer which features universal, all-purpose usability, and a high operating speed that results from the use of a fast processor.



Patent Claims

1. Printer with a universal interface, with a processor (1) which can be connected to a storage medium (26, 27) as well as to data input and data output connections (28) for external devices, characterized by a common interface (20) which is activated by the processor (1), and to which it is possible to connect both the storage medium (26, 27) and the data input and data output connections (28) for external devices.
2. Printer according to Claim 1, characterized in that the interface (20) has a write signal wire (6) and a read signal wire (7) for data input and data output connections (28) for external devices, as well as a write signal wire (8) and a read signal wire (9) for storage media (26, 27).
3. Printer according to Claim 2, characterized by a multiplexer (4) which controls the write signal and read signal wires (6 - 9) of the interface (20) by referring to the signal on a read signal wire (2), the signal on a write signal wire (3) and the address bus (11) associated with the processor (1).
4. Printer according to Claim 3, characterized by an address decoder (21) which controls the multiplexer (4) by referring to the address bus (11) associated with the processor (1).



- 10 -

5. Printer according to any one of Claims 1 to 4, characterized in that the processor (1) can switch over from one width of the databus (18, 19) to another, said databus being the one associated with the interface (20).
6. Printer according to any one of Claims 1 to 5, characterized by a baud rate generator (23) which serves as a clock generator associated with the interface (20), the processor (1) having a clock generator (5) of its own.
7. Printer according to any one of Claims 1 to 6, characterized in that the processor (1) controls a printing mechanism (25).
8. Printer according to any one of Claims 1 to 7, characterized in that it is a thermal printer which is capable of printing onto label strips.
9. Printer according to any one of Claims 1 to 8, characterized by a graphics card which can be connected to the interface (20).
10. Printer according to any one of Claims 1 to 9, characterized in that the processor (1) is an RISC processor.