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(54) Title: COLUMN IV TRANSISTORS FOR PMOS INTEGRATION

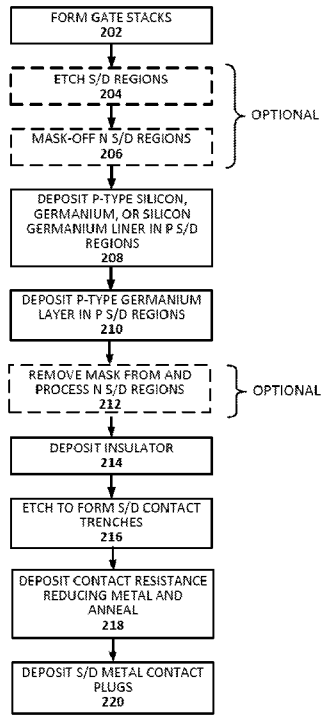


FIG. 2

(57) Abstract: Techniques are disclosed for forming column IV transistor devices having source/drain regions with high concentrations of germanium, and exhibit reduced parasitic resistance relative to conventional devices. In some example embodiments, the source/drain regions each includes a thin p-type silicon or germanium or SiGe deposition with the remainder of the source/drain material deposition being p-type germanium or a germanium alloy (e.g., germanium:tin or other suitable strain inducer, and having a germanium content of at least 80 atomic % and 20 atomic % or less other components). In some cases, evidence of strain relaxation may be observed in the germanium rich cap layer, including misfit dislocations and/or threading dislocations and/or twins. Numerous transistor configurations can be used, including both planar and non-planar transistor structures (e.g., FinFETs and nanowire transistors), as well as strained and unstrained channel structures.

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