Claims

1. A method to process an Integrated Circuit device comprising:

processing a first layer of first transistors, then

processing a first metal layer overlaying said first transistors and providing at least one connection to said first transistors, then

processing a second metal layer overlaying said first metal layer, then

processing a second layer of second transistors overlaying said second metal layer, wherein

said second metal layer is connected to provide power to at least one of said second transistors.

2. A method to process an Integrated Circuit device comprising:

processing a first layer of first transistors, then

processing a first metal layer overlaying said first transistors and providing at least one connection to said first transistors, then

processing a second metal layer overlaying said first metal layer, then

processing a second layer of second transistors overlaying said second metal layer, comprising

forming at least one connection path between said second transistors and said second metal layer, wherein

said connection path comprises at least one through-layer via, and wherein said through-layer via comprises material whose co-efficient of thermal expansion is within 50 percent of a coefficient of thermal expansion of said second layer.

3. A method to process an Integrated Circuit device comprising:

processing a first layer of first transistors, then

processing a first metal layer overlaying said first transistors and providing at least one connection to said first transistors, then

processing a second metal layer overlaying said first metal layer, then

processing a second layer of second transistors overlaying said second metal layer, then

processing a third metal layer overlying said second transistors,

wherein at least one of said second transistors is one of:

(i) a replacement-gate transistor;

(ii) a Finfet transistor; or

(iii) a double gate horizontally oriented transistor.

4. A 3D semiconductor device, the device comprising:

a first level comprising a first single crystal layer and first transistors,

wherein said first transistors each comprise a single crystal channel;

first metal layers interconnecting at least said first transistors; and

a second level comprising a second single crystal layer and second transistors,

wherein said second level overlays said first level,

wherein said second transistors are horizontally oriented and each comprise at least two side gates, and

wherein said second level is bonded to said first level.

5. A 3D semiconductor device, the device comprising:

a first level comprising a first single crystal layer and first transistors,

wherein said first transistors each comprise a single crystal channel;

first metal layers interconnecting at least said first transistors;

alignment marks,

wherein said first level comprises said alignment marks; and

a second level comprising a second single crystal layer and second transistors,

wherein said second level overlays said first level,

wherein said second transistors are horizontally oriented and each comprise at least two side gates,

wherein said second level is bonded to said first level,

wherein said bonded comprises oxide to oxide bonds, and

wherein said second transistors are aligned to said alignment marks.

6. A semiconductor device, the device comprising:

a plurality of transistors,

wherein at least one of said plurality of transistors comprises a first single crystal source, channel, and drain,

wherein at least one of said plurality of transistors comprises a second single crystal source, channel, and drain,

wherein said second single crystal source, channel, and drain is disposed above said first single crystal source, channel, and drain,

wherein at least one of said plurality of transistors comprises a third single crystal source, channel, and drain,

wherein said third single crystal source, channel, and drain is disposed above said second single crystal source, channel, and drain,

wherein at least one of said plurality of transistors comprises a fourth single crystal source, channel, and drain, and

wherein said fourth single crystal source, channel, and drain is disposed above said third single crystal source, channel, and drain; and

an ohmic connection between said first single crystal source or drain and said second single crystal source or drain.

7. A semiconductor device, the device comprising:

a plurality of transistors,

wherein at least one of said plurality of transistors comprises a first single crystal source, channel, and drain,

wherein at least one of said plurality of transistors comprises a second single crystal source, channel, and drain,

wherein said second single crystal source, channel, and drain is disposed above said first single crystal source, channel, and drain,

wherein at least one of said plurality of transistors comprises a third single crystal source, channel, and drain,

wherein said third single crystal source, channel, and drain is disposed above said second single crystal source, channel, and drain,

wherein at least one of said plurality of transistors comprises a fourth single crystal source, channel, and drain, and

wherein said first single crystal source or drain, and said second single crystal source or drain each comprise n+ doped regions.

8. A semiconductor device, the device comprising:

a plurality of transistors,

wherein at least one of said plurality of transistors comprises a first single crystal channel,

wherein at least one of said plurality of transistors comprises a second single crystal channel,

wherein said second single crystal channel is disposed above said first single crystal channel,

wherein at least one of said plurality of transistors comprises a third single crystal channel,

wherein said third single crystal channel is disposed above said second single crystal channel,

wherein at least one of said plurality of transistors comprises a fourth single crystal channel,

wherein said fourth single crystal channel is disposed above said third single crystal channel, and

wherein formation of said fourth single crystal channel comprises a layer transfer process.

9. A semiconductor device, the device comprising:

a plurality of transistors,

wherein at least one of said plurality of transistors comprises a first single crystal source, channel, and drain,

wherein at least one of said plurality of transistors comprises a second single crystal source, channel, and drain,

wherein said second single crystal source, channel, and drain is disposed above said first single crystal source, channel, and drain,

wherein at least one of said plurality of transistors comprises a third single crystal source, channel, and drain,

wherein said third single crystal source, channel, and drain is disposed above said second single crystal source, channel, and drain,

wherein at least one of said plurality of transistors comprises a fourth single crystal source, channel, and drain, and

wherein said fourth single crystal source, channel, and drain is disposed above said third single crystal source, channel, and drain; and

wherein at least one of said plurality of transistors comprises two side gates.

10. A semiconductor device, the device comprising:

a plurality of transistors,

wherein at least one of said plurality of transistors comprises a first single crystal channel,

wherein at least one of said plurality of transistors comprises a second single crystal channel,

wherein said second single crystal channel is disposed above said first single crystal channel,

wherein at least one of said plurality of transistors comprises a third single crystal channel,

wherein said third single crystal channel is disposed above said second single crystal channel,

wherein at least one of said plurality of transistors comprises a fourth single crystal channel,

wherein said fourth single crystal channel is disposed above said third single crystal channel,

wherein said least one of said plurality of transistors is a horizontally oriented transistor, and

wherein formation of said fourth single crystal channel comprises a layer transfer process.

11. A semiconductor device, the semiconductor device comprising:

a first silicon level comprising a first single crystal silicon layer and a plurality of first transistors;

a first metal layer disposed over said first silicon level;

a second metal layer disposed over said first metal layer;

a third metal layer disposed over said second metal layer;

a second level comprising a plurality of second transistors, said second level disposed over said third metal layer;

a third level comprising a plurality of third transistors, said third level disposed over said second level;

a fourth metal layer disposed over said third level;

a fifth metal layer disposed over said fourth metal layer; and

a via disposed through said second level and through said third level as part of a connection path between said fourth metal layer to said second metal layer,

wherein each of said plurality of second transistors comprises a metal gate,

wherein at least one of said metal gates comprises tungsten,

wherein formation of said plurality of second transistors comprises a first lithography step, and

wherein formation of said plurality of third transistors comprises a second lithography step.

12. A method for producing a 3D semiconductor device, the method comprising:

providing a first level, said first level comprising a first single crystal layer;

forming memory control circuits in and/or on said first level.

wherein said memory control circuits comprise first single crystal transistors, and

wherein said memory control circuits comprise at least two interconnection metal layers;

forming at least one second level;

performing a first etch step into said at least one second level;

forming at least one third level;

performing additional processing steps to form a plurality of first memory cells within said second level and a plurality of second memory cells within said third level.

wherein each of said plurality of first memory cells comprise at least one second transistor.

wherein each of said plurality of second memory cells comprise at least one third transistor, and

wherein said at least one second transistor comprises a metal gate; and

performing bonding of said first level to said second level.

wherein said third level is disposed above said second level, and

wherein said first level comprises control of power delivery to said at least one third transistor.

13. A method for producing a 3D semiconductor device, the method comprising:

providing a first level. said first level comprising a first single crystal layer;

forming memory control circuits in and/or on said first level,

wherein said memory control circuits comprise first single crystal transistors, and

wherein said memory control circuits comprise at least two interconnection metal layers;

forming at least one second level disposed above or below said memory control circuits;

performing a first etch step into said at least one second level;

forming at least one third level disposed on top of said second level;

performing additional processing steps to form a plurality of first memory cells within said second level and a plurality of second memory cells within said third level,

wherein each of said plurality of first memory cells comprise at least one second transistor,

wherein each of said plurality of second memory cells comprise at least one

third transistor;

forming at least one via, said at least one via is disposed through said third level and through said second level, and connects to at least one of said at least two interconnection metal layers; and

a step of gate replacement of said at least one third transistor.