

REPLACED SHEETS SG
40022-7 2/85
☒ Description : paged ... to paged ...
☒ Claim(s) : paged ... to paged ...
☒ Drawing(s) : paged ... to paged ...
☒ Abstract : paged ... to paged ...
DATE OF RECEIPT

Method and device for monitoring an
alternating signal

5 The present invention relates to a method for monitoring an alternating signal in accordance with the precharacterizing clause of Claim 1 and a device in accordance with the precharacterizing clause of the first substantive claim.

10 The use of stages which output an alternating signal which is used for controlling a connected stage is generally known. Control stages of this type may contain, for example, a microprocessor which outputs an alternating signal in the form of a digital signal and thus controls a connected stage. Oscillators are also known
15 signal for processing further signals by means of corresponding stages.

Various possibilities are conceivable for a signal which is of the type output by a control stage of the said type, is alternating, also called changing
20 below, to change its course. Thus, for example, a potential shift may occur in that a DC voltage is superimposed upon the changing signal. It is furthermore possible that the pulse duty ratio of the changing signal changes. Depending on the device in which the control stage is
25 used and/or depending on the operating state, changes of this type can be intentional or can point to a fault in the control stage.

30 It is the object of the present invention to monitor the state of an alternating signal in a simple way.

This object is achieved by means of a method according to the main claim and by means of a device in accordance with the first substantive claim.

35 According to the invention, an alternating signal which is generated, for example, by a control stage or by an oscillator, is conditioned in such a way that, by means of comparing the conditioned signal with reference values, signals are generated which can be evaluated in a simple way.

This Sheet Has Been Replaced



The conditioning of the changing signal can be effected, for example, in that the latter is essentially smoothed. The value of the smoothed signal is a measure of a possible DC component and/or of the clock ratio of the changing signal.

Another possibility for conditioning is, for example, to route the changing signal via a capacitor which is connected in series between a first stage, which is generating the changing signal, and a second stage, which is controlled by this signal. In this arrangement, the first side of the capacitor, which is connected to the second stage, is charged by means of a voltage source, a current source or the like in such a way that, in the event of no change or only small changes in the potential at the second side, connected to the first stage, of the capacitor, the first side assumes specific voltage values in accordance with a prescribed time variation.

It should be pointed out that both the alternating signals which are used for control and the signals which are derived therefrom can be conditioned.

A variation in the pulse duty ratio and/or the DC component of the alternating signal can, for example, be used for controlling a connected stage or can also point to a functional disturbance. Thus, for example, in the case of a control stage of the type mentioned, an uncontrolled state may occur in which the output signal from the control stage corresponds to a DC voltage level, a positive operating voltage or earth potential. This can be caused, for example, by induction peaks or the like which influence the sequence of a control program which is being used for the functioning of the control stage. It is likewise conceivable that elements of the control stage become defective, that the supply voltage of the control stage fails, or the like.

In the cases mentioned, faulty functioning occurs of the stages connected to the control stage.

It is an advantage of the present invention that states of this type can be detected in a simple way and



a prescribed state of the connected stages can then be controlled.

Operational monitoring of this type can be used, for example, in the case of a device such as a video recorder which drives a tape on which information is stored and from which information can be read.

Further features, advantages and details of the invention are explained in the following exemplary embodiments, with reference to the drawing, in which:

Fig. 1: shows the block diagram of a first exemplary embodiment;

Fig. 2: shows variations of signals in the exemplary embodiment of Fig. 1

Fig. 3: shows the block diagram of a second exemplary embodiment;

Fig. 4: shows variations of signals in the exemplary embodiment of Fig. 3

Before the description of the exemplary embodiments is gone into in more detail, it should be pointed out that the blocks shown individually in the figures are merely used for improved understanding of the invention. Normally, individual blocks or a plurality of these blocks are combined into units. These blocks may be realized in integrated or hybrid technology or as program-controlled microcomputers, or as part of a program suitable for controlling it.

The elements contained in the individual stages can also be of separate design, however.

Fig. 1 shows an electronic control device 10, which routes control signals U_s via a conditioning stage, which in this exemplary embodiment is designed as a smoothing element 11, to a drive stage 12, which applies current to a motor 13. The smoothing element 11 comprises a resistor 11a, whose first terminal is connected to the output of the control device 10, and a capacitor 11b, which is connected between the second terminal of the resistor 11a and earth. The smoothing element 11 effects smoothing of the control signal U_s , as a result of which a signal U_i is formed. The latter is then fed to the



noninverting (+) inputs of a first comparator 14, a second comparator 15 and a third comparator 16. The comparators 14, 15, 16 are connected by their inverting (-) inputs to a first reference voltage $Ur1$, to a second reference voltage $Ur2$ and to a third reference voltage $Ur3$. The output signals $Ua1$ and $Ua3$ from the comparators 14, 16 are each fed to an input of an EXCLUSIVE-OR gate 17, whose output signal So is fed to further drive means which apply current to the motor 13. These further drive means, which inter alia contain an output stage, and means which evaluate the signal So and a signal Ss of a starting stage 19 and then drive the output stage as described below, are represented symbolically in Fig. 1 by the stage 18.

The output signal $Ua2$ from the comparator passes to the starting stage 19, whose output signal Ss is fed to the stage 18.

The functioning of the exemplary embodiment of Fig. 1 is explained below with the aid of Fig. 2 only to the extent that is necessary for understanding the present invention.

In order to start the motor 13 running, the control device 10 outputs the clocked control signal Us , which leads to a smoothed signal Ui , as is represented in Figures 2a and 2b in the interval between $t0$ and $t1$. The signal Ui has a residual ripple which, for the purposes of better understanding, is drawn somewhat exaggerated. The values of the reference voltages Ur are likewise drawn in Figure 2b. The comparators output signals Ua , as is shown in Figures 2c) to 2e).

Normal operation, such as is present during the interval between $t0$ and $t1$, will be considered first. On the basis of the signal Ui , the comparator 15 simulates the output signal $Ua2$ with a variation which corresponds to the clock rate of the original output signal Us , with a clock ratio t_b/t_1 during a period T . The signal $Ua1$ is "low", that is to say it assumes the digital value "0", and the signal $Ua2$ is "high", corresponding to the value "1". Hence, as can be seen from Fig. 2f, the output



signal S_0 of the EX-OR gate 17 is high, as a result of which the operation of the output stage containing the stage 18 is not impaired.

5 In this exemplary embodiment, the signal U_s is used not only for initiating a motor start but also for operational monitoring of the control device 10. If a disturbance should occur during the operation of the control device 10, as a result of which the control device assumes an operating voltage value which, in this
10 exemplary embodiment, can be U_+ or earth, the state of the signal S_0 of the gate 17 changes, and the driving of the output stage contained in stage 18 changes therewith.

Firstly, let possible disturbed operation in the interval between t_1 and t_2 be considered, in which the
15 signal U_s assumes the positive operating voltage U_+ , as a result of which U_{a2} also becomes "high". Since U_+ is greater than both U_{r1} and U_{r3} , both the signals U_{a1} , U_{a3} are "high" and the signal S_0 of the gate 17 becomes "low". This has the effect that the stage 18 slows down
20 the motor 13 in a prescribed way from an instantaneous rotational speed to a standby speed. This standby speed can mean, for example, the standstill of the motor 10.

A second possible disturbed case is shown above the time t_2 . Here the signals U_s and U_i are intended to
25 assume the value of earth potential. Since this lies below both U_{r1} and U_{r3} , the signals U_{a1} and U_{a3} become "low". Hence, S_0 is also "low" and standby operation is maintained.

The cases shown in Fig. 2 represent a special
30 case to the extent that the first disturbance (t_1 - t_2) occurs first and the second disturbance (after t_2) then occurs subsequently. It is of course possible that the signal U_i falls directly to earth potential after normal operation. As a result, standby operation is then accord-
35 ingly initiated, in that the motor 13 is slowed down.

In describing this exemplary embodiment it was initially assumed that the signal U_s was sampled between the two values U_+ , U_m of the operating voltages. However, it is also possible that a lower range is provided for

the signal U_s . In this case, the circuit of Fig. 1 can also be used for the purpose of determining a possible DC component of the signal U_s .

5 The block diagram of a second exemplary embodiment is shown in Fig. 3 and is explained with the aid of Fig. 4. Means and signals having an analogous function as in the case of the exemplary embodiment of Fig. 1 and Fig. 2 are designated as they were there. They will be discussed below only to the extent that is essential for
10 the understanding of the present invention.

The essential difference from the exemplary embodiment of Fig. 1 lies in the fact that another type of conditioning of the signal U_s is carried out. The latter is not routed via the smoothing element 11 but via
15 a capacitor 20, which is connected in series with a resistor 21. At the connection between the elements 20, 21 a signal $U_{i'}$ is tapped off and fed to the comparators 14, 15, 16. In this case the signal $U_{i'}$ passes in each case at the comparators 14 and 15 to the noninverting
20 input and at the comparator 16 to the inverting input. The resistor 21 is connected to the centre tap of a voltage divider which is formed from resistors 22, corresponding to 22a-22d, and which serves to generate the reference voltages U_{r1} , U_{r2} , U_{r3} , which are in each
25 case applied to the free inputs of the comparators 14-16. The output signals U_{a1} and U_{a3} are fed to the OR-gate, which is designated here by 17', since in this exemplary embodiment it can be designed as a "simple" OR-gate, and does not necessarily need to be an EXCLUSIVE-OR gate. In
30 the case of a preferred embodiment, the gate 17' is realized by two diodes which are in each case connected downstream of the comparators 14 and 15 in the forward direction, as is indicated inside block 17'.

Connected downstream of gate 17 is a capacitor 23
35 which has the effect that, if the signal S_0 is switched over briefly, this is not noticeable by the stage 18.

Figures 4a and 4b show the variation of the signals U_s and $U_{i'}$. In the event of a change of U_s from "low" to "high", the right-hand side of the capacitor 20



(see Fig. 3), from which the signal U_i' is taken, is recharged in a finite time, that is to say only approximately abruptly, to a voltage whose value is close to the positive supply voltage U_+ of the control device 10. As long as U_s remains "high", the right-hand capacitor side is discharged exponentially via the resistor 21 in the direction of the reference voltage U_{r2} , which is picked off at the centre tap of the voltage divider.

The values for the elements 20, 21 are selected in such a way that, within the intervals t_h and t_l , in which the signal U_s is respectively "high" and "low" in normal operation, the signal U_i' does not fall below the first reference value U_{r1} or does not exceed the third reference value U_{r3} , respectively. Hence, in normal operation, during the intervals t_h , the first output signal U_{a1} is "high" (see Fig. 2c) and the third output signal U_{a3} is "low" (see Fig. 2e).

At this point it should be noted that the vertical auxiliary lines of Fig. 4, which are drawn with dashed lines or chain-dotted lines, have the following meaning: the chain-dotted lines mark the points in time at which the signal U_s changes its state in each case. The dashed lines mark those points in time at which the signal U_i' respectively exceeds or falls below the second reference value U_{r2} and at which the signal U_{a2} accordingly respectively changes its state. In this case, gate propagation times have been neglected.

In the case of a change in the signal U_s from "high" to "low", the signal U_i' falls with a finite speed to a value which virtually corresponds to that of the earth potential U_m . The exponential voltage variation on the right-hand side of the capacitor once more tends to U_{r2} , the third reference voltage U_{r3} not being exceeded in normal operation, however.

By means of the variation of the signal U_i' , as is shown in Fig. 2b in the interval t_0 to t_1 , the effect is achieved that one of the output signals U_{a1} , U_{a2} is always "high", if it is initially neglected that in the event of a voltage jump in U_s the signal U_i' does not



follow arbitrarily quickly. Hence, the output signal S_o of the gate 17 is "high" in normal operation. However, since, as already indicated, U_i' rises or falls only at a finite speed, brief drops in the signal S_o are to be expected. However, these are smoothed by the capacitor 23 in such a way that they are not noticeable by the stage 18 and that taking account of the jumps can be omitted in Fig. 4f.

In implementing the OR-gate 17', it is to be taken into account that, during the brief drops in its output signal, discharging of the capacitor 23 is avoided. This is achieved, for example, by realizing the gate 17' by means of the two diodes, which are drawn in block 17'. It is furthermore possible to use another type of OR gate, such as is realized, for example, by a TTL gate. However, an additional diode is then possibly necessary between the output of the gate 17' and the capacitor 23.

If normal operation is left at a point in time t_1 , in that the signal U_s assumes the constant "high" value, the exponential voltage drop on the right-hand side of the capacitor leads to the voltage falling below the first reference voltage U_{r1} at the point in time t_1' . Then, apart from the third output signal U_{a3} , the first output signal U_{a1} also becomes "low" and hence also the gate output signal S_o . This situation is detected by the stage 18, which then drives the output stage contained in it in such a way that the motor 13 is slowed down to a standby speed.

In the case of an operational disturbance, in which the signal U_s constantly assumes the earth potential, as is intended to be carried out after a point in time t_2 , U_i' initially falls below the values of the two reference voltages U_{r1} , U_{r3} , as a result of which normal operation is briefly faked by the gate signal S_o . However, from a point in time t_2' the reference value U_{r3} is exceeded and an operational disturbance is detected.

The advantage of the exemplary embodiment of Fig. 2 as compared with that of Fig. 1 lies in particular



in the fact that there is reliable monitoring for the control device 10 and the drive stage 12 even in the case of different operating voltages U_+ , U_+' . In the event that the second reference voltage U_{r2} has a value of 2.5 volt and the two other reference voltages U_{r1} , U_{r3} lie symmetrically around this value, faulty functioning occurs in Fig. 1 if the operating voltage U_+ of the control device 10 is, for example, 2 volt or 10 volt and the control signal U_s is sampled between U_+ and earth. Even in the case of slight deviations in the operating voltages from each other, faulty functioning is to be expected in the case of the exemplary embodiment according to Fig. 1, but not in the case of the circuit of Fig. 3.

In the case of configuring the exemplary embodiment according to Fig. 3, the charging of the right-hand side of the capacitor can be effected by means of a controlled current source. The latter is connected, for example, directly between the right-hand side of the capacitor and an operating voltage, such as U_+' or earth, and can be controlled by a comparison signal whose value is a measure of the voltage difference between that voltage applied to the right-hand side of the capacitor and a desired voltage such as, for example, the second reference voltage U_{r2} . Depending on the current source and the said comparison signal, a desired variation of voltage with time can be set for the right-hand side of the capacitor. This can vary exponentially, linearly or in accordance with another function.

Further versions of the exemplary embodiments can have at least one of the following variations:

- the signal U_s can be divided into a first signal, which is used for driving the stage 18 and can be fed to the latter directly, and into a second signal which is used for monitoring the alternating signal U_s . In this case, a second feed line to the circuit 12 is necessary, but the comparator 15 can be dispensed with;
- by means of suitable selection of the values for the



reference voltages U_r , it is possible not only to detect when the signal U_s assumes a DC value, but also to detect exceeding or falling below prescribed pulse duty ratios;

- 5 - more than three reference voltages can be provided. As a result it is possible, for example, to detect corresponding DC components and further functions in the circuit 12 can then be controlled using only one connecting line. If the signal U_s is designed as a pulse-width-modulated (PWM) signal, it is also
- 10 possible to detect corresponding values of the clock ratio corresponding to the number of reference voltages. This can be used for monitoring the operation of a load, such as that of the motor 13.
- 15 Reference should be made at this point in particular to the previous Applications P 42 27 761.2, in which the determination is described of the value of a current with which a PWM load is driven, and to P 42 29 344.8, in which a load is controlled as a
- 20 function of a temperature;
- after a disturbance has been detected once, in the event that a normal case is detected later, the stage 18 can automatically once more control a downstream load, such as the motor 13, into normal
- 25 operation, or provision can also be made for this to be effected only after the receipt of a confirmation signal which is output by means which are not shown or by a user of the system whose functioning is being monitored;
- 30 - the exemplary embodiments can be used as part of a video recorder, a compact disk (CD) player or another device having a motor;
- instead of a device with a motor, functions of other devices or systems can be monitored in the ways
- 35 described;
- instead of functional monitoring, the manner in which control signals are converted into U_i and U_i' , respectively, and the subsequent evaluation can also be used for controlling other functions.





PATENT CLAIMS

1. Method for monitoring an alternating signal (U_s), characterized in that

- 5 - the alternating signal (U_s) is conditioned in such a way that a conditioned signal (U_i ; U_i') is generated whose time variation is a measure of the clock ratio and/or of the possible DC component of the alternating signal, in that
- 10 - the conditioned signal (U_i ; U_i') is compared with prescribed reference values (U_{r1} , U_{r3}), as a result of which corresponding comparison values (U_{a1} , U_{a3}) are produced, and in that
- 15 - on the basis of the comparison values (U_{a1} , U_{a3}), conclusions are drawn about the clock ratio and/or the DC component of the alternating signal.

2. Method according to Claim 1, characterized in that the alternating signal (U_s) is conditioned in that it is smoothed, the conditioned signal (U_i) having a DC component whose value is a measure of the clock ratio and/or the DC component of the alternating signal (U_s), and being able to have an AC component with a prescribed amplitude, the alternating signal (U_s) optionally being able to be regenerated from the AC component (U_{a2}).

3. Method according to Claim 1, characterized in that the alternating signal (U_s) is conditioned in that a signal derived from it has applied to it a voltage in such a way that, following a voltage change in the alternating signal (U_s), the derived signal tends towards a prescribed voltage value (U_{r2}) with a prescribed time variation.

4. Method according to one of Claims 1 to 3, characterized in that, on the basis of the comparison signals (U_{a1} , U_{a3}), a control signal (S_o) is formed whose value is a measure of a possible operational disturbance.

35 5. Method according to one of Claims 1 to 4, characterized in that, on the basis of the values of the comparison signals (U_{a1} , U_{a3}), means (13), which can be controlled with the aid of the alternating signal, are controlled down into quiescent operation (standby





operation).

6. Device for monitoring an alternating signal (U_s) which is generated by generator means (10), characterized in that

- 5 - a conditioning stage (11; 20, 21) is provided which conditions the alternating signal (U_s) in such a way that a conditioned signal (U_i ; U_i') is generated whose time variation is a measure of the clock ratio and/or a possible DC component of the alternating
- 10 signal, in that
 - comparison means (14, 16) are provided which compare the conditioned signal (U_i ; U_i') with prescribed reference values (U_{r1} , U_{r3}), as a result of which corresponding comparison values (U_{a1} , U_{a3}) are
 - 15 produced, and in that
 - evaluation means (17, 18) are provided which, on the basis of the comparison values (U_{a1} , U_{a3}), draw conclusions about the clock ratio and/or the DC component of the alternating signal.

20 7. Device according to Claim 6, characterized in that the conditioning stage contains smoothing means (11) which smooth the alternating signal (U_s) in such a way that the conditioned signal (U_i) has a DC component whose value is a measure of the pulse duty ratio and/or the DC

25 component of the alternating signal (U_s), and can have an AC component with a prescribed amplitude, the alternating signal (U_s) optionally being able to be regenerated from the AC component (U_{a2}).

8. Device according to Claim 6, characterized in

30 that the conditioning stage has a capacitor (20) which is connected by its first terminal to the generator (10), in that there is a voltage or current device (21, 22) which charges or discharges the second terminal with a prescribed current, as a result of which a conditioned

35 signal (U_i') is generated which, following a voltage change of the alternating signal (U_s), tends towards a prescribed voltage value (U_{r2}) with a prescribed time variation.

9. Device according to one of Claims 6 to 8, charac-





terized in that, on the basis of the comparison signals (Ua1, Ua3), evaluation means (17) form a control signal (So) whose value is a measure of a possible operational disturbance.

- 5 10. Device according to one of Claims 6 to 9, characterized in that, on the basis of the values of the comparison signals (Ua1, Ua3), means (13) which can be controlled with the aid of the alternating signal are controlled down into quiescent operation (standby
10 operation).



ABSTRACT

1. Method and device for monitoring an alternating signal.
- 2.1 It is the object of the present invention to monitor the state, such as the clock ratio or DC component, of an alternating signal.
- 2.2 According to the invention, the alternating signal to be monitored is conditioned in such a way that, by means of a simple comparison with reference voltages, it is possible to draw conclusions about the clock ratio or a DC component. As a result, for example, various information can be transmitted over one feed line. It is also possible to monitor the operating state of the stage generating the alternating signal.
- 2.3 The invention may be used, for example, for operational monitoring of a video recorder.
3. Fig. 1.

1/4

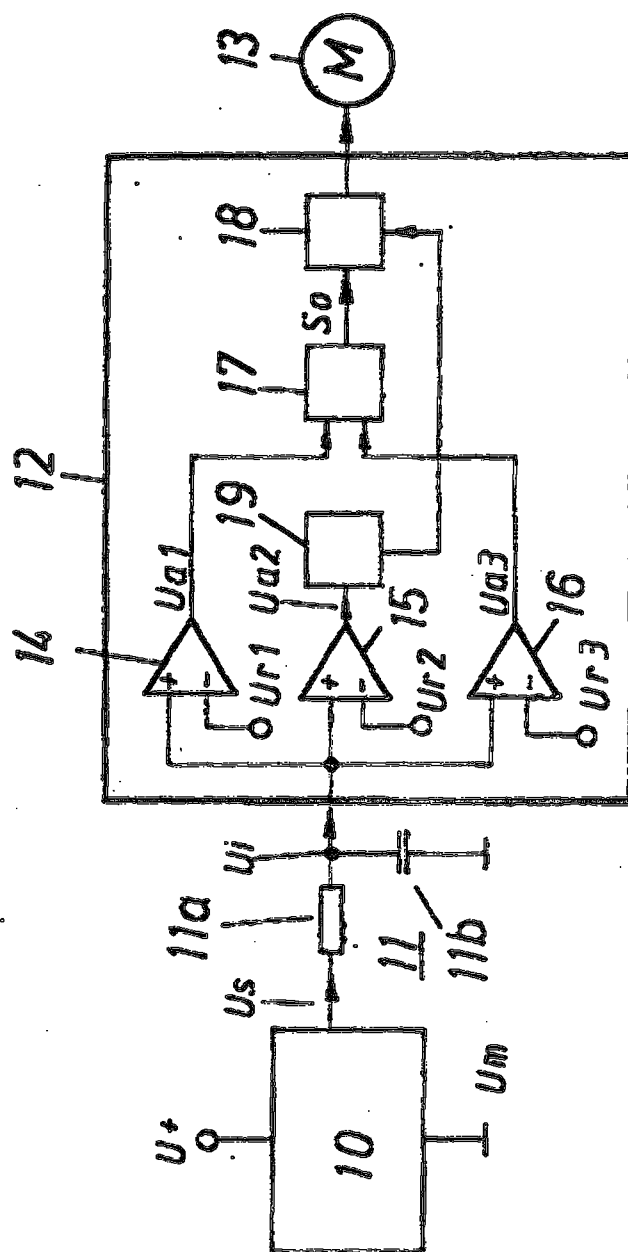


FIG. 1



2/4

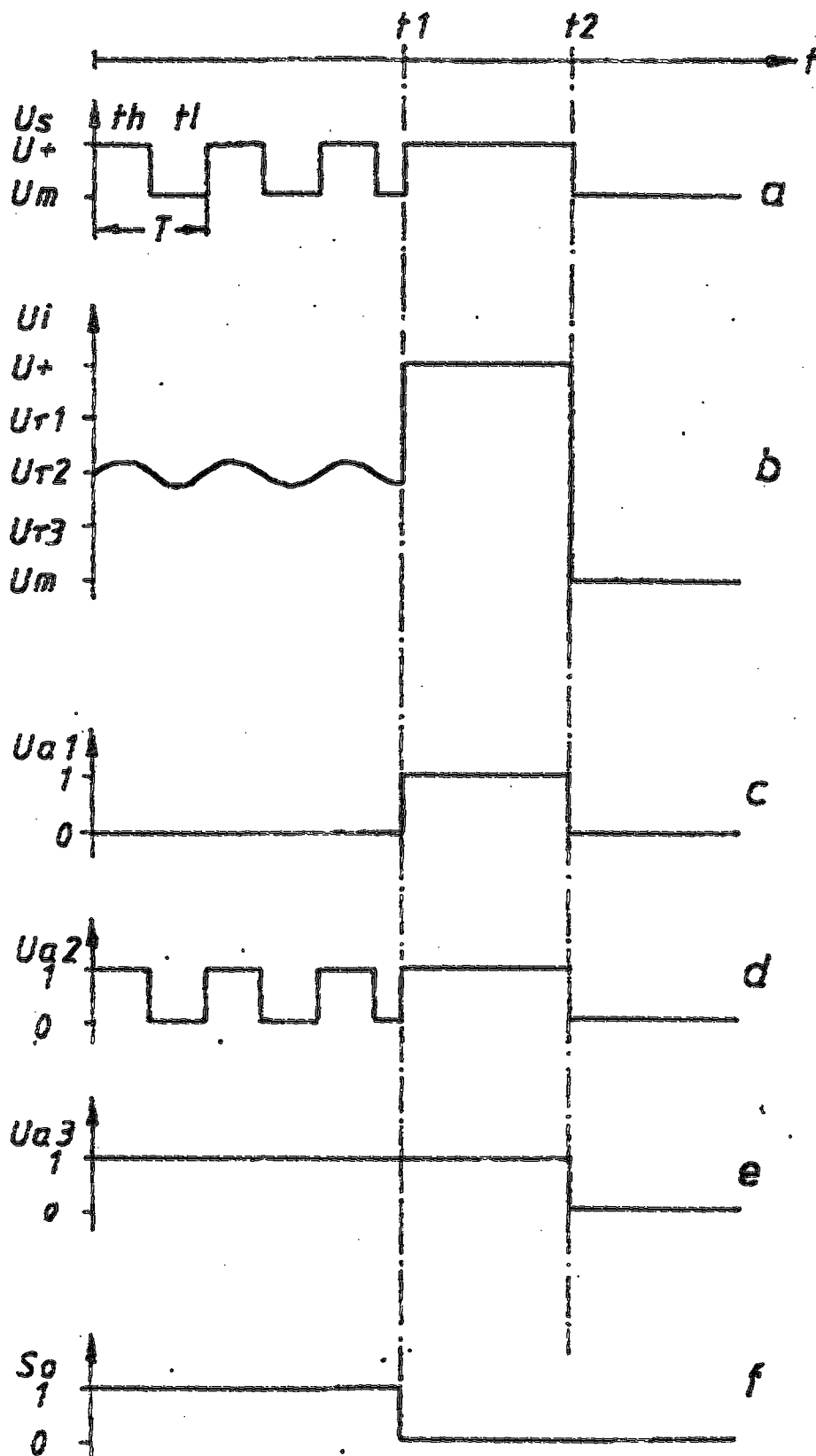


FIG. 2



3/4

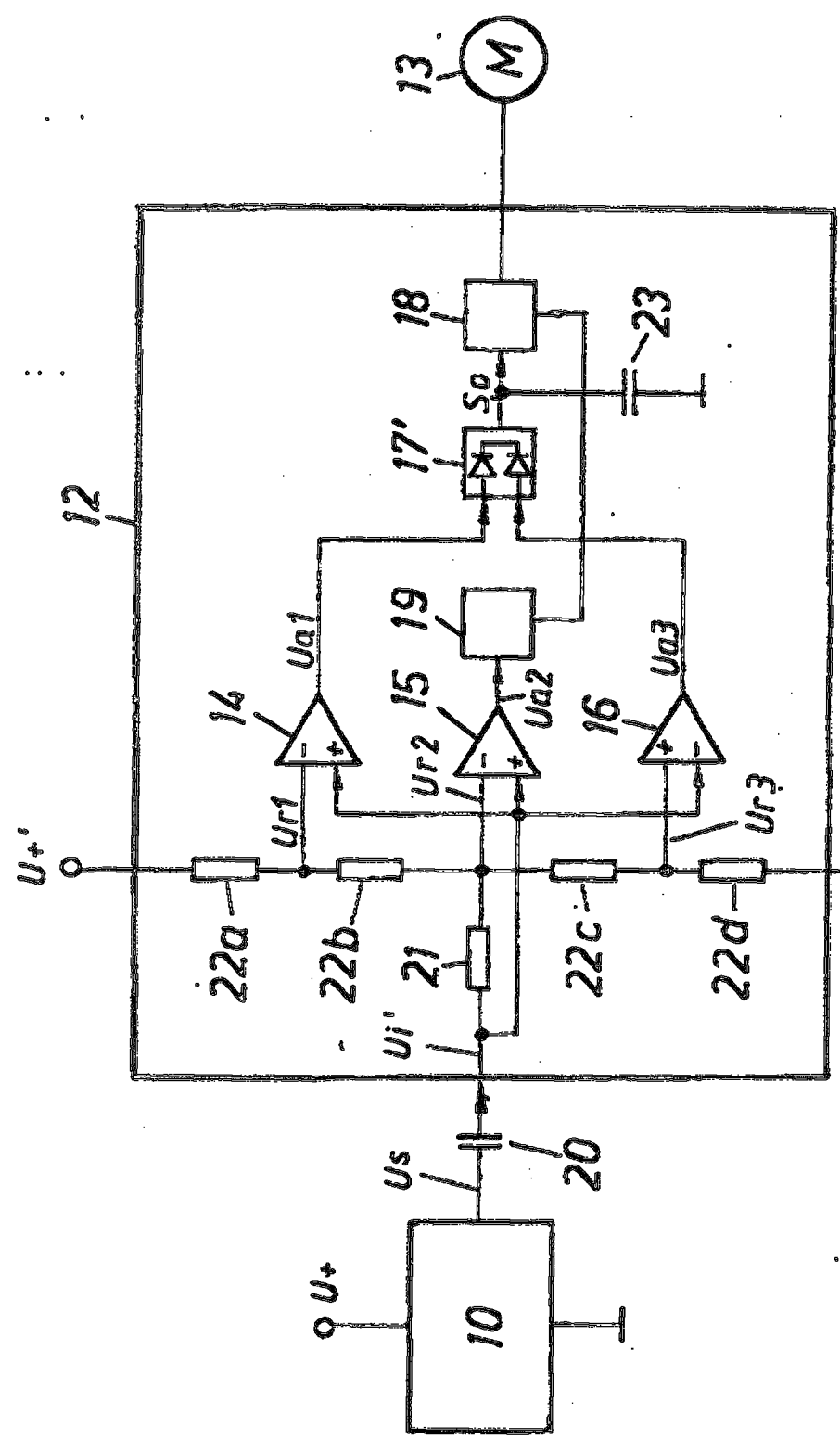


FIG. 3

4/4

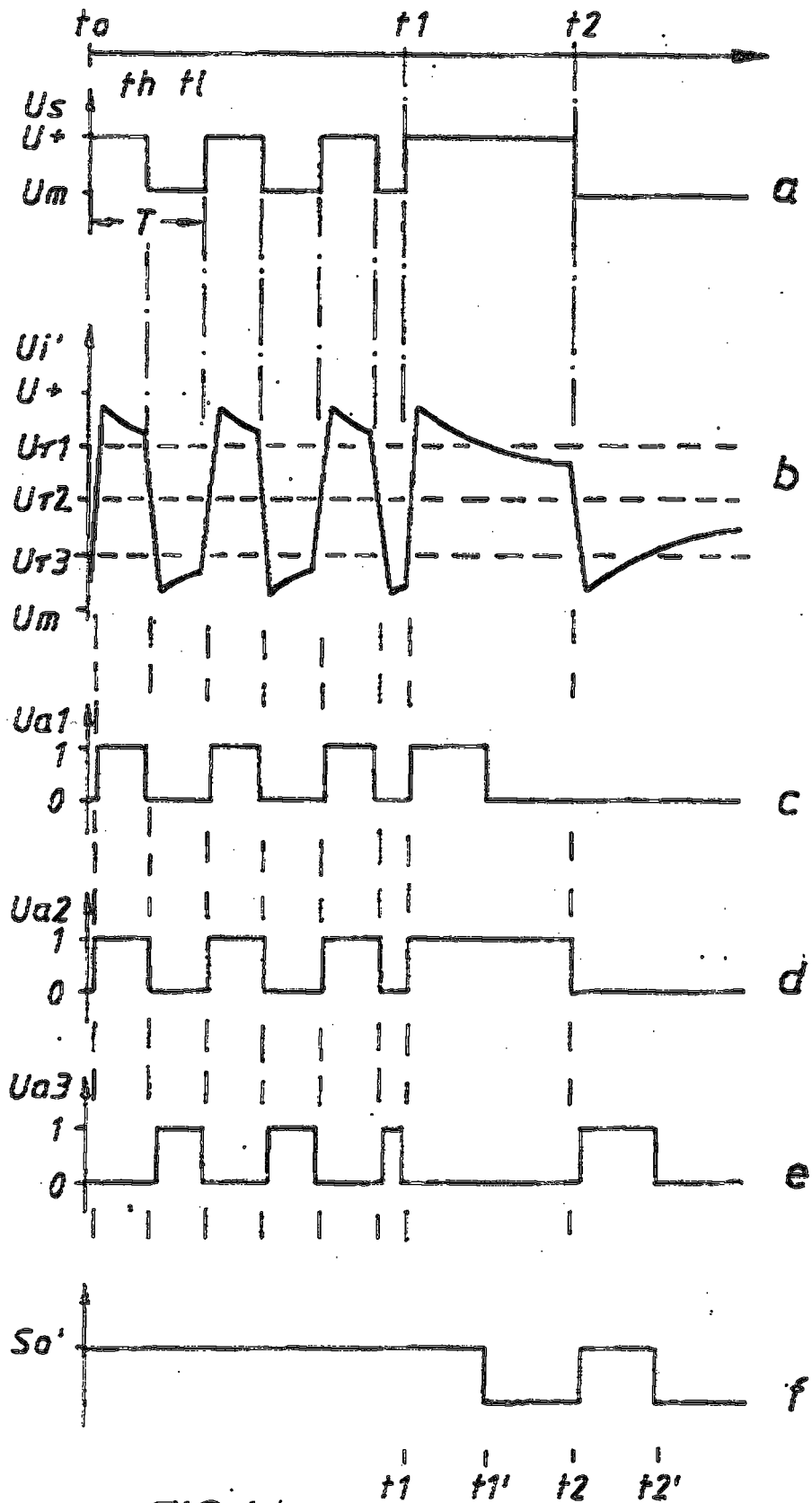


FIG. 4

This Sheet Has Been Replaced



REPLACED SHEETS		SG
☒	Description	: paged ... to paged ...
☒	Claim(s)	: paged ... to paged ...
☒	Drawing(s)	: paged ... to paged ...
☒	Abstract	: paged ... to paged ...
DATE OF RECEIPT		

REPLACEMENT SHEETS		SG
☒	Description	: paged ... to paged ...
☒	Claim(s)	: paged ... to paged ...
☒	Drawing(s)	: paged ... to paged ...
☒	Abstract	: paged ... to paged ...
DATE OF RECEIPT ...		

Method and device for monitoring an
alternating signal

The present invention relates to a method for monitoring an alternating signal in accordance with the precharacterizing clause of Claim 1 and a device in accordance with the precharacterizing clause of the first substantive claim.

The use of stages which output an alternating signal which is used for controlling a connected stage is generally known. Control stages of this type may contain, for example, a microprocessor which outputs an alternating signal in the form of a digital signal and thus controls a connected stage. Oscillators are also known which use a sinusoidal, rectangular or other alternating signal for processing further signals by means of corresponding stages.

Various possibilities are conceivable for a signal which is of the type output by a control stage of the said type, is alternating, also called changing below, to change its course. Thus, for example, a potential shift may occur in that a DC voltage is superimposed upon the changing signal. It is furthermore possible that the pulse duty ratio of the changing signal changes. Depending on the device in which the control stage is used and/or depending on the operating state, changes of this type can be intentional or can point to a fault in the control stage.

It is the object of the present invention to monitor the state of an alternating signal in a simple way.

This object is achieved by means of a method according to the main claim and by means of a device in accordance with the first substantive claim.

According to the invention, an alternating signal which is generated, for example, by a control stage or by an oscillator, is conditioned in such a way that, by means of comparing the conditioned signal with reference values, signals are generated which can be evaluated in a simple way.

This Sheet Has Been Replaced

This is the replacement sheet



Date: 17 FEB 1997



- 2 -

The conditioning of the changing signal can be effected, for example, in that the latter is essentially smoothed. The value of the smoothed signal is a measure of a possible DC component and/or of the clock ratio of the changing signal.

Another possibility for conditioning is, for example, to route the changing signal via a capacitor which is connected in series between a first stage, which is generating the changing signal, and a second stage, which is controlled by this signal. In this arrangement, the first side of the capacitor, which is connected to the second stage, is charged by means of a voltage source, a current source or the like in such a way that, in the event of no change or only small changes in the potential at the second side, connected to the first stage, of the capacitor, the first side assumes specific voltage values in accordance with a prescribed time variation.

It should be pointed out that both the alternating signals which are used for control and the signals which are derived therefrom can be conditioned.

A variation in the pulse duty ratio and/or the DC component of the alternating signal can, for example, be used for controlling a connected stage or can also point to a functional disturbance. Thus, for example, in the case of a control stage of the type mentioned, an uncontrolled state may occur in which the output signal from the control stage corresponds to a DC voltage level, a positive operating voltage or earth potential. This can be caused, for example, by induction peaks or the like which influence the sequence of a control program which is being used for the functioning of the control stage. It is likewise conceivable that elements of the control stage become defective, that the supply voltage of the control stage fails, or the like.

In the cases mentioned, faulty functioning occurs of the stages connected to the control stage.

It is an advantage of the present invention that states of this type can be detected in a simple way and

This is the replacement sheet

Date: 17 FEB 1997



- 3 -

a prescribed state of the connected stages can then be controlled.

Operational monitoring of this type can be used, for example, in the case of a device such as a video recorder which drives a tape on which information is stored and from which information can be read.

Further features, advantages and details of the invention are explained in the following exemplary embodiments, with reference to the drawing, in which:

Fig. 1: shows the block diagram of a first exemplary embodiment;

Fig. 2: shows variations of signals in the exemplary embodiment of Fig. 1

Fig. 3: shows the block diagram of a second exemplary embodiment;

Fig. 4: shows variations of signals in the exemplary embodiment of Fig. 3

Before the description of the exemplary embodiments is gone into in more detail, it should be pointed out that the blocks shown individually in the figures are merely used for improved understanding of the invention. Normally, individual blocks or a plurality of these blocks are combined into units. These blocks may be realized in integrated or hybrid technology or as program-controlled microcomputers, or as part of a program suitable for controlling it.

The elements contained in the individual stages can also be of separate design, however.

Fig. 1 shows an electronic control device 10, which routes control signals U_s via a conditioning stage, which in this exemplary embodiment is designed as a smoothing element 11, to a drive stage 12, which applies current to a motor 13. The smoothing element 11 comprises a resistor 11a, whose first terminal is connected to the output of the control device 10, and a capacitor 11b, which is connected between the second terminal of the resistor 11a and earth. The smoothing element 11 effects smoothing of the control signal U_s , as a result of which a signal U_i is formed. The latter is then fed to the

This is the replacement sheet

Date: 17 FEB 1997



- 4 -

noninverting (+) inputs of a first comparator 14, a second comparator 15 and a third comparator 16. The comparators 14, 15, 16 are connected by their inverting (-) inputs to a first reference voltage U_{r1} , to a second reference voltage U_{r2} and to a third reference voltage U_{r3} . The output signals U_{a1} and U_{a3} from the comparators 14, 16 are each fed to an input of an EXCLUSIVE-OR gate 17, whose output signal S_o is fed to further drive means which apply current to the motor 13. These further drive means, which inter alia contain an output stage, and means which evaluate the signal S_o and a signal S_s of a starting stage 19 and then drive the output stage as described below, are represented symbolically in Fig. 1 by the stage 18.

The output signal U_{a2} from the comparator passes to the starting stage 19, whose output signal S_s is fed to the stage 18.

The functioning of the exemplary embodiment of Fig. 1 is explained below with the aid of Fig. 2 only to the extent that is necessary for understanding the present invention.

In order to start the motor 13 running, the control device 10 outputs the clocked control signal U_s , which leads to a smoothed signal U_i , as is represented in Figures 2a and 2b in the interval between t_0 and t_1 . The signal U_i has a residual ripple which, for the purposes of better understanding, is drawn somewhat exaggerated. The values of the reference voltages U_r are likewise drawn in Figure 2b. The comparators output signals U_a , as is shown in Figures 2c) to 2e).

Normal operation, such as is present during the interval between t_0 and t_1 , will be considered first. On the basis of the signal U_i , the comparator 15 simulates the output signal U_{a2} with a variation which corresponds to the clock rate of the original output signal U_s , with a clock ratio t_h/t_l during a period T . The signal U_{a1} is "low", that is to say it assumes the digital value "0", and the signal U_{a2} is "high", corresponding to the value "1". Hence, as can be seen from Fig. 2f, the output

This is the replacement sheet

Date: 17 FEB 1997



- 5 -

signal S_o of the EX-OR gate 17 is high, as a result of which the operation of the output stage containing the stage 18 is not impaired.

In this exemplary embodiment, the signal U_s is used not only for initiating a motor start but also for operational monitoring of the control device 10. If a disturbance should occur during the operation of the control device 10, as a result of which the control device assumes an operating voltage value which, in this exemplary embodiment, can be U_+ or earth, the state of the signal S_o of the gate 17 changes, and the driving of the output stage contained in stage 18 changes therewith.

Firstly, let possible disturbed operation in the interval between t_1 and t_2 be considered, in which the signal U_s assumes the positive operating voltage U_+ , as a result of which U_{a2} also becomes "high". Since U_+ is greater than both U_{r1} and U_{r3} , both the signals U_{a1} , U_{a3} are "high" and the signal S_o of the gate 17 becomes "low". This has the effect that the stage 18 slows down the motor 13 in a prescribed way from an instantaneous rotational speed to a standby speed. This standby speed can mean, for example, the standstill of the motor 10.

A second possible disturbed case is shown above the time t_2 . Here the signals U_s and U_i are intended to assume the value of earth potential. Since this lies below both U_{r1} and U_{r3} , the signals U_{a1} and U_{a3} become "low". Hence, S_o is also "low" and standby operation is maintained.

The cases shown in Fig. 2 represent a special case to the extent that the first disturbance (t_1 - t_2) occurs first and the second disturbance (after t_2) then occurs subsequently. It is of course possible that the signal U_i falls directly to earth potential after normal operation. As a result, standby operation is then accordingly initiated, in that the motor 13 is slowed down.

In describing this exemplary embodiment it was initially assumed that the signal U_s was sampled between the two values U_+ , U_m of the operating voltages. However, it is also possible that a lower range is provided for

This is the replacement sheet

Date: 17 FEB 1997



the signal U_s . In this case, the circuit of Fig. 1 can also be used for the purpose of determining a possible DC component of the signal U_s .

The block diagram of a second exemplary embodiment is shown in Fig. 3 and is explained with the aid of Fig. 4. Means and signals having an analogous function as in the case of the exemplary embodiment of Fig. 1 and Fig. 2 are designated as they were there. They will be discussed below only to the extent that is essential for the understanding of the present invention.

The essential difference from the exemplary embodiment of Fig. 1 lies in the fact that another type of conditioning of the signal U_s is carried out. The latter is not routed via the smoothing element 11 but via a capacitor 20, which is connected in series with a resistor 21. At the connection between the elements 20, 21 a signal U_i' is tapped off and fed to the comparators 14, 15, 16. In this case the signal U_i' passes in each case at the comparators 14 and 15 to the noninverting input and at the comparator 16 to the inverting input. The resistor 21 is connected to the centre tap of a voltage divider which is formed from resistors 22, corresponding to 22a-22d, and which serves to generate the reference voltages U_{r1} , U_{r2} , U_{r3} , which are in each case applied to the free inputs of the comparators 14-16. The output signals U_{a1} and U_{a3} are fed to the OR-gate, which is designated here by 17', since in this exemplary embodiment it can be designed as a "simple" OR-gate, and does not necessarily need to be an EXCLUSIVE-OR gate. In the case of a preferred embodiment, the gate 17' is realized by two diodes which are in each case connected downstream of the comparators 14 and 16 in the forward direction, as is indicated inside block 17'.

Connected downstream of gate 17 is a capacitor 23 which has the effect that, if the signal S_0 is switched over briefly, this is not noticeable by the stage 18.

Figures 4a and 4b show the variation of the signals U_s and U_i' . In the event of a change of U_s from "low" to "high", the right-hand side of the capacitor 20

This is the replacement sheet

Date: 17 FEB 1997



(see Fig. 3), from which the signal U_i' is taken, is recharged in a finite time, that is to say only approximately abruptly, to a voltage whose value is close to the positive supply voltage U_+ of the control device 10. As long as U_s remains "high", the right-hand capacitor side is discharged exponentially via the resistor 21 in the direction of the reference voltage U_{r2} , which is picked off at the centre tap of the voltage divider.

The values for the elements 20, 21 are selected in such a way that, within the intervals t_h and t_l , in which the signal U_s is respectively "high" and "low" in normal operation, the signal U_i' does not fall below the first reference value U_{r1} or does not exceed the third reference value U_{r3} , respectively. Hence, in normal operation, during the intervals t_h , the first output signal U_{a1} is "high" (see Fig. 2c) and the third output signal U_{a3} is "low" (see Fig. 2e).

At this point it should be noted that the vertical auxiliary lines of Fig. 4, which are drawn with dashed lines or chain-dotted lines, have the following meaning: the chain-dotted lines mark the points in time at which the signal U_s changes its state in each case. The dashed lines mark those points in time at which the signal U_i' respectively exceeds or falls below the second reference value U_{r2} and at which the signal U_{a2} accordingly respectively changes its state. In this case, gate propagation times have been neglected.

In the case of a change in the signal U_s from "high" to "low", the signal U_i' falls with a finite speed to a value which virtually corresponds to that of the earth potential U_m . The exponential voltage variation on the right-hand side of the capacitor once more tends to U_{r2} , the third reference voltage U_{r3} not being exceeded in normal operation, however.

By means of the variation of the signal U_i' , as is shown in Fig. 2b in the interval t_0 to t_1 , the effect is achieved that one of the output signals U_{a1} , U_{a2} is always "high", if it is initially neglected that in the event of a voltage jump in U_s the signal U_i' does not

This is the replacement sheet

Date: 17 FEB 1997



follow arbitrarily quickly. Hence, the output signal S_o of the gate 17 is "high" in normal operation. However, since, as already indicated, U_i' rises or falls only at a finite speed, brief drops in the signal S_o are to be expected. However, these are smoothed by the capacitor 23 in such a way that they are not noticeable by the stage 18 and that taking account of the jumps can be omitted in Fig. 4f.

In implementing the OR-gate 17', it is to be taken into account that, during the brief drops in its output signal, discharging of the capacitor 23 is avoided. This is achieved, for example, by realizing the gate 17' by means of the two diodes, which are drawn in block 17'. It is furthermore possible to use another type of OR gate, such as is realized, for example, by a TTL gate. However, an additional diode is then possibly necessary between the output of the gate 17' and the capacitor 23.

If normal operation is left at a point in time t_1 , in that the signal U_s assumes the constant "high" value, the exponential voltage drop on the right-hand side of the capacitor leads to the voltage falling below the first reference voltage U_{r1} at the point in time t_1' . Then, apart from the third output signal U_{a3} , the first output signal U_{a1} also becomes "low" and hence also the gate output signal S_o . This situation is detected by the stage 18, which then drives the output stage contained in it in such a way that the motor 13 is slowed down to a standby speed.

In the case of an operational disturbance, in which the signal U_s constantly assumes the earth potential, as is intended to be carried out after a point in time t_2 , U_i' initially falls below the values of the two reference voltages U_{r1} , U_{r3} , as a result of which normal operation is briefly faked by the gate signal S_o . However, from a point in time t_2' the reference value U_{r3} is exceeded and an operational disturbance is detected.

The advantage of the exemplary embodiment of Fig. 2 as compared with that of Fig. 1 lies in particular

This is the replacement sheet

Date: 17 FEB 1997



- 9 -

in the fact that there is reliable monitoring for the control device 10 and the drive stage 12 even in the case of different operating voltages U_+ , U_+' . In the event that the second reference voltage U_{r2} has a value of 2.5 volt and the two other reference voltages U_{r1} , U_{r3} lie symmetrically around this value, faulty functioning occurs in Fig. 1 if the operating voltage U_+ of the control device 10 is, for example, 2 volt or 10 volt and the control signal U_s is sampled between U_+ and earth. Even in the case of slight deviations in the operating voltages from each other, faulty functioning is to be expected in the case of the exemplary embodiment according to Fig. 1, but not in the case of the circuit of Fig. 3.

In the case of configuring the exemplary embodiment according to Fig. 3, the charging of the right-hand side of the capacitor can be effected by means of a controlled current source. The latter is connected, for example, directly between the right-hand side of the capacitor and an operating voltage, such as U_+' or earth, and can be controlled by a comparison signal whose value is a measure of the voltage difference between that voltage applied to the right-hand side of the capacitor and a desired voltage such as, for example, the second reference voltage U_{r2} . Depending on the current source and the said comparison signal, a desired variation of voltage with time can be set for the right-hand side of the capacitor. This can vary exponentially, linearly or in accordance with another function.

Further versions of the exemplary embodiments can have at least one of the following variations:

- the signal U_s can be divided into a first signal, which is used for driving the stage 18 and can be fed to the latter directly, and into a second signal which is used for monitoring the alternating signal U_s . In this case, a second feed line to the circuit 12 is necessary, but the comparator 15 can be dispensed with;
- by means of suitable selection of the values for the

This is the replacement sheet

Date: 17 FEB 1997



- 10 -

reference voltages U_r , it is possible not only to detect when the signal U_s assumes a DC value, but also to detect exceeding or falling below prescribed pulse duty ratios;

- more than three reference voltages can be provided. As a result it is possible, for example, to detect corresponding DC components and further functions in the circuit 12 can then be controlled using only one connecting line. If the signal U_s is designed as a pulse-width-modulated (PWM) signal, it is also possible to detect corresponding values of the clock ratio corresponding to the number of reference voltages. This can be used for monitoring the operation of a load, such as that of the motor 13. Reference should be made at this point in particular to the previous Applications P 42 27 761.2, in which the determination is described of the value of a current with which a PWM load is driven, and to P 42 29 344.8, in which a load is controlled as a function of a temperature;
- after a disturbance has been detected once, in the event that a normal case is detected later, the stage 18 can automatically once more control a downstream load, such as the motor 13, into normal operation, or provision can also be made for this to be effected only after the receipt of a confirmation signal which is output by means which are not shown or by a user of the system whose functioning is being monitored;
- the exemplary embodiments can be used as part of a video recorder, a compact disk (CD) player or another device having a motor;
- instead of a device with a motor, functions of other devices or systems can be monitored in the ways described;
- instead of functional monitoring, the manner in which control signals are converted into U_i and U_i' , respectively, and the subsequent evaluation can also be used for controlling other functions.

This is the replacement sheet

Date: 17 FEB 1997



- 11 -

PATENT CLAIMS

1. Method for monitoring an alternating signal (U_s), characterized in that

- the alternating signal (U_s) is conditioned in such a way that a conditioned signal (U_i ; U_i') is generated whose time variation is a measure of the clock ratio and/or of the possible DC component of the alternating signal, in that
- the conditioned signal (U_i ; U_i') is compared with prescribed reference values (U_{r1} , U_{r3}), as a result of which corresponding comparison values (U_{a1} , U_{a3}) are produced, and in that
- on the basis of the comparison values (U_{a1} , U_{a3}), conclusions are drawn about the clock ratio and/or the DC component of the alternating signal.

2. Method according to Claim 1, characterized in that the alternating signal (U_s) is conditioned in that it is smoothed, the conditioned signal (U_i) having a DC component whose value is a measure of the clock ratio and/or the DC component of the alternating signal (U_s), and being able to have an AC component with a prescribed amplitude, the alternating signal (U_s) optionally being able to be regenerated from the AC component (U_{a2}).

3. Method according to Claim 1, characterized in that the alternating signal (U_s) is conditioned in that a signal derived from it has applied to it a voltage in such a way that, following a voltage change in the alternating signal (U_s), the derived signal tends towards a prescribed voltage value (U_{r2}) with a prescribed time variation.

4. Method according to one of Claims 1 to 3, characterized in that, on the basis of the comparison signals (U_{a1} , U_{a3}), a control signal (S_o) is formed whose value is a measure of a possible operational disturbance.

5. Method according to one of Claims 1 to 4, characterized in that, on the basis of the values of the comparison signals (U_{a1} , U_{a3}), means (13), which can be controlled with the aid of the alternating signal, are controlled down into quiescent operation (standby

This is the replacement sheet



Date: 17 FEB 1997



operation).

6. Device for monitoring an alternating signal (U_s) which is generated by generator means (10), characterized in that

- a conditioning stage (11; 20, 21) is provided which conditions the alternating signal (U_s) in such a way that a conditioned signal (U_i ; U_i') is generated whose time variation is a measure of the clock ratio and/or a possible DC component of the alternating signal, in that
- comparison means (14, 16) are provided which compare the conditioned signal (U_i ; U_i') with prescribed reference values (U_{r1} , U_{r3}), as a result of which corresponding comparison values (U_{a1} , U_{a3}) are produced, and in that
- evaluation means (17, 18) are provided which, on the basis of the comparison values (U_{a1} , U_{a3}), draw conclusions about the clock ratio and/or the DC component of the alternating signal.

7. Device according to Claim 6, characterized in that the conditioning stage contains smoothing means (11) which smooth the alternating signal (U_s) in such a way that the conditioned signal (U_i) has a DC component whose value is a measure of the pulse duty ratio and/or the DC component of the alternating signal (U_s), and can have an AC component with a prescribed amplitude, the alternating signal (U_s) optionally being able to be regenerated from the AC component (U_{a2}).

8. Device according to Claim 6, characterized in that the conditioning stage has a capacitor (20) which is connected by its first terminal to the generator (10), in that there is a voltage or current device (21, 22) which charges or discharges the second terminal with a prescribed current, as a result of which a conditioned signal (U_i') is generated which, following a voltage change of the alternating signal (U_s), tends towards a prescribed voltage value (U_{r2}) with a prescribed time variation.

9. Device according to one of Claims 6 to 8, charac-

This is the replacement sheet

Date:

17 FEB 1997





- 13 -

terized in that, on the basis of the comparison signals (Ua1, Ua3), evaluation means (17) form a control signal (So) whose value is a measure of a possible operational disturbance.

10. Device according to one of Claims 6 to 9, characterized in that, on the basis of the values of the comparison signals (Ua1, Ua3), means (13) which can be controlled with the aid of the alternating signal are controlled down into quiescent operation (standby operation).



This is the replacement sheet

Date: 17 FEB 1997



ABSTRACT

Method and device for monitoring an alternating signal.

It is the object of the present invention to monitor the state, such as the clock ratio or DC component, of an alternating signal.

According to the invention, the alternating signal to be monitored is conditioned in such a way that, by means of a simple comparison with reference voltages, it is possible to draw conclusions about the clock ratio or a DC component. As a result, for example, various information can be transmitted over one feed line. It is also possible to monitor the operating state of the stage generating the alternating signal.

The invention may be used, for example, for operational monitoring of a video recorder.

Fig. 1.

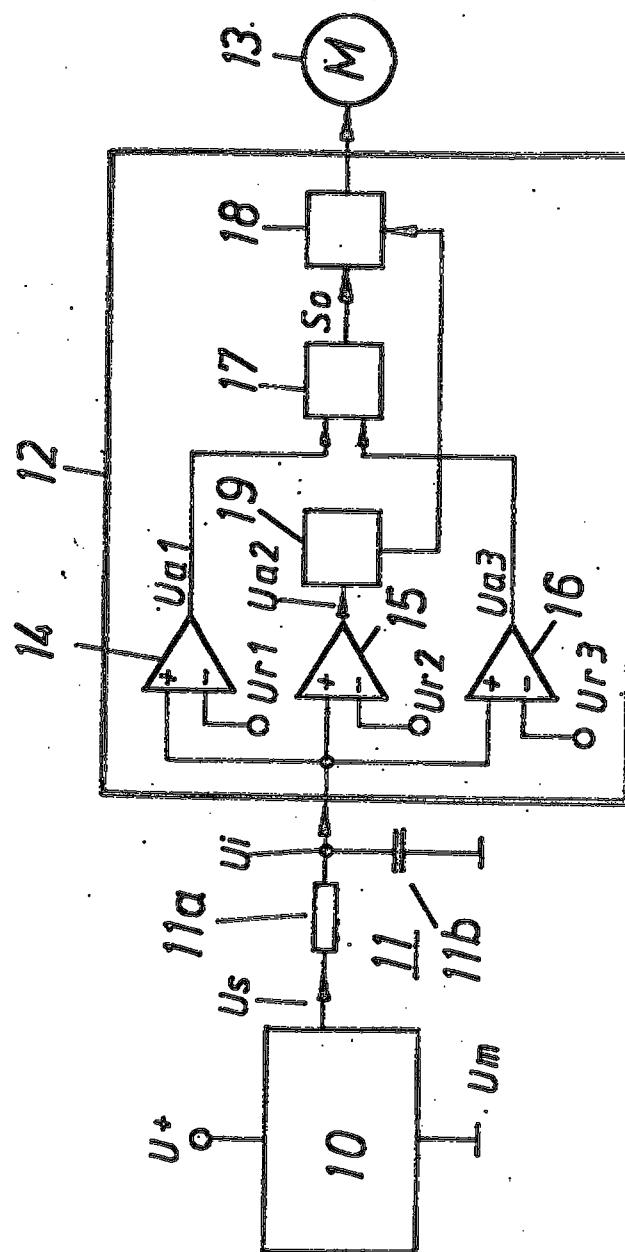


FIG. 1

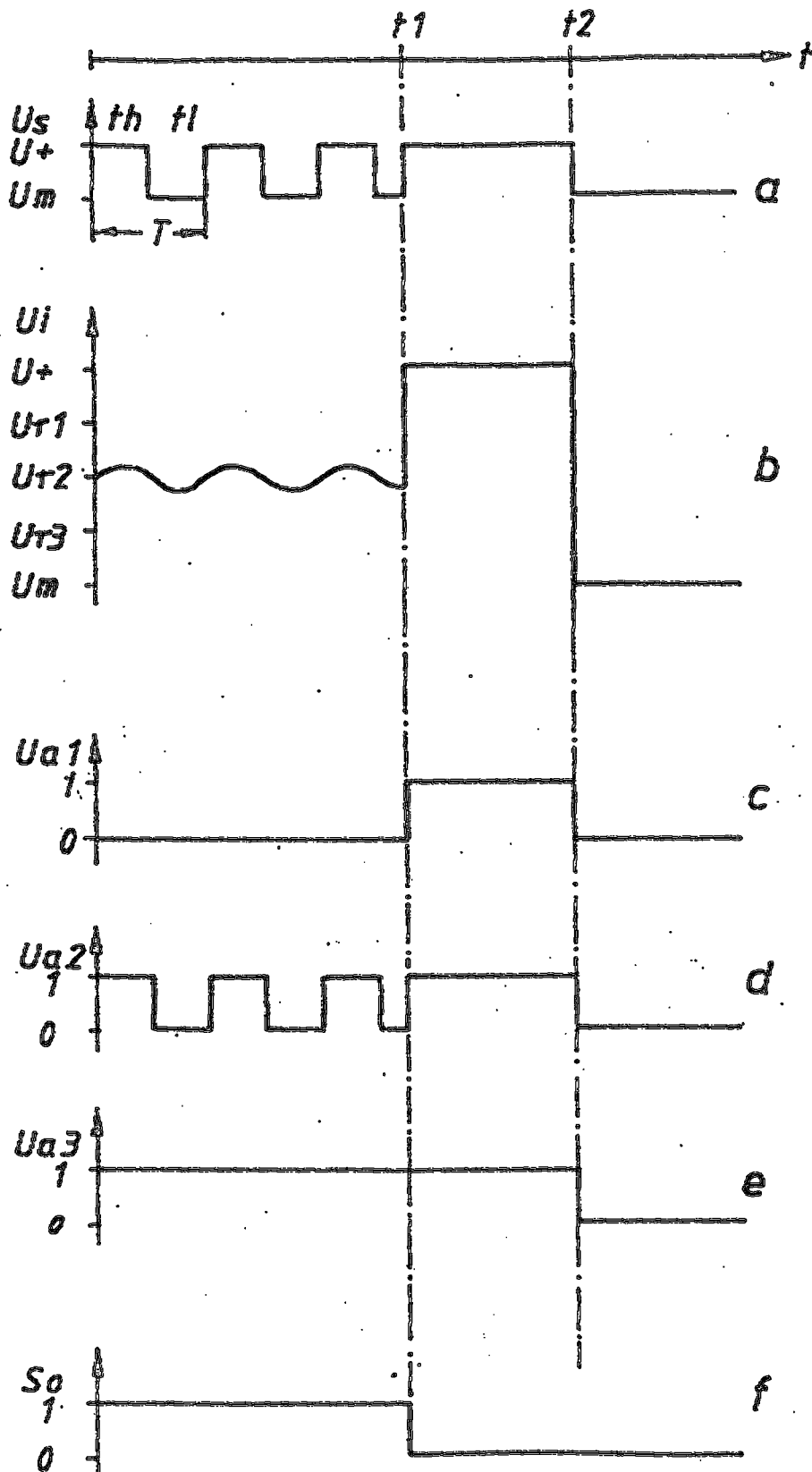


FIG. 2

This is the replacement sheet

Date: 17 FEB 1997

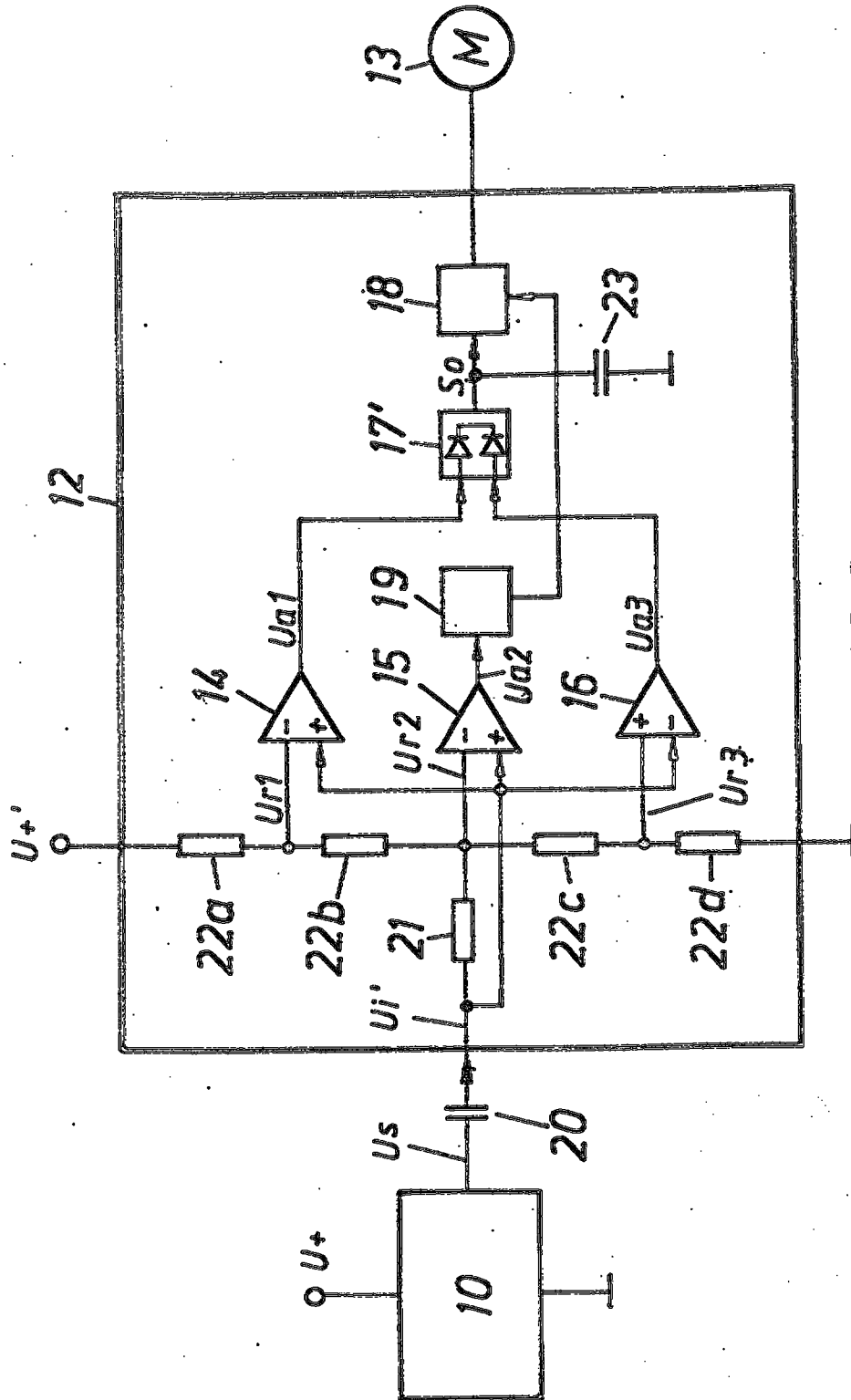


FIG. 3

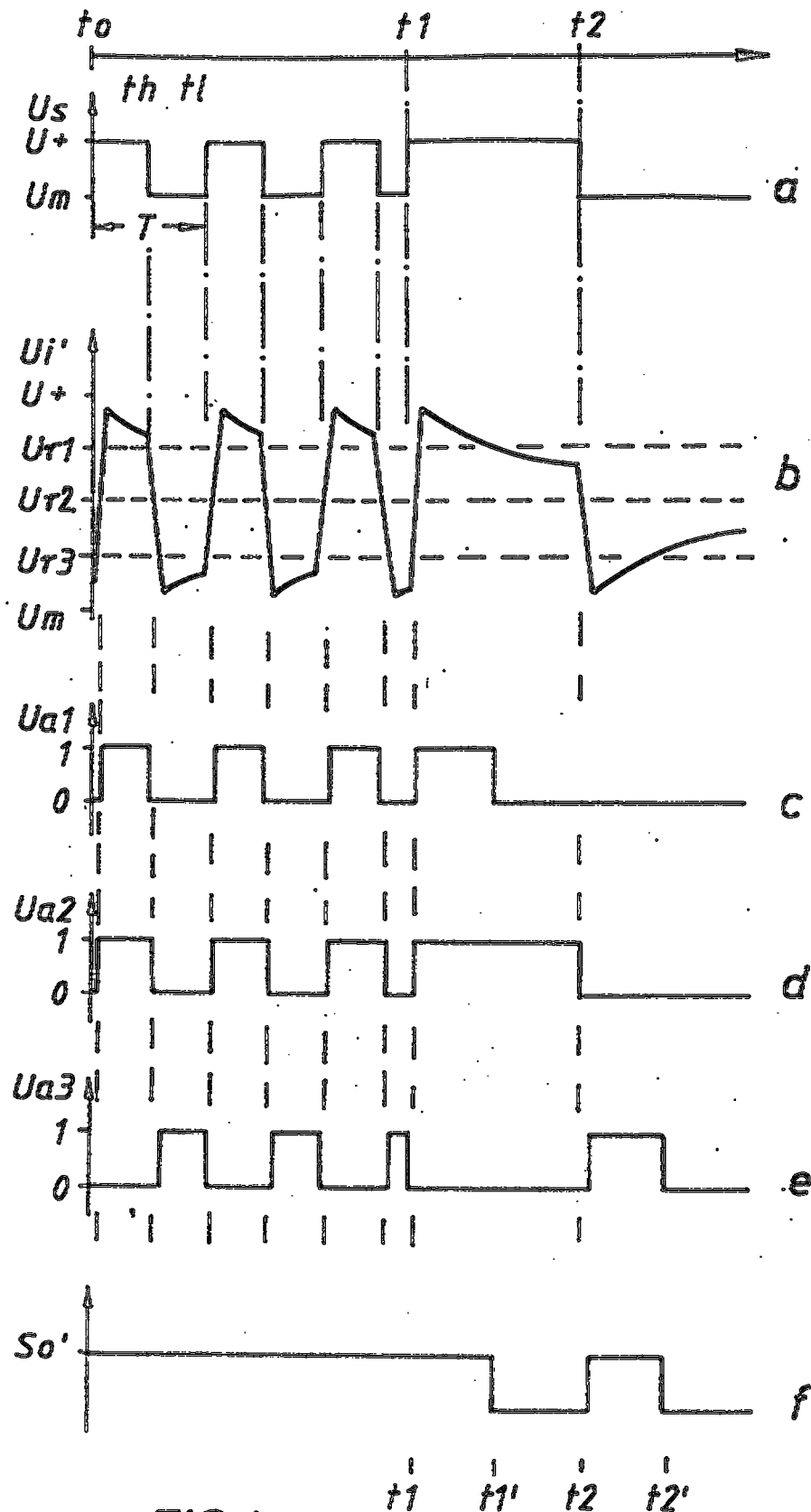


FIG.4

This is the replacement sheet

Date: 17 FEB 1997

REPLACEMENT SHEETS		SG
☒ Description	: paged 1. to paged 13.	
☐ Claim(s)	: paged to paged	
☒ Drawing(s)	: paged 14. to paged 15.	
☐ Abstract	: paged to paged	
DATE OF RECEIPT		2/10/97

**METHOD AND APPLIANCE FOR MONITORING
AN ALTERNATING SIGNAL**

1

THIS SHEET HAS BEEN
REPLACED

The present invention relates to a method of monitoring an alternating signal in accordance with the first part of claim 1 and to an apparatus in accordance with the first part of claim 6.

The use of stages which emit an alternating signal that serves for controlling a stage connected thereto is generally known. Control stages of this type may, for example, incorporate a micro-processor which emits an alternating signal in the form of a digital signal and thereby controls a stage connected thereto. Oscillators are also known which use a sinusoidal, rectangular or some other form of alternating signal for the purposes of processing further signals via appropriate stages.

One can conceive of various ways in which the alternating signal, which is emitted by a control stage of the said type and is also referred to hereinafter as an oscillatory signal, can alter its waveform. Thus, for example, it may happen that there is a shift in potential due to the fact that a dc voltage is superimposed on the oscillatory signal.

Furthermore, it is possible for the duty ratio of the oscillatory signal to alter. In dependence on the equipment in which the control stage is being used, or, in dependence on the operational state, alterations of this type may be wanted or they may point to a defect in the control stage.

The object of the present invention is to monitor the state of an alternating signal in a simple manner.

This object is achieved by means of a method in accordance with claim 1 and by an apparatus in accordance with claim 6.

This Sheet Has Been Replaced



This is the replacement sheet

Date: 02 OCT 1997

In accordance with the invention, an alternating signal, which is produced by a control stage or an oscillator for example, is processed in such a way that signals, which can be evaluated in a simple manner, are produced by comparing the processed signals with reference value signals.

The processing of the oscillatory signal may, for example, be effected in that it is substantially smoothed. The value of the smoothed signal provides a measure for the duty ratio and/or for a possible dc voltage component of the oscillatory signal.

Another way of effecting the processing for example is by conducting the oscillatory signal through a capacitor which is connected in series between a first stage producing the oscillatory signal and a second stage that is controlled by this signal. The first side of the capacitor, which is connected to the second stage, is thereby charged by means of a voltage source, a current source or the like, in such a way that the first side adopts certain voltage values in conformity with a predetermined timing pattern when there is no alteration or there are only very small alterations in the potential on the second side of the capacitor that is connected to the first stage.

It should be pointed out that the alternating signals being used for the control process as well as the signals derived therefrom may be subjected to processing.

A change in the duty ratio and/or of the dc voltage component of the alternating signal may, for example, serve to control a stage connected thereto or else may indicate a functional

This is the replacement sheet

Date: 02 OCT 1997

fault. Thus, for example, in the case of a control stage of the said type, an uncontrolled condition may arise in which the output signal of the control stage corresponds to the dc voltage level of a positive operating voltage or earth potential. This may be caused for example by induced spikes or the like which have an effect upon the running of a control program that is being used for the functional purposes of the control stage. It is likewise conceivable that elements in the control stage are defective, that the supply voltage for the control stage has failed or the like.

In these said cases, there are functional faults in the stages connected to the control stage.

It is an advantage of the present invention that circumstances of this type can be recognised in a simple manner and the stages connected thereto can thereupon be placed in a predetermined state.

An operational monitoring process of this type may be used in the case of an equipment such as a video recorder for example which is driving a tape on which items of information are stored and from which the items of information can be read out.

Further features, advantages and details of the invention will be explained in the following embodiments with the help of the drawing. Therein:

Fig. 1 shows the block circuit diagram of a first embodiment;

This is the replacement sheet

Date: 02 OCT 1997

Fig. 2 the waveforms of the signals in the embodiment of Fig. 1

Fig. 3 the block circuit diagram of a second embodiment;

Fig. 4 the waveforms of the signals in the embodiment of Fig. 3

Before going in detail into the description of the embodiments, it is pointed out that the individually illustrated blocks in the Figures merely serve for a better understanding of the invention. Usually, some or several of these blocks are combined into units. These may be realised using integrated or hybrid techniques or as a program controlled micro-computer or as a part of a program suitable for its control.

However, the elements contained in the individual stages may also be implemented separately.

Fig. 1 shows an electronic control equipment 10 which conveys control signals U_s via a processing stage, which is constructed as a smoothing member 11 in this embodiment, to a controller stage 12 that is supplying current to a motor 13. The smoothing member 11 consists of a resistor 11a whose first terminal is connected to the output of the control equipment 10 and of a capacitor 11b which is connected between the second terminal of the resistor 11a and earth. The smoothing member 11 has the effect of smoothing the control signal U_s whereby a signal U_i is formed. This signal is supplied to the non-inverting (+) inputs of a first comparator 14, a second comparator 15 and a third comparator 16. The comparators 14,

This is the replacement sheet

Date: 02 OCT 1997

15, 16 are connected via their respective inverting (-) inputs to a first reference voltage $Ur1$, to a second reference voltage $Ur2$ and to a third reference voltage $Ur3$. The output signals $Ua1$ and $Ua3$ of the comparators 14, 16 are each supplied to an input of an EXCLUSIVE-OR gate 17 whose output signal So is supplied to further controller means that are supplying current to the motor 13. These further controller means, which incorporate inter alia a power output stage and means for evaluating the signal So and a signal Ss from a start stage 19 and for thereupon controlling the power output stage as described below, are symbolically illustrated in Fig. 1 by the stage 18.

The output signal $Ua2$ from the comparator is extended to the start stage 19 whose output signal Ss is supplied to the stage 18.

The functioning of the embodiment in Fig. 1 will be explained hereinafter with the aid of Fig. 2 only insofar as this is required for an understanding of the present invention.

In order to start the motor 13 running, the control equipment 10 emits the clocked control signal Us which leads to the production of a smoothed signal Ui as is illustrated in Figures 2a and 2b in the time period between $t0$ and $t1$. The signal Ui has a residual ripple which has been drawn in a somewhat exaggerated manner for the purposes of a better understanding. The values of the reference voltages Ur are likewise inscribed in Figure 2b. The comparators emit signals Ua as is shown in Figures 2c) to 2 e).

Initially, we will consider normal operation as occurs during the period of time between t_0 and t_1 . The comparator 15 reproduces, on the basis of the signal U_i , the output signal U_{a2} that has a waveform which corresponds to the clock rate of the original output signal U_s having a duty ratio t_h/t_l over a period T . The signal U_{a1} is "low" i.e. it adopts the digital value "0", and the signal U_{a2} is "high" corresponding to the value "1". Consequently, as is apparent from Fig. 2 f, the output signal S_o of the EX-OR gate 17 is high whereby the operation of the power output stage including the stage 18 is not adversely affected.

In this embodiment, the signal U_s serves not only for initiating the starting of the motor but also for monitoring the operation of the control equipment 10. If, during the operational process, there should be some fault in the control equipment 10 whereby it adopts an operational voltage value that may be U_+ or ground in this embodiment, then the state of the signal S_o from the gate 17 changes and thereby affects the control of the power output stage included in the stage 18.

Next, we will consider a first possible instance of defective operation in the time period between t_1 and t_2 in which the signal U_s adopts the positive operating voltage U_+ whereby U_{a2} is also "high". Since U_+ is greater than both U_{r1} and U_{r3} , the two signals U_{a1} , U_{a3} are "high" and the signal S_o from the gate 17 is "low". This causes the stage 18 to shut down the motor 13 in a predetermined manner from its instantaneous rotational speed to a stand-by speed. This stand-by speed could for example signify that the motor 10 is stopped.

This is the replacement sheet

Date: 02 OCT 1997

A second possible case of fault is illustrated above the time t_2 . Here, the signals U_s and U_i are considered to have adopted the value of earth potential. Since this lies below both U_{r1} as well as U_{r3} , the signals U_{a1} and U_{a3} are "low". Hence, S_o is also "low" and the stand-by mode is maintained.

The cases illustrated in Fig. 2 represent a special instance insofar as the first case of a fault ($t_1 - t_2$) occurs first and the second case of a fault (after t_2) follows thereon. Naturally, it is possible for the signal U_i to drop to earth potential immediately after the normal mode of operation. The stand-by mode will thereby be initiated in a corresponding manner in that the motor 13 will be shut down.

In the description of this embodiment, it was initially assumed that the signal U_s was keyed between the two values U_+ , U_m of the operating voltages. It is also possible however that a lesser voltage range is provided for the signal U_s . In this case, the circuit of Fig. 1 can also be used for the purposes of determining the existence of a possible dc voltage component in the signal U_s .

The block circuit diagram of a second embodiment is illustrated in Fig. 3 and this will be explained with the help of Fig. 4. Means and signals having analogous functions as in the embodiment of Fig. 1 are referred to in Fig. 2 in the same manner as there. They will only be gone into hereinafter insofar as this is essential for an understanding of the present invention.

The basic difference relative to the embodiment of Fig. 1 is that another form of processing of the signal U_s occurs. This

This is the replacement sheet

Date: 02 OCT 1997

is not performed by the smoothing member 11 but by means of a capacitor 20 which is connected in series with a resistor 21. A signal U_i' is tapped from the connection between the elements 20, 21 and supplied to the comparators 14, 15, 16. In the case of the comparators 14 and 15, the signal U_i' is thereby applied to the respective non-inverting input and, in the case of the comparator 16, to the inverting input. The resistor 21 is connected to the centre tap of a voltage divider which is formed by resistors 22, corresponding to 22a - 22d, and serves for producing the reference voltages U_{r1} , U_{r2} , U_{r3} which are respectively present on the free inputs of the comparators 14 - 16. The output signals U_{a1} and U_{a3} are supplied to the OR gate which is referenced here by 17' since, in this embodiment, it may be implemented in the form of a "simple" OR gate and does not necessarily have to be an EXCLUSIVE-OR GATE. In a preferred embodiment, the gate 17' is realised by two diodes which are respectively connected after the comparators 14 and 16 in their forward conduction directions as is indicated within the block 17'.

A capacitor 23 is connected after the gate 17, this having the effect that in the case of short-term excursions of the signal U_s these will not be of significance for the stage 18.

Figures 4a and 4b show the waveform of the signals U_s and U_i' . In the event of a change of U_s from "low" to "high", the right-hand side of the capacitor 20 (see Fig. 3), from which the signal U_i' is taken, will be recharged in a finite time i.e. only in an approximation to a jump, to a voltage whose value is close to the positive supply voltage U_+ of the control equipment 10. As long as U_s remains "high", the right-hand side of the capacitor discharges exponentially via the

This is the replacement sheet

Date: 02 OCT 1997

resistor 21 towards the reference voltage U_{r2} which is taken from the centre tap of the voltage divider.

The values of the elements 20, 21 are selected in such a way that the signal $U_{i'}$ does not fall below the first reference value U_{r1} or does not exceed the third reference value U_{r3} during the time periods t_h and t_l in which the signal U_s is respectively "high" and "low" in normal operation.

Consequently, in the normal mode, the first output signal U_{a1} is "high" (see Fig. 2c) during the time periods t_h and the third output signal U_{a3} is "low" (see Fig. 2e).

It should be noted at this point, that the perpendicular guide lines in Fig. 4, which are shown dashed or as dash-dotted lines, have the following significance: the dash-dotted lines mark the respective time points at which the signal U_s alters its state. The dashed lines mark those particular time points at which the signal $U_{i'}$ falls below or exceeds the second reference value U_{r2} and at which the signal U_{a2} alters its state accordingly. The gate transit times have been neglected here.

In the event of a change of the signal U_s from "high" to "low", the signal $U_{i'}$ falls at finite speed to a value which nearly corresponds to that of the earth potential U_m . The exponential voltage waveform on the right-hand side of the capacitor again goes towards U_{r2} but, in so doing, the third reference voltage U_{r3} is not exceeded in normal operation.

Due to the waveform of the signal $U_{i'}$ as is illustrated in Fig. 2b in the time period t_0 to t_1 , the effect is that one of the output signals U_{a1} , U_{a2} will always be "high" if one

This is the replacement sheet

Date: 02 OCT 1997

initially neglects the fact that the signal U_i' does not follow at an arbitrary rate when U_s is subjected to a jump in voltage. As a consequence, the output signal S_o of the gate 17 is "high" during normal operation. However, as has already been indicated, since U_i' only rises or falls at a finite speed, one has to reckon on short-term drops in the signal S_o . These, however, are smoothed by the capacitor 23 in such a way that they are not of significance for the stage 18 and one can therefore dispense with the need to make allowance for such jumps in Fig. 4f.

In the implementation of the OR gate 17', one has to take into consideration that any discharge of the capacitor 23 should be avoided during the short-term falls of its output signal. This is achieved for example by the implementation of the gate 17' by means of the two diodes which are inscribed in the block 17'. It is also possible to use another type of OR gate such as is implemented for example by a TTL gate. However, an additional diode between the output of the gate 17' and the capacitor 23 may then be needed.

If there is a departure from normal operation at a time point t_1 , in that the signal U_s adopts a constantly "high" value, then the exponential fall in voltage on the right-hand side of the capacitor leads to the voltage dropping below the first reference voltage U_{r1} at the time point t_1' . Thereupon, apart from the third output signal U_{a3} , the first output signal U_{a1} will also be "low" and hence too, the gate output signal S_o . This is detected by the stage 18 which thereupon controls the power output stage contained therein in such a way that the motor 13 is shut down to a stand-by speed.

This is the replacement sheet

Date: 02 OCT 1997

In the event of an operational fault, in which the signal U_s constantly adopts earth potential as is intended to occur from a time point t_2 , U_i' initially falls below the value of the two reference voltages U_{r1} , U_{r3} whereby normal operation is simulated for a short time by virtue of the gate signal S_o . However, the reference value U_{r3} is exceeded as from the time point t_2' and an operational fault is detected.

The advantage of the embodiment of Fig. 2 vis a vis that of Fig. 1 lies particularly in that it provides a greater degree of certainty in monitoring the operation even in the case where there are differing operating voltages U_+ , U_+' for the control equipment 10 and the controller stage 12. In the event that the second reference voltage U_{r2} has a value of 2.5 volts and the other two reference voltages U_{r1} , U_{r3} are symmetrically disposed around this value then functional faults will occur in Fig. 1 if the operating voltage U_+ of the control equipment 10 amounts to 2 volts or 10 volts for example and the control signal U_s is caused to vary between U_+ and earth. One can reckon with functional faults in the case of the embodiment in accordance with Fig. 1 even when there are only very small deviations between the respective operating voltages, but this is not so in the case of the circuit of Fig. 3.

In the case of one development of the embodiment in accordance with Fig. 3, the charging of the right-hand side of the capacitor can be effected by means of a controlled current source. This is connected, for example, directly between the right-hand side of the capacitor and an operating voltage such as U_+' or earth and may be controlled by a comparison signal whose value provides a measure for the voltage difference

This is the replacement sheet

Date: 02 OCT 1997

between the voltage present on the right-hand side of the capacitor and a reference voltage such as the second reference voltage U_{r2} for example. A desired timing waveform for the voltage on the right-hand side of the capacitor can be set in dependence on the current source and the said comparison signal. The waveform may be exponential, linear or follow any other form of function.

Other versions of the embodiments may comprise at least one of the following variations:

- the signal U_s may be divided into a first signal which serves for controlling the stage 18 and which can be directly supplied thereto and into a second signal which serves for monitoring the alternating signal U_s . In this case, a second supply lead for the circuit 12 is necessary but the comparator 15 can be dispensed with;

- by suitably selecting the value of the reference voltage U_r , one can not only detect when the signal U_s adopts a dc voltage value but one can also detect whether a predetermined duty ratio is being exceeded or not being reached;

- more than three reference voltages may be provided.

Corresponding dc voltage components can thereby be detected for example and further functions of the circuit 12 can thereupon be controlled with the use of only one connecting lead. If the signal U_s is formed as a pulse width modulated signal (PWM), it is also possible to detect the corresponding values of the duty ratio in correspondence with the number of reference voltages. This can be used for monitoring the operation of a load such as the motor 13. Particular reference

This is the replacement sheet

Date: 02 OCT 1997

is made at this point to the earlier applications P 42 27 761.2 in which the detection of the value of a current, with which a PWM load is controlled, is described and P 42 29 344.8 in which a load is controlled in dependence on a temperature;

- once a case of a fault has been detected and in the event that a normal case is subsequently detected, the stage 18 may automatically return a following load, such as the motor 13 for example, to normal operation or else provision may be made for this to occur only after the reception of a confirmatory signal which is emitted by not-illustrated means or by someone using the system whose functioning is being monitored;
- the embodiments may be employed as part of a video recorder, a compact disk (CD) player or any other type of equipment including a motor;
- instead of an equipment including a motor, the functioning of other equipment or systems may be monitored in the manners described;
- instead of monitoring a function, the manner in which the control signals are converted into U_i or U_i' and the subsequent evaluation thereof may also be used for controlling other functions.

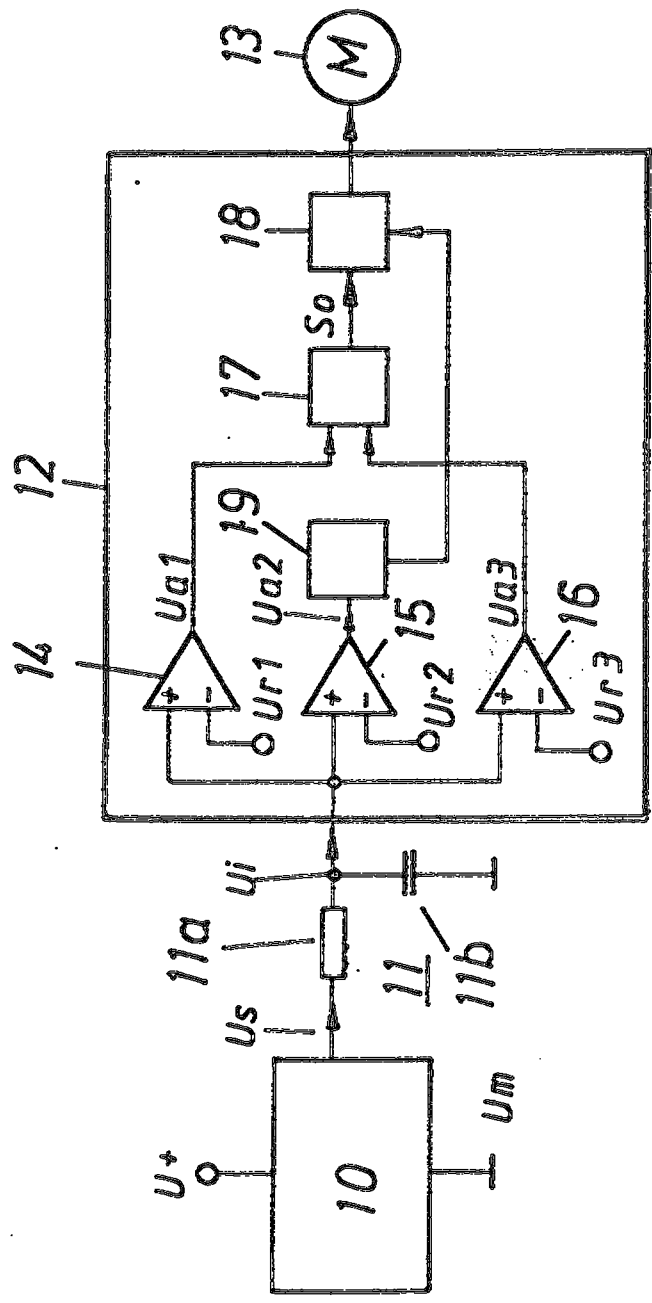


FIG.1

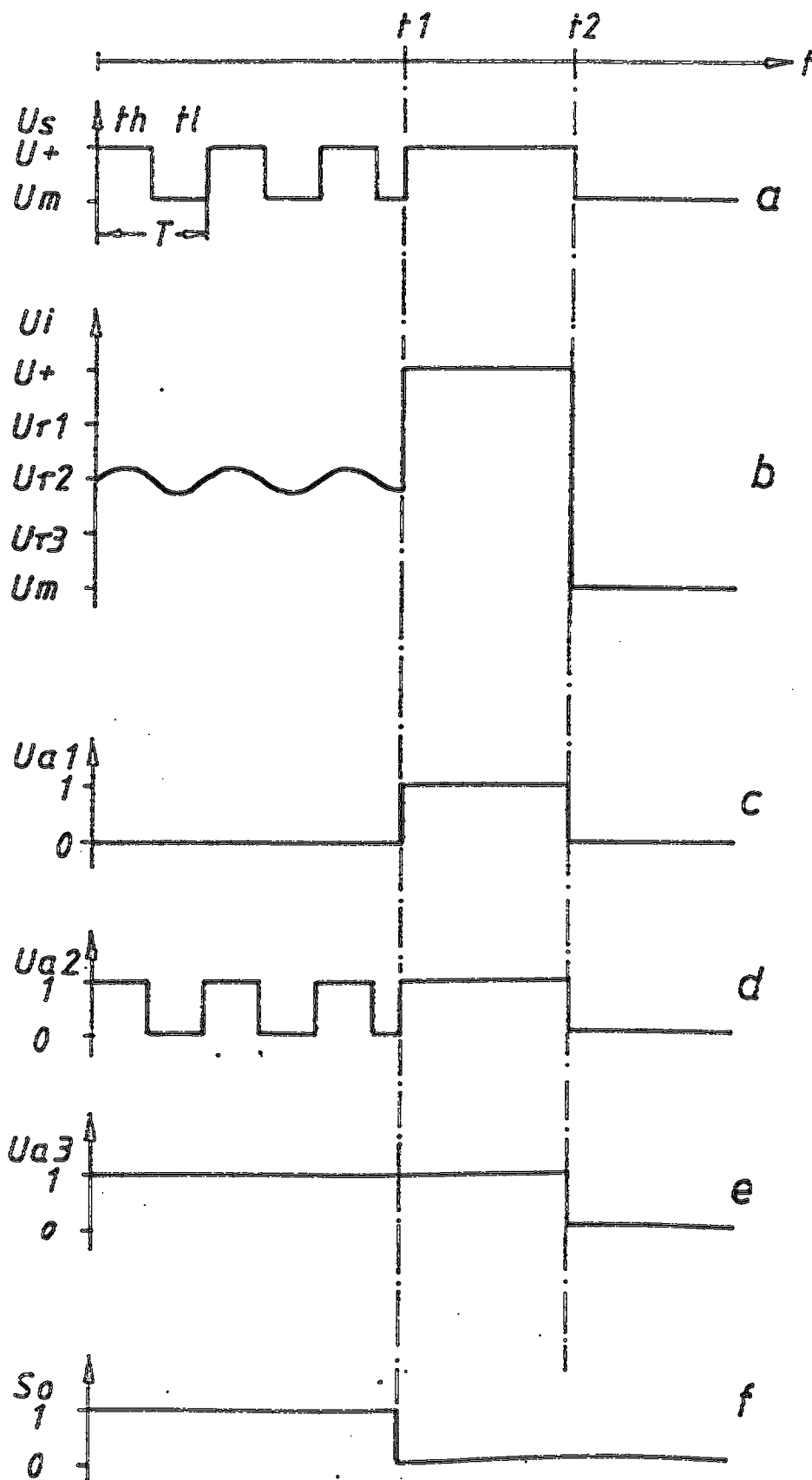


FIG. 2

This is the replacement sheet

Date: 02 OCT 1997

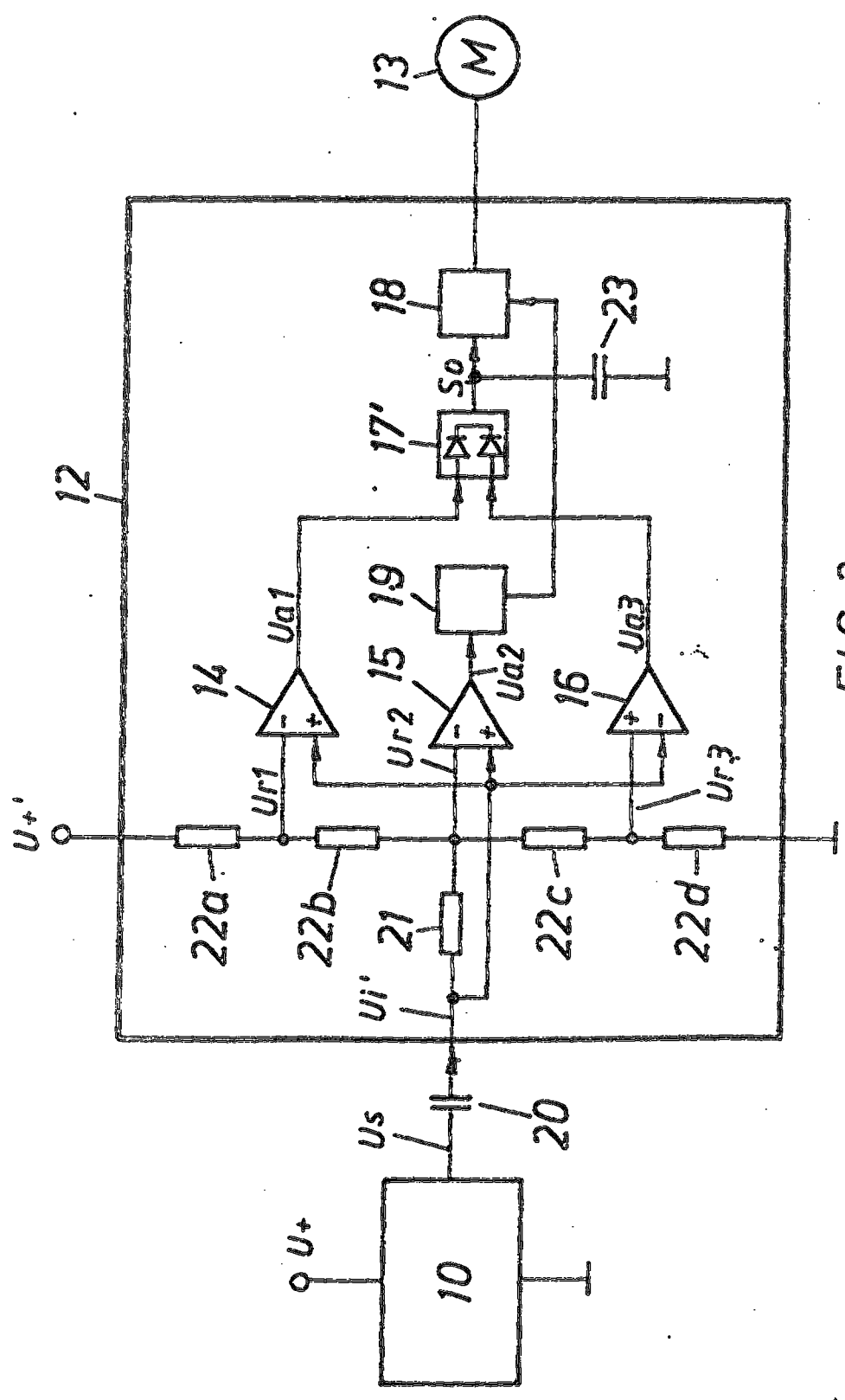


FIG. 3

REPLACEMENT SHEETS		50
☒ Description	: paged ...1. to paged ...	
☒ Claim(s)	: paged ...4. to paged ...6.	
☐ Drawing(s)	: paged to paged	
☒ Abstract	: paged ...7. to paged ...	
DATE OF RECEIPT <u>3/4/99</u> <u>AN ALTERNATING SIGNAL</u>		

- 1 -

REPLACEMENT SHEET

METHOD AND APPLIANCE FOR MONITORING

The present invention relates to a method of monitoring an alternating signal in accordance with the first part of claim 1 and to an apparatus in accordance with the first part of claim 6.

The use of stages which emit an alternating signal that serves for controlling a stage connected thereto is generally known. Control stages of this type may, for example, incorporate a micro-processor which emits an alternating signal in the form of a digital signal and thereby controls a stage connected thereto. Oscillators are also known which use a sinusoidal, rectangular or some other form of alternating signal for the purposes of processing further signals via appropriate stages.

One can conceive of various ways in which the alternating signal, which is emitted by a control stage of the said type and is also referred to hereinafter as an oscillatory signal, can alter its waveform. Thus, for example, it may happen that there is a shift in potential due to the fact that a dc voltage is superimposed on the oscillatory signal.

Furthermore, it is possible for the duty ratio of the oscillatory signal to alter. In dependence on the equipment in which the control stage is being used, or, in dependence on the operational state, alterations of this type may be wanted or they may point to a defect in the control stage.

The object of the present invention is to monitor the state of an alternating signal in a simple manner.

This object is achieved by means of a method in accordance with claim 1 and by an apparatus in accordance with claim 6.

This is the replacement sheet

Date: 03 APR 1999

**Claims**

1. Method of monitoring an alternating signal (U_s) for a motor control system, characterised in that,
 - the alternating signal (U_s) is processed in such a way as to produce a processed signal (U_i ; U_i') whose timing waveform provides a measure for the duty ratio and/or for a possible dc voltage component of the alternating signal, that
 - the processed signal (U_i ; U_i') is compared with at least two predetermined reference values (U_{r1} , U_{r3}) whereby corresponding comparison values (U_{a1} , U_{a3}) are produced and that
 - the duty ratio and/or the dc voltage component of the alternating signal is determined on the basis of the comparison values (U_{a1} , U_{a3}) in that the comparison values (U_{a1} , U_{a3}) are combined with one another using an EXOR or an OR function.
2. Method in accordance with Claim 1, characterised in that, the alternating signal (U_s) is processed in that it is smoothed whereby the processed signal (U_i) comprises a dc voltage component whose value provides a measure for the duty ratio and/or for the dc voltage component of the alternating signal (U_s) and may comprise an ac voltage part having a predetermined amplitude whereby the alternating signal (U_s) can, where necessary, be regenerated (U_{a2}) from the ac voltage component.
3. Method in accordance with Claim 1, characterised in that, the alternating signal (U_s) is processed in that a signal derived therefrom is subjected to a voltage in such a way that, following any change in the



voltage of the alternating signal (U_s), the derived signal moves towards a predetermined voltage value (U_{r2}) in a predetermined timely manner.

4. Method in accordance with any of the Claims 1 to 3, characterised in that, a control signal (S_0), whose value provides a measure for a possible operational fault, is formed on the basis of the comparison signals (U_{a1} , U_{a3}).
5. Method in accordance with any of the Claims 1 to 4, characterised in that, means (13), which can be controlled with the aid of the alternating signal, are regulated down to a quiescent operational level (standby mode) on the basis of the values of the comparison signals (U_{a1} , U_{a3}).
6. Apparatus for monitoring an alternating signal (U_s) for a motor control system which is produced by generator means (10), characterised in that,
 - there is provided a processing stage (11; 20, 21) which processes the alternating signal (U_s) in such a way as to produce a processed signal (U_i ; U_i') whose timing waveform provides a measure for the duty ratio and/or for a possible dc voltage component of the alternating signal, that
 - there are provided comparison means (14, 16) which compare the processed signal (U_i ; U_i') with at least two predetermined reference values (U_{r1} , U_{r3}) whereby corresponding comparison values (U_{a1} , U_{a3}) are produced and that
 - there are provided EXOR or OR gates (17, 17') which determine the duty ratio and/or the dc



voltage component of the alternating signal on the basis of the comparison values (U_{a1} , U_{a3}).

7. Apparatus in accordance with Claim 6, characterised in that, the processing stage includes smoothing means (11) which smooth the alternating signal (U_s) in such a way that the processed signal (U_i) comprises a dc voltage component whose value provides a measure for the duty ratio and/or the dc voltage component of the alternating signal (U_s) and may comprise an ac voltage part having a predetermined amplitude whereby the alternating signal (U_s) can, where necessary, be regenerated (U_{a2}) from the ac voltage component.
8. Apparatus in accordance with Claim 6, characterised in that, the processing stage comprises a capacitor (20) which is connected by its first terminal to the generator (10) and that there is provided a voltage or current device (21, 22) which charges or discharges the second terminal using a predetermined current whereby a processed signal (U_i) is produced, which signal, following any change in the voltage of the alternating signal (U_s), moves towards a predetermined voltage value (U_{r2}) in a predetermined timely manner.
9. Apparatus in accordance with any of the Claims 6 to 8, characterised in that, evaluating means (17) form a control signal (S_o), whose value provides a measure for a possible operational fault, on the basis of the comparison signals (U_{a1} , U_{a3}).
10. Apparatus in accordance with any of the Claims 6 to 9, characterised in that, means (13), which can be controlled with the aid of the alternating signal, are regulated down to a quiescent operational level (standby mode) on the basis of the values of the comparison signals (U_{a1} , U_{a3}).

METHOD AND APPLIANCE FOR MONITORINGAN ALTERNATING SIGNAL

ABSTRACT

It is the object of the present invention to monitor the state, such as the clock ratio or DC component, of an alternating signal.

According to the invention, the alternating signal to be monitored is conditioned in such a way that, by means of a simple comparison with reference voltages, it is possible to draw conclusions about the clock ratio or a DC component. As a result, for example, various information can be transmitted over one feed line. It is also possible to monitor the operating state of the stage generating the alternating signal.

The invention may be used, for example, for operational monitoring of a video recorder.

Fig. 1.

This is the replacement sheet

Date: 03 APR 1989