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(54) Title: MECHANISM TO ACCELERATE GRAPHICS WORKLOADS IN A MULTI-CORE COMPUTING ARCHITECTURE

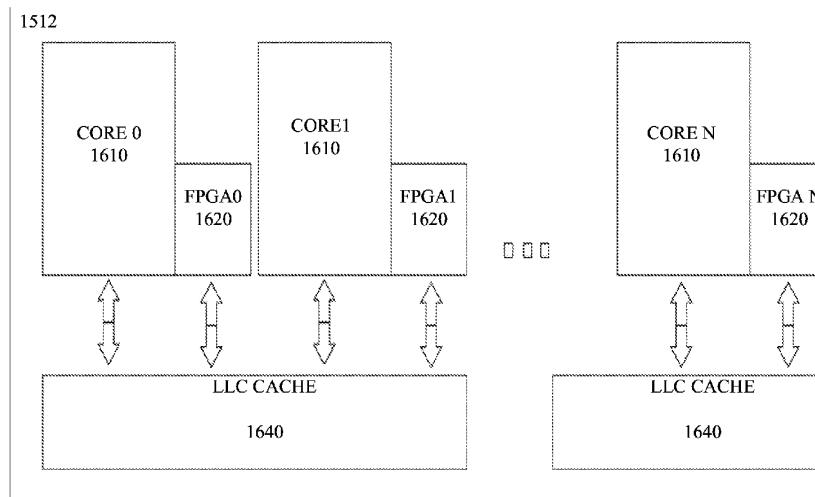


FIG. 16A

(57) Abstract: A processing apparatus is described. The apparatus includes a plurality of processing cores, including a first processing core and a second processing core a first field programmable gate array (FPGA) coupled to the first processing core to accelerate execution of graphics workloads processed at the first processing core and a second FPGA coupled to the second processing core to accelerate execution of workloads processed at the second processing core.

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