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PROCESS FOR MAKING FINE PITCH CONNECTIONS BETWEEN DEVICES AND STRUCTURE MADE BY THE PROCESS

FIELD OF THE INVENTION

This invention relates to manufacturing of integrated circuit devices. More particularly, this invention relates to a process for interconnecting multiple devices (generally with different sizes, architectures and functions) at close proximity and with a very high wiring density.

BACKGROUND OF THE INVENTION

The need for greater functionality and performance in semiconductor devices has resulted in the development of larger and more complex chips. In addition, it is often desirable to include several different functions on a single chip to obtain a "system on a chip," which generally requires both an increased chip size and a more complicated manufacturing process. These factors both tend to depress manufacturing yield. It is estimated that many such complex chips, with areas greater than 400 mm^2, will generally have very poor manufacturing yield (perhaps under 10%).

One method of maintaining acceptable yields is to manufacture smaller chips, and then to interconnect those chips on a single substrate or chip carrier. Besides improved manufacturing yield, another major advantage of this approach is that the individual chips may be of different sizes, perform different functions, or be fabricated by different or

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incompatible methods. A conventional method of joining a semiconductor device to a carrier involves the use of controlled-collapse chip connections (C4s). For example, U.S. Patent No. 4,489,364, assigned to International Business Machines Corporation, discloses a ceramic chip carrier for supporting an array of chips by means of solder balls, such as C4s, to form a multichip module (MCM). As an example, as shown in Figure 1, four separate chips 10 are mounted on a carrier 11; the carrier includes the wiring necessary to interconnect the chips. A C4 chip/carrier joining method typically requires an array of pads of about 100 μm diameter, with the pads at approximately a 200 μm pitch. Such MCMs tend to be expensive, due to their multilayered ceramic structure, and require significantly more area than the combined area of the chips. For devices which require a joining pitch below 150 μm, another method must be used.

To realize the advantages offered by the system-on-a-chip (SOC) concept, it becomes necessary for all of the different chip functions to be in very close proximity and have very precise alignment with respect to each other. The alignment and interconnection should also be performed with minimal added complexity in the overall process. In the case of an SOC, the interconnections should be made on top of the chips rather than in the chip carrier substrate.

There remains a need for a process for fabricating a device having a dense arrangement of chips and a high wiring density of chip-to-chip interconnections which can be practiced with high manufacturing yield.

SUMMARY OF THE INVENTION

The present invention addresses the above-described need by providing a method for fabricating a semiconductor device

including a chip, in which very fine-pitch connections are made between chips by using matching stud/via structures.

According to a first aspect of the invention, a stud is provided on a first surface of a chip (the surface closest to the active area), and a first layer is formed on a plate which is transparent to ablating radiation. The first layer includes a conducting pad on a surface of the layer opposite the plate, and generally has electrical wiring therein for device interconnection. A second layer is formed on that surface of the first layer, and a via is formed in the second layer to expose the conducting pad; the alignment substrate, the first layer and the second layer form a temporary alignment structure. The stud on the chip surface is then aligned and inserted into the via, and the chip is attached to the alignment structure. The first surface of the chip thus contacts the second layer and the stud makes electrical contact with the conducting pad (so that a stud/via connection is made). A support is then attached to the chip (or array of chips) on the backside thereof. The interface between the first layer and the transparent plate is ablated using ablating radiation (typically laser radiation) transmitted through the plate, thereby detaching the plate.

The chip (or chip array) and the alignment structure may be fully bonded by performing a lamination process. To ensure thermal conductivity from the chip to the support material, the support may be attached by forming an alloy between metal layers deposited on the backside of the chip and on the top surface of the support. Alternatively, the chip array and support may be attached by forming stud/via connections (e.g. studs on the back surfaces of the chips with vias formed in a layer deposited on the support). If the chips are of different thicknesses, the chips are planarized (typically by grinding and/or chemical-mechanical polishing) before the support is attached.

The detaching and removal of the transparent plate exposes a surface of the first layer. In order to permit interconnection with other carriers, connection pads such as C4 pads are formed on this surface.

According to a second aspect of the invention, a stud is provided on the first layer formed on the transparent plate, while a via is formed in a second layer on the first surface of the chip. The stud is aligned to the via, and the chip is attached to the alignment structure so that the first layer contacts the second layer and the stud makes electrical contact with the conducting pad.

After the stud and via are aligned, the chip and the alignment structure may be bonded by a lamination process, as noted above. The support substrate may also be attached by metallizing the chip and support and forming an alloy therebetween, or by making stud/via connections. If the chips are of different thicknesses, the chips are planarized. A backside support is then attached to the chip (or array of chips). The interface between the first layer and the transparent plate is ablated using ablating radiation transmitted through the plate, thereby detaching the plate.

According to another aspect of the invention, a semiconductor device is provided which includes a plurality of chips. A support is attached to the chips on the back surfaces thereof. A first layer is disposed on the front surfaces of the chips; this layer has a plurality of vias formed therein and conducting pads in registration with the vias. A plurality of studs, corresponding to the vias, are disposed in the vias. A second layer is attached to the first layer on a surface of the first layer opposite the front surfaces of the chips. This second layer is aligned to the first layer by the studs in the vias. The second layer includes electrical wiring connecting to the chips through the studs and the conducting pads.

The electrical wiring in the second layer makes electrical

connections between the chips. The stud/via structures may be formed either with the studs in contact with the front surfaces of the chips or with the studs in contact with the second layer.

The support may be attached to the back surfaces of the chips by a metal alloy layer, or by a layer which includes stud/via structures. Electrical connection pads (such as C4 pads) may be provided on the second layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a chip carrier on which four individual chips are mounted and through which the chips are interconnected.

Figure 2A is a schematic cross-sectional view of a semiconductor device or chip, according to a first embodiment of the invention.

Figure 2B is a schematic cross-sectional view of a temporary structure including a transparent plate for aligning and attaching the chip, according to the first embodiment of the invention.

Figures 3A-3E illustrate steps in a fabrication process for a device having a dense arrangement of chips, in accordance with the first embodiment of the invention.

Figures 4A-4C illustrate an alternative method of attaching the chip support shown in Figure 3E.

Figure 5 illustrates the use of ablating radiation to detach the transparent plate.

Figures 6A and 6B illustrate further steps in the fabrication process according to the first embodiment of the invention, after removal of the transparent plate; Figures 6A and 6B show chip supports attached as in Figures 3E and 4C, respectively.

Figures 7A and 7B are schematic cross-sectional views of a chip and temporary alignment structure, respectively, according to a second embodiment of the invention.

Figures 8A-8C illustrate steps in a fabrication process for a device having a dense arrangement of chips, in accordance with the second embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In accordance with the present invention, a semiconductor device including a chip is fabricated using stud/via connections, as detailed below.

In the first embodiment of the invention, chip 2 has metal studs 20 formed on the terminal surface 2a (see Figure 2A). Studs 20 may be formed of Ni, Cu, Ni-plated Cu, W or some other metal or combination of metals. It is understood that the active areas of chip 2 are close to surface 2a; some material will be removed from the back surface 2b in a later processing step. The studs 20 protrude from surface 2a a distance which typically is 5 μm or less. A layer 21 of a low-melting-point alloy material is deposited on the surface of the stud; this facilitates formation of an electrical connection during the joining process. This material is typically 90/10 Pb/Sn solder, 2 μm or less thick; alternative alloy materials include Au/Sn and Sn/Ag. The alloy material may be subjected to a thermal reflow process so that layer 21 acquires a rounded shape, as shown in Figure 2A; this facilitates alignment of the studs on the chip to vias on the alignment structure.

Figure 2B shows the structure of a temporary alignment structure 12, according to the first embodiment of the invention. The temporary alignment structure 12 includes a transparent plate 22 (such as boro-float glass from Schott Glasses). At this stage in the process, the transparent plate

22 has various layers disposed thereon; plate 22 is separated from those layers at a later stage of the process. Dielectric layer 23 (typically polyimide), on top of plate 22, has embedded therein high-density wiring 24 (generally several levels of Cu conductors, as shown schematically in Figure 2B), and has electrical joining pads 25 on the surface 23a opposite plate 22. Although layer 23, including the conductors, is shown as a single layer, it will be appreciated that for ease of manufacturing it is often designed and fabricated as a multilayer structure. Pads 25 are typically Ni, but may also be Cu, Au, Co or a combination thereof. A dielectric layer 26 overlies the wiring layer 23; layer 26 may be formed of a polyimide material typically used in thin film packaging processing.

Layer 26 has vias 27 formed therein (e.g. by reactive-ion etching or by an excimer laser), so that a terminal metal joining pad 25 is at each via bottom. The thickness of layer 26 (and hence the depth of the vias 27) is chosen to match the height of the studs 20.

As shown in Figure 2B, the vias may be formed with a sloped wall angle as a guide for high-accuracy, self-aligned placement of the studs 20 in the vias 27. The wall angle of the via may be tailored to be either near-vertical or sloped. A near-vertical profile can be obtained if the vias are formed by RIE. It has been noticed that stud/via alignment is readily accomplished when the wall angle is 65°; a via with this wall angle may conveniently be obtained when an excimer laser is used to form the via.

A thin coating 28 of thermoplastic polymer adhesive (such as Kapton-KJ® from Dupont) may be deposited on the top of the dielectric layer 26, to ensure reliable bonding to the chip surface 2a. Alternatively, the entire layer 26 may be formed of adhesive material. An adhesive layer may be deposited on surface 2a of chip 2 in addition to, or instead of, layer 28.

The process for aligning and mounting multiple chips 2 to the alignment structure 12, in accordance with the first embodiment of the invention, is shown in Figures 3A-3G. The chips are aligned to the alignment structure 12 by placing studs 20 in corresponding vias 27. As is understood by those skilled in the art, an automated alignment tool may be used to align the chips to the alignment structure; if such a tool is used, the matching of the stud pattern to the via pattern can be made with a pitch of as little as 2 μm. Alternatively, the alignment may be done optically, by viewing an alignment mark on surface 2a of chip 2 through the transparent plate 22; in that case a viewing hole must be formed in layers 23 and 26. Since the system may be built from chips having different functions and originating from different device wafers, adjacent chips may have different thicknesses, as shown in Figure 3A.

Each chip 2 may be temporarily held in position relative to the alignment structure 12, while alignment and placement of other chips is performed. This may be done by using focused infrared heating to melt solder on a selected stud (e.g. solder 21t on stud 20t), thereby "spot welding" the stud to the corresponding joining pad 25t. It will be appreciated that such heating should be performed outside an active device area of the chip, as heating through the device area should be avoided. Adhesive or solder fuses may also be used at specified locations on the front surface 2a of the chip, so that the chip is temporarily held to corresponding portions of the alignment structure.

Alternatively (even if adhesive layer 28 is not used), chip 2 may be temporarily held in position by performing the alignment procedure at an elevated temperature, so that the surface of polyimide layer 26 is slightly "tacky" before being brought into contact with surface 2a of chip 2.

After all of the chips 2 have been aligned and temporarily

held or "tacked" to the alignment structure, a lamination process is performed to permanently attach the chips to layers 23 and 26 (see Figure 3B). The lamination process is typically performed at elevated temperature and pressure, to ensure (1) stud/via registration; (2) vertical metal bonding between the studs 20 and via joining pads 25; and (3) bonding of the chips 2 to layer 26 (and to any material therebetween). Depending on the materials used, the temperature may be in the range 200 °C - 400 °C and the pressure may be in the range 10 psi - 200 psi. As shown in Figure 3B, the lamination process causes the solder 21 to flow so that solder either partially or completely fills via 27.

To build a dense array of chips (so as to arrive at an optimum performance integrated system-on-a-chip structure), it is desirable that the gaps 30 between adjacent chips be as narrow as possible (see Figures 3A and 3B). The minimum gap width (and hence the chip density) depends on the gap filling technique. Gaps having a width of about 60 μm may be filled with polyimide by dispensing the polyimide with a MicroPen™, manufactured by OhmCraft™ of Honeoye Falls, NY.

After the lamination process, the gaps 30 between chips are fully or partially filled with a suitable material 31, such as thermoset epoxy or another organic material (Figure 3C). Since the different chips will typically have their thicknesses reduced and preferably made uniform in a later processing step, the gaps 30 need only be filled to a level matching their eventual uniform thickness.

The chips are then thinned and planarized to have a uniform thickness, preferably by grinding and chemical-mechanical polishing (CMP) of their back surfaces 2b. As shown in Figure 3D, the result of this process is that the various chips have a uniform planar back surface 2p with respect to each other.

A chip support 32 (typically a Si wafer) is then bonded to

the planarized back surface 2p of the chips, as shown in Figure 3E. If the system has only low-power (~ 1 W) chips, this bonding may be performed using an insulating adhesive.

However, if the system includes high-power chips, it is necessary to allow for heat transfer away from the chips; the bonding material must then be thermally conductive. A thermally conductive bond between chips 2 and support 32 may be obtained by a metal alloying process, in which an alloy is formed between metallized surfaces of the planarized chips 2 and the chip support 32. To create this conductive layer, the chip support 32 is first coated with a layer 33 to ensure adhesion of the conductive layer to the chip support surface; for example, this layer may be a Ti/TiN combination or TiW. A similar layer 34 is deposited on the back surface 2p of the chips. The two layers 33, 34 are then placed together facing each other, with an alloying layer 35 placed between them (see Figure 3E). Alloying layer 35 is preferably a metal (e.g. Sn) or combination of metals (e.g. Au-Sn) which permits bonding below 400 °C, in order to be compatible with previously processed materials. Using a slightly crushable Sn foil between the two layers 33, 34 ensures good mechanical contact before alloying. Alternatively, an additional layer with suitable eutectic properties may be deposited on each bonding layer 33, 34, and the two surfaces then brought into direct contact. Applying a heat treatment (below 400 °C) results in formation of an alloy between layer 35 and each of layers 33 and 34. Another low cost alternative, which is known in the art, is to coat one surface with Au or Au/Si which becomes a bonding layer at 400 °C.

An alternative process for obtaining a thermally conductive bond between chips 2 and support 32 is shown in Figures 4A-4C. This process uses a stud/via matching technique, similar to that described above. Metal studs 40 are formed on the planarized surface 2p of the chips. These studs

may be the same metal as studs 20, or may be of Cu to ensure thermal conductivity. A layer of solder 41 may be applied to the surface of the stud. Chip support 32 has conducting pads 45 deposited thereon, with a polyimide layer 46 overlying the pads (Figure 4B). The polyimide layer 46 has vias 47 formed therein to expose pads 45. The studs 40 on chips 2 are then aligned to the vias 47, and a lamination process is performed to permanently attach the chip support 32 (Figure 4C). As shown in Figure 4C, the size and pitch of studs 40 and vias 47 may be much greater than those of the wiring interconnection studs 20 and vias 27.

It will be appreciated that a stud/via connection between the support 32 and chips 2 may also be realized by reversing the positions of studs and vias shown in Figures 4A-4C; that is, studs 40 may be formed on support 32 while conducting pads 45 and layer 46 are deposited on planarized surface 2p.

It should be noted that the chip support 32 can be of any convenient size and shape to accommodate the chips. In particular, if the chips are generally rectangular, the substrate may also be rectangular.

The structure shown in Figure 3E (alternatively, Figure 4C) is then subjected to a laser ablation process. Laser radiation 36, incident on surface 22a of transparent plate 22, penetrates the plate and ablates the interface between the plate and the polyimide of layer 23 (Figure 5). This results in delamination of the plate from layer 23, so that plate 22 may be removed. The chip support 32 thus becomes the support for the chips, the wiring layer, and the stud/via connections therebetween.

With plate 22 removed, surface 23b of layer 23 is exposed. C4 pads 37 are then formed on this surface (or are exposed if already present), so that the interconnected chips may be joined to an appropriate carrier. The device then appears as shown in Figure 6A, if the chip support 32 is attached using a

metallization and alloying process (see Figure 3E). Alternatively, if a stud/via connection process is used to attach chip support 32 (see Figures 4A-4C), the device appears as shown in Figure 6B. It should be noted that the size and pitch of the C4 pads 37 is much greater than that of the studs 20 or vias 27.

In a second embodiment of the invention, a similar stud/via joining process is used to join the chips and the wiring layer, but the positions of studs and vias are reversed. As shown in Figure 7A, chip 2 has disposed thereon conducting pads 55, dielectric layer 56 with vias 57, and thermoplastic adhesive layer 58. Temporary alignment structure 12, including transparent plate 22 and high-density wiring layer 23, has studs 50 with solder layers 51 (Figure 7B).

The chips and alignment structure are then aligned as in the first embodiment, resulting in the arrangement shown in Figure 8A. Further processing, including lamination, filling the gap 60, planarizing the chips and attaching chip support 32, also proceeds as in the first embodiment. If the chip support is attached using a metallization/alloying process, the resulting structure is as shown in Figure 8B (compare Figure 6A). If the chip support is attached using a stud/via connection process with studs on the planarized back surface of the chips, the resulting structure is as shown in Figure 8C (compare Figure 6B).

The chip connection method described herein permits greatly increased wiring density for chip-to-chip interconnections, thereby realizing higher device bandwidth. Furthermore, with this method the need for conventional C4 chip-to-chip connections is eliminated; the complexity of the carrier substrate is therefore reduced. More space thus becomes available for a system designer to allocate C4s to meet other requirements; this in turn offers opportunities to design more advanced device structures.

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In addition, this method permits both highly accurate chip placement with vertical interconnections on the front side of the chips and assured thermal conductivity on the backside of the chips. It should also be noted that bonding over large areas often leads to formation of voids in the bonding area; with the small area of the stud/via connections this problem is greatly reduced. Furthermore, by using direct wiring interconnections, the overall chip signal fidelity is significantly improved (especially for high-frequency devices), and power requirements are reduced.

As noted above, this method is applicable to form large-area chips, chips with mixed functions, and chips fabricated with various (perhaps incompatible) processes. Accordingly, this method is especially useful for specialized, high-functionality chips such as ASICs, wireless chips and A/D convertor chips, among others.

While the invention has been described in terms of specific embodiments, it is evident in view of the foregoing description that numerous alternatives, modifications and variations will be apparent to those skilled in the art. Accordingly, the invention is intended to encompass all such alternatives, modifications and variations which fall within the scope and spirit of the invention and the following claims.

We claim:

1. A method for fabricating a semiconductor device including a chip, comprising the steps of:

providing a stud on a first surface of the chip;

providing a plate transparent to ablating radiation;

forming a first layer on the plate, the first layer including a conducting pad on a first surface of the first layer opposite the plate;

forming a second layer on the first surface of the first layer, where the plate, the first layer and the second layer form an alignment structure;

forming a via in the second layer to expose the conducting pad;

aligning the stud to the via;

attaching the chip to the alignment structure, so that the first surface of the chip contacts the second layer and the stud makes electrical contact with the conducting pad;

attaching a support to the chip; and

ablating an interface between the first layer and the plate using ablating radiation transmitted through the plate, thereby detaching the plate.

2. A method according to claim 1, wherein the first layer comprises polyimide, and the ablating radiation comprises laser radiation.

3. A method according to claim 1, wherein said step of forming the first layer further comprises providing electrical wiring in the first layer connecting to the conducting pad.

4. A method according to claim 1, wherein said step of forming the second layer further comprises depositing and curing a polyimide layer.

5. A method according to claim 1, further comprising the step of depositing an adhesive layer on the second layer prior to said step of attaching the chip to the alignment structure.

6. A method according to claim 1, wherein said step of providing a stud further comprises providing an alloy material on the stud, so that a metallic connection between the stud and the conducting pad is formed in said step of attaching the chip to the alignment structure.

7. A method according to claim 1, wherein said step of attaching the chip to the alignment structure further comprises the step of laminating the chip and the alignment structure.

8. A method according to claim 7, wherein the laminating step is performed using a temperature in the range 200 °C - 400 °C and a pressure in the range 10 psi - 200 psi.

9. A method according to claim 1, wherein the support is attached to a second surface of the chip opposite the first surface thereof, and further comprising the step of planarizing the second surface of the chip before said step of attaching the support.

10. A method according to claim 9, wherein said planarizing step is performed using chemical-mechanical polishing.

11. A method according to claim 1, wherein said step of attaching the support to the chip further comprises the steps of:

depositing a first metal layer on the support;

depositing a second metal layer on a second surface of the chip opposite the first surface thereof;

providing a third metal layer in contact with the first metal layer and in contact with the second metal layer; and

forming an alloy between the first metal layer and the third metal layer and between the second metal layer and the third metal layer, thereby bonding the support to the chip.

12. A method according to claim 1, wherein said step of attaching the support to the chip further comprises the steps of:

depositing a first bonding layer on the support;

depositing a second bonding layer on a second surface of the chip opposite the first surface thereof;

depositing an alloying layer on at least one of the first bonding layer and the second bonding layer; and

forming an alloy between the first bonding layer and the second bonding layer by a eutectic alloying process, thereby bonding the support to the chip.

13. A method according to claim 1, wherein said step of attaching a support to the chip further comprises the steps of:

providing a support connection stud on a second surface of the chip opposite the first surface thereof;

forming a layer on the support including a support conducting pad;

forming a via in the layer on the support to expose the support conducting pad;

aligning the support connection stud to the via in the layer on the support; and

causing the support connection stud to bond to the support conducting pad, thereby bonding the support to the chip.

14. A method according to claim 13, wherein said step of providing a support connection stud further comprises providing solder material on said stud, so that a solder connection between the support connection stud and the support conducting pad is formed in said step of causing the support connection stud to bond to the support conducting pad.

15. A method according to claim 1, wherein said step of attaching a support to the chip further comprises the steps of:

providing a support connection stud on the support;

forming a layer including a support conducting pad on a second surface of the chip opposite the first surface thereof;

forming a support connection via in said layer to expose the support conducting pad;

aligning the support connection stud to the support connection via; and

causing the support connection stud to bond to the support conducting pad, thereby bonding the support to the chip.

16. A method according to claim 15, wherein said step of providing a support connection stud further comprises providing solder material on said stud, so that a solder connection between the support connection stud and the support conducting pad is formed in said step of causing the support connection stud to bond to the support conducting pad.

17. A method according to claim 1, wherein said detaching of the plate exposes a second surface of the first layer opposite the first surface thereof, and further comprising the step of forming a connection pad on the second surface of the first layer.

18. A method according to claim 17, wherein the connection pad is a C4 pad.

19. A method according to claim 3, wherein a plurality of chips with a plurality of studs are connected to the alignment structure, the first layer includes a plurality of conducting pads, and the wiring in the first layer interconnects the chips.

20. A method according to claim 19, wherein said detaching of the plate exposes a second surface of the first layer opposite the first surface thereof, and further comprising the step of forming a plurality of C4 pads on the second surface of the first layer, the C4 pads making electrical connection with the chips through the wiring in the first layer, the studs and the conducting pads.

21. A method for fabricating a semiconductor device including a chip, comprising the steps of:

providing a plate transparent to ablating radiation;

forming a first layer on the plate;

providing a stud on a first surface of the first layer opposite the plate, where the plate, the first layer and the stud form an alignment structure;

forming a second layer on a first surface of the chip including a conducting pad contacting the chip;

forming a via in the second layer to expose the conducting pad;

aligning the stud to the via;

attaching the chip to the alignment structure, so that the first layer contacts the second layer and the stud makes electrical contact with the conducting pad;

attaching a support to the chip; and

ablating an interface between the first layer and the

plate using ablating radiation transmitted through the plate, thereby detaching the plate.

22. A method according to claim 21, wherein the first layer comprises polyimide, and the ablating radiation comprises laser radiation.

23. A method according to claim 21, wherein said step of forming the first layer further comprises providing electrical wiring in the first layer connecting to the stud.

24. A method according to claim 21, wherein said step of forming the second layer further comprises depositing and curing a polyimide layer.

25. A method according to claim 21, further comprising the step of depositing an adhesive layer on the second layer prior to said step of attaching the chip to the alignment structure.

26. A method according to claim 21, wherein said step of providing a stud further comprises providing an alloy material on the stud, so that a metallic connection between the stud and the conducting pad is formed in said step of attaching the chip to the alignment structure.

27. A method according to claim 21, wherein said step of attaching the chip to the alignment structure further comprises the step of laminating the chip and the alignment structure.

28. A method according to claim 27, wherein the laminating step is performed using a temperature in the range 200 °C - 400 °C and a pressure in the range 10 psi - 200 psi.

29. A method according to claim 21, wherein the chip support is attached to a second surface of the chip opposite the first surface thereof, and further comprising the step of planarizing the second surface of the chip before said step of attaching the chip support.

30. A method according to claim 29, wherein said planarizing step is performed using chemical-mechanical polishing.

31. A method according to claim 21, wherein said step of attaching a support to the chip further comprises the steps of:

depositing a first metal layer on the support;

depositing a second metal layer on a second surface of the chip opposite the first surface thereof;

providing a third metal layer in contact with the first metal layer and in contact with the second metal layer; and

forming an alloy between the first metal layer and the third metal layer and between the second metal layer and the third metal layer, thereby bonding the support to the chip.

32. A method according to claim 21, wherein said step of attaching the support to the chip further comprises the steps of:

depositing a first bonding layer on the support;

depositing a second bonding layer on a second surface of the chip opposite the first surface thereof;

depositing an alloying layer on at least one of the first bonding layer and the second bonding layer; and

forming an alloy between the first bonding layer and the second bonding layer by a eutectic alloying process, thereby bonding the support to the chip.

33. A method according to claim 21, wherein said step of attaching a support to the chip further comprises the steps of:

providing a support connection stud on a second surface of the chip opposite the first surface thereof;

forming a layer on the support including a support conducting pad;

forming a via in the layer on the support to expose the support conducting pad;

aligning the support connection stud to the via in the layer on the support; and

causing the support connection stud to bond to the support conducting pad, thereby bonding the support to the chip.

34. A method according to claim 33, wherein said step of providing a support connection stud further comprises providing solder material on said stud, so that a solder connection between the support connection stud and the support conducting pad is formed in said step of causing the support connection stud to bond to the support conducting pad.

35. A method according to claim 21, wherein said step of attaching a support to the chip further comprises the steps of:

providing a support connection stud on the support;

forming a layer including a support conducting pad on a second surface of the chip opposite the first surface thereof;

forming a support connection via in said layer to expose the support conducting pad;

aligning the support connection stud to the support connection via; and

causing the support connection stud to bond to the support conducting pad, thereby bonding the support to the chip.

36. A method according to claim 35, wherein said step of providing a support connection stud further comprises providing an alloy material on said stud, so that a metallic connection between the support connection stud and the support conducting pad is formed in said step of causing the support connection stud to bond to the support conducting pad.

37. A method according to claim 21, wherein said detaching of the plate exposes a second surface of the first layer opposite the first surface thereof, and further comprising the step of forming a connection pad on the second surface of the first layer.

38. A method according to claim 37, wherein the connection pad is a C4 pad.

39. A method according to claim 23, wherein a plurality of chips with a plurality of vias are connected to the alignment structure, the first layer has a plurality of studs thereon, and the wiring in the first layer interconnects the chips.

40. A method according to claim 39, wherein said detaching of the plate exposes a second surface of the first layer opposite the first surface thereof, and further comprising the step of forming a plurality of C4 pads on the second surface of the first layer, the C4 pads making electrical connection with the chips through the wiring in the first layer, the studs and the conducting pads.

41. A semiconductor device including a plurality of chips, the chips having front surfaces and back surfaces, the device comprising:

a support attached to the chips on the back surfaces thereof;

a first layer disposed on the front surfaces of the chips and having a plurality of vias formed therein and conducting pads in registration with the vias;

a plurality of studs corresponding to the vias and disposed therein; and

a second layer attached to the first layer on a surface of the first layer opposite the front surfaces of the chips, the second layer being aligned to the first layer by the studs in the vias, the second layer including electrical wiring connecting to the chips through the studs and the conducting pads.

42. A semiconductor device according to claim 41, wherein the electrical wiring in the second layer makes electrical connections between the chips.

43. A semiconductor device according to claim 41, wherein the conducting pads are disposed between the second layer and the corresponding vias, and the studs are formed in contact with the front surfaces of the chips.

44. A semiconductor device according to claim 41, wherein the conducting pads are disposed between the front surfaces of the chips and the corresponding vias, and the studs are formed in contact with the second layer.

45. A semiconductor device according to claim 41, wherein the first layer includes polyimide.

46. A semiconductor device according to claim 41, wherein the first layer includes an adhesive layer in contact with the front surface of the chips.

47. A semiconductor device according to claim 41, wherein an alloy material is disposed in the vias, so that metallic connections are formed between the studs and the corresponding conducting pads.

48. A semiconductor device according to claim 41, wherein the chips, the first layer and the second layer comprise a laminated structure.

49. A semiconductor device according to claim 41, wherein the back surfaces of the chips comprise a planarized surface.

50. A semiconductor device according to claim 41, wherein adjacent chips are separated by not more than 100 μm.

51. A semiconductor device according to claim 50, wherein a gap between the adjacent chips is filled with polyimide.

52. A semiconductor device according to claim 41, further comprising an attachment layer between the support and the chips.

53. A semiconductor device according to claim 52, wherein the attachment layer includes a metal alloy layer.

54. A semiconductor device according to claim 53, wherein the metal alloy layer is formed by a eutectic alloying process.

55. A semiconductor device according to claim 52, wherein the attachment layer has a plurality of support connection vias formed therein, support connection pads in registration with the support connection vias, and a plurality of support connection studs disposed in the support connection vias and connected to the support connection pads.

56. A semiconductor device according to claim 55, wherein an alloy material is disposed in the support connection vias, so that metallic connections are formed between the support connection studs and the corresponding support connection pads.

57. A semiconductor device according to claim 55, wherein the support connection pads are disposed between the support connection vias and the support, and the support connection studs are formed in contact with the back surfaces of the chips.

58. A semiconductor device according to claim 55, wherein the support connection pads are disposed between the support connection vias and the back surfaces of the chips, and the support connection studs are formed in contact with the support.

59. A semiconductor device according to claim 41, further comprising a plurality of electrical connection pads on a surface of the second layer opposite the first layer.

60. A semiconductor device according to claim 59, wherein the electrical connection pads are C4 pads.