17/06/02

2002036416

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

162162

(43) International Publication Date
28 June 2001 (28.06.2001)

PCT

(10) International Publication Number
WO 01/46989 A3

(51) International Patent Classification[7]: H01L 29/94, 27/06

(21) International Application Number: PCT/US00/31352

(22) International Filing Date:
13 November 2000 (13.11.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/469,406 22 December 1999 (22.12.1999) US

(71) Applicant *(for all designated States except US)*: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **KESHAVARZI, Ali** [IR/IR]; 2341 NW Berkendene Street, Portland, OR 97229 (US). **DE, Vivek, K.** [IN/IN]; 9785 SW 151st Avenue, Beaverton, OR 97007 (US). **KARNIK, Tanay** [IN/IN]; 3574 NW Blackcomb Drive, Portland, OR 97229 (US). **NAIR, Rajendran** [IN/IN]; 19000 NW Evergreen Parkway #258, Hillsboro, OR 97124 (US).

(74) Agents: **MALLIE, Michael, J.** et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th Floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

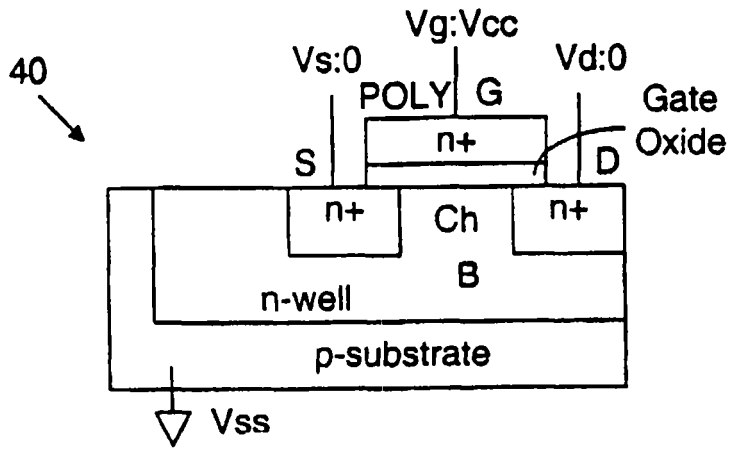
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(88) Date of publication of the international search report:
10 May 2002

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: DECOUPLING CAPACITORS FOR THIN GATE OXIDES



(57) Abstract: In some embodiments, the invention involves a die having a first conductor carrying a power supply voltage and a second conductor carrying a ground voltage. A semiconductor capacitor operating in depletion mode is coupled between the first and second conductors to provide decoupling capacitance between the first and second conductors, the semiconductor capacitor having a gate voltage. Various configurations may be used including: n+ gate poly and n+ source/drain regions in an n-body; p+ gate poly and n+ source/drain regions in an n-body; p+ gate poly and p+ source/drain regions in an n-body; p+ gate poly and p+ source/drain regions in a p-body; n+ gate poly and p+ source/drain regions in a p-body; n+ gate poly and n+ source/drain regions in a p-body. The power supply voltage may have a larger absolute value than does a flatband voltage.

WO 01/46989 A3

ACTION