What is claimed is:

1. A semiconductor device comprising:

a source layer on a substrate;

a plurality of channel structures on the substrate, the plurality of channel structures each including a vertical insulating layer and a vertical channel layer, the plurality of channel structures extending in a first direction perpendicular to an upper surface of the substrate; a plurality of gate electrodes on the source layer and spaced apart from each other along the first direction on a sidewall of each of the plurality of channel structures, and at least one gate electrode of the plurality of gate electrodes is configured to provide a gate-induced drain leakage (GIDL) line;

a common source line penetrating through the plurality of gate electrodes, the common source line extending in the first direction and electrically connected to the source layer; and

a memory controller configured to, during an erasing operation,

apply an erasing voltage to the common source line until the erasing voltage reaches a target voltage,

increase the erasing voltage to a desired step-up voltage which has a voltage level higher than a voltage level of the target voltage, for a desired step-up time period after the erasing voltage reaches the target voltage, wherein the desired step-up time period is less than a total time period of the erasing operation in which the erasing voltage is applied, and

reduce the erasing voltage to the target voltage after the desired step-up time period expires.

2. The semiconductor device of claim 1, wherein the desired step-up voltage is at least two step increments higher than the voltage level of the target voltage.

3. The semiconductor device of claim 1 or claim 2, wherein

a portion of the source layer extends along the vertical channel layer in a common source extension region; and

the common source extension region overlaps at least a portion of the GIDL line.

4. The semiconductor device of any one of claims 1 to 3, further comprising:

an insulating layer surrounding a side surface of the common source line,

wherein the plurality of gate electrodes are electrically isolated from each other by the insulating layer.

5. The semiconductor device of any one of claims 1 to 4, wherein the memory controller is further configured to increase the erasing voltage by stepping up the erasing voltage by step increments until the erasing voltage reaches the target voltage.

6. The semiconductor device of claim 5, wherein the increase of the erasing voltage during the desired step-up time period has a pulse width equal to a pulse width of a unit step voltage of the erasing voltage.

7. The semiconductor device of claim 5 or claim 6, wherein the increase of the erasing voltage during the desired step-up time period has a voltage magnitude equal to a voltage magnitude of a unit step voltage of the erasing voltage.

8. The semiconductor device of claim 5, wherein the increase of the erasing voltage during the desired step-up time period has a pulse width different from a pulse width of a unit step voltage of the erasing voltage.

9. The semiconductor device of claim 5 or claim 8, wherein the increase of the erasing voltage during the desired step-up time period has a voltage magnitude different from a voltage magnitude of a unit step voltage of the erasing voltage.

10. The semiconductor device of any one of claims 1 to 4, wherein the increase of the erasing voltage during the desired step-up time period has a pulse width that is 10% or less of the total time period of the erasing operation.

11. The semiconductor device of any one of claims 1 to 4 or claim 10, wherein the increase of the erasing voltage during the desired step-up time period has a voltage magnitude that is 10% or less of the target voltage.

12. The semiconductor device of any one of claims 1 to 11, wherein the memory controller is further configured to:

increase a GIDL voltage applied to the GIDL line until the erasing voltage reaches the target voltage, the increased GIDL voltage being increased or decreased while maintaining a constant potential difference with the erasing voltage.

13. A semiconductor device comprising:

a plurality of bitlines;

a common source line configured to receive an erasing voltage during an erasing operation;

at least one memory cell string connected between one bit line of the plurality of bitlines and the common source line, the at least one memory cell string including a plurality of memory cells, and at least one string select line connected to the one bitline;

a gate-induced drain leakage (GIDL) line electrically connected to the common source line, the GIDL line configured to receive a GIDL voltage, the received GIDL voltage

being increased while maintaining a constant potential difference with the erasing voltage until the erasing voltage reaches a target voltage during the erasing operation;

a ground select line on the GIDL line; and

a plurality of wordlines between the string select line and the ground select line

wherein an overshoot occurs when a voltage higher than the target voltage is applied after the erasing voltage, that is applied to the common source line, reaches the target voltage during the erasing operation, and

wherein a time period in which the voltage higher than the target voltage is applied, is less than a total time period of the erasing operation in which the erasing voltage is applied.

14. The semiconductor device of claim 13, further comprising:

a string select transistor connected to the string select line, the string select transistor configured to be in a turned-off state during the erasing operation.

15. The semiconductor device of claim 13 or claim 14, wherein the plurality of wordlines are configured to receive a ground voltage during the erasing operation.

16. The semiconductor device of any one of claims 13 to 15, wherein the GIDL voltage is increased by a unit step voltage while maintaining the constant potential difference with the erasing voltage when the erasing voltage is increased by a unit step voltage, until the erasing voltage reaches the target voltage.

17. A semiconductor device comprising:

a substrate;

a source layer on an upper surface of the substrate;

a plurality of gate electrode layers, the plurality of gate electrode layers includes a lowermost gate electrode configured to provide a gate-induced drain leakage (GIDL) line;

a plurality of insulating layers, the plurality of insulating layers and the plurality of gate electrode layers stacked alternately on the source layer;

a plurality of channel structures, each of the plurality of channel structures having a vertical insulating layer and a vertical channel layer, the plurality of channel structures extending in a first direction perpendicular to the upper surface of the substrate;

a common source line penetrating through the plurality of gate electrodes, the common source line extending in the first direction and electrically connected to the source layer;

a common source extension region including a portion of the source layer which extends along the vertical channel layer, the common source extension region formed to overlap at least a portion of the GIDL line; and

a memory controller configured to, during an erasing operation,

apply an erasing voltage to the common source line until the erasing voltage reaches a target voltage,

provide a high magnitude voltage to the source layer during the erasing operation, the high magnitude voltage having a magnitude greater than a magnitude of the erasing voltage of the erasing operation, wherein the high magnitude voltage has a voltage level higher than a voltage level of the target voltage, and

wherein a time period in which the high magnitude voltage is applied, is less than a total time period of the erasing operation in which the erasing voltage is applied.

18. The semiconductor device of claim 17, wherein the memory controller is further configured to:

generate an increasing GIDL voltage during a first period of the erasing operation, the increasing GIDL voltage having a first potential difference that is maintained with the erasing voltage until the erasing voltage reaches the target voltage, wherein a lateral field is generated based on the first potential difference between the GIDL voltage and the erasing voltage;

increase a voltage level of the erasing voltage to at least one step higher than the voltage level of the target voltage during a second period of the erasing operation after the erasing voltage reaches the target voltage, the increasing the voltage level of the erasing voltage including establishing a second potential difference between the erasing voltage and the GIDL voltage, the second potential difference being greater than the first potential difference, wherein the lateral field is increased by the second potential difference;

decrease the erasing voltage to the target voltage after the voltage level of the erasing voltage is increased; and

maintain the erasing voltage at the target voltage during a third period of the erasing operation following the second period, the maintaining the erasing voltage including maintaining the first potential difference between the erasing voltage and the GIDL voltage.

19. The semiconductor device of claim 18, wherein the first potential difference causes a portion of the vertical channel layer to accumulate holes as electrons of the vertical channel layer migrate to the common source extension region.

20. The semiconductor device of claim 19, wherein the second potential difference causes an increase in a speed of the electrons of the vertical channel layer as the electrons migrate to the common source extension region.