INTEGRATED CIRCUIT FABRICATION

Priority Application

[0001] This application claims the benefit of U.S. Provisional Patent Application 60/666,031 (filed 28 March 2005). The entire disclosure of this priority application is hereby incorporated by reference herein.

Reference to Related Applications

[0002] This application is related to U.S. Patent Application 10/932,993 (filed 1 September 2004; Attorney Docket MICRON.293A; Micron Docket 2003-1435.00/US), U.S. Patent Application 10/934,778 (filed 2 September 2004; Attorney Docket MICRON.294A; Micron Docket 2003-1446.00/US), U.S. Patent Application 10/931,771 (filed 31 August 2004; Attorney Docket MICRON.295A; Micron Docket 2004-0068.00/US), U.S. Patent Application 10/934,317 (filed 2 September 2004; Attorney Docket MICRON.296A; Micron Docket 2004-0114.00/US), U.S. Patent Application _____ (filed concurrently herewith; Attorney Docket MICRON.313A; Micron Docket 2004-1065.00/US), U.S. Provisional Patent Application 60/662,323 (filed 15 March 2005; Attorney Docket MICRON.316PR; Micron Docket 2004-1130.00/PR), and U.S. Patent Application 11/134,982 (filed 23 May 2005; Attorney Docket MICRON.317A; Micron Docket 2004-0968.00/US). The entire content of all of these related applications is hereby incorporated by reference herein.

Field of the Invention

[0003] The present invention relates generally to integrated circuit fabrication, and more specifically to masking techniques.

Background of the Invention

[0004] Integrated circuits are continuously being made smaller as demand for portability, computing power, memory capacity and energy efficiency in modern electronics grows. Therefore, the size of the integrated circuit constituent features, such as electrical devices and interconnect line widths, is also decreasing continuously. The trend of decreasing feature size is evident in memory circuits or devices such as dynamic

random access memory ("DRAM"), flash memory, nonvolatile memory, static random access memory ("SRAM"), ferroelectric ("FE") memory, logic gate arrays and so forth.

[0005] For example, DRAM typically comprises millions of identical circuit elements, known as memory cells. In its most general form, a memory cell typically consists of two electrical devices: a storage capacitor and an access field effect transistor. Each memory cell is an addressable location that can store one binary digit ("bit") of data. A bit can be written to a cell through the transistor and read by sensing charge on the storage electrode from the reference electrode side. By decreasing the sizes of constituent electrical devices and the conducting lines that access them, the sizes of the memory devices incorporating these features can be decreased. Thus, storage capacities can be increased by fitting more memory cells into the memory devices.

[0006] As another example, flash memory (for example, electrically erasable programmable read only memory or "EEPROM") is a type of memory that is typically erased and reprogrammed in blocks instead of one byte at a time. A typical flash memory comprises a memory array, which includes a large number of memory cells. The memory cells include a floating gate field effect transistor capable of holding a charge. The data in a cell is determined by the presence or absence of the charge in the floating gate. The cells are usually grouped into sections called "erase blocks." The memory cells of a flash memory array are typically arranged into a "NOR" architecture (each cell directly coupled to a bit line) or a "NAND" architecture (cells coupled into "strings" of cells, such that each cell is coupled indirectly to a bit line and requires activating the other cells of the string for access). The cells within an erase block can be electrically programmed in a random basis by charging the floating gate. The charge can be removed from the floating gate by a block erase operation, wherein all floating gate memory cells in the erase block are erased in a single operation.

[0007] The pitch of a pattern is defined as the distance between an identical point in two neighboring pattern features. These features are typically defined by openings in, and spaced from each other by, a material, such as an insulator or conductor. Thus, pitch can be understood as the sum of the width of a feature and the width of the space separating that feature from a neighboring feature.

Summary of the Invention

[0008] In one embodiment of the present invention, a method for defining patterns in an integrated circuit comprises defining a plurality of features in a first photoresist layer using photolithography over a first region of a substrate. Pitch multiplication is used to produce at least two features in a lower masking layer for each feature in the photoresist layer. The features in the lower masking layer include looped ends. A second photoresist layer covers a second region of the substrate including the looped ends in the lower masking layer. A pattern of trenches is etched in the substrate through the features in the lower masking layer without etching in the second region. The trenches have a trench width.

[0009] In another embodiment of the present invention, a method of making a plurality of conductive lines in an array comprises providing a film stack. The film stack includes a substrate in contact with a plurality of conductive plugs, an insulating film overlying the conductive plugs, a lower mask layer overlying the insulating film, and an array of spacers formed over the lower mask layer. A sacrificial film is deposited over the lower mask layer and the array of spacers. A secondary mask is formed over a portion of the sacrificial film. The secondary mask defines an opening in the array of spacers. The lower mask layer and the sacrificial film can be etched selectively with respect to the secondary mask. The sacrificial film is etched and a portion of the lower mask layer is exposed. The method further comprises etching the lower mask layer and exposing a portion of the insulating film. A plurality of trenches are etched in the insulating film, the lower mask layer, and the sacrificial film to expose at least a portion of the conductive plugs. A blanket metal deposition is performed. A planar surface is then formed, alternating between metal and insulating film in a damascene process.

[0010] In another embodiment of the present invention, a method of pitch multiplication for damascene features in an integrated circuit comprises providing a substrate. A first masking process is performed to define an array of spacer lines over the substrate. The spacer lines are separated by a plurality of gaps. A second masking process is performed to block a portion of the spacer lines and that defines a plurality of interconnects in a logic region of the integrated circuit. A plurality of trenches are etched in the gaps between the spacer lines. A metal layer is deposited to form a plurality of metal lines in the gaps between the spacer lines. The integrated circuit is provided with a substantially planar surface in a damascene process.

[0011] In another embodiment of the present invention, a method of forming integrated circuit components on a substrate comprises using a lithographic technique to pattern a first resist layer and define a plurality of lines. A pitch multiplication technique is used to form a pattern of spacers around a region defined by the plurality of lines. The spacers comprise elongate loops having loop ends. A second resist layer is deposited over the loop ends to define a blocked region of the substrate. The method further comprises selectively etching through the spacers to from a plurality of trenches in the substrate without etching in the blocked regions.

Brief Description of the Drawings

[0012] Exemplary embodiments of the integrated circuits and integrated circuit fabrication techniques are illustrated in the accompanying drawings, which are for illustrative purposes only. The drawings comprise the following figures, which are not necessarily drawn to scale. In the figures like numerals indicate like parts.

[0013] Figure 1A is a cross-sectional view of a substrate having a plurality of mask lines formed thereon.

[0014] Figure 1B is a cross-sectional view of the substrate of Figure 1A after an anisotropic etch process transferring the mask pattern into a temporary layer.

[0015] Figure 1C is a cross-sectional view of the substrate of Figure 1B after removal of the mask lines and an isotropic "shrink" etch.

[0016] Figure 1D is a cross-sectional view of the substrate of Figure 1C after blanket deposition of a spacer material of mandrels left in the temporary layer.

[0017] Figure 1E is a cross-sectional view of the substrate of Figure 1D after a directional spacer etch process to leave pitch-multiplied features or spacers.

[0018] Figure 1F is a cross-sectional view of the substrate of Figure 1E after removal of the mandrels.

[0019] Figure 2 is a schematic top view of an exemplary partially formed integrated circuit.

[0020] Figure 3 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 2 after forming a plurality of pitch-multiplied features in and over the substrate.

[0021] Figure 4 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 3 after forming an insulating film thereover.

[0022] Figure 5 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 4 after forming a hard mask layer thereover.

[0023] Figure 6A is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 5 after forming a plurality of spacers thereover.

[0024] Figure 6B is a schematic top view of the partially formed integrated circuit of Figure 6A.

[0025] Figure 7 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 6A after deposition of a bottom antireflective coating ("BARC") thereover.

[0026] Figure 8A is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 7 after formation of a second photoresist pattern thereover.

[0027] Figure 8B is a schematic top view of the partially formed integrated circuit of Figure 8A.

[0028] Figure 9 is a schematic, cross-sectional side view of the partially formed integrated circuit of Figure 8A after etching the bottom antireflective coating.

[0029] Figure 10A is a schematic, view of the partially formed integrated circuit of Figure 9 after etching the hard mask layer through the spacers and the second photoresist pattern; the view is a cross-section taken along a line perpendicular to a spacer loop.

[0030] Figure 10B is a schematic view of the partially formed integrated circuit of Figure 9 after etching the hard mask layer through the spacers and the second photoresist pattern; the view is a cross-section taken along the length of a spacer loop.

[0031] Figure 11 is a schematic, cross-sectional view of the partially formed integrated circuit of Figure 10A after etching insulating film and removing the photoresist, the BARC and the spacers.

[0032] Figure 12 is a schematic, cross-sectional view of the partially formed integrated circuit of Figure 11 after deposition of a conductive material thereover.

[0033] Figure 13 is a schematic, cross-sectional view of the partially formed integrated circuit of Figure 12 after a chemical mechanical planarization process is performed.

[0034] Figure 14 is a flowchart illustrating an exemplary process for forming certain of the integrated circuit structures disclosed herein.

[0035] Figure 15 is a schematic top view of a partially formed integrated circuit including spacer loops and a metal layer.

[0036] Figure 16 is a schematic, cross-sectional view of the partially formed integrated circuit of Figure 13, further including an overhead contact between the array region and the peripheral region.

[0037] Figure 17A is a layout view of a first mask formed by a photolithographic process; the first mask defines a plurality of mandrels.

[0038] Figure 17B is a layout view of a spacer pattern obtained by performing a pitch multiplication technique on the mandrels of Figure 17A.

[0039] Figure 17C is a layout view of a partially formed integrated circuit formed by application of a second metal mask to the spacer pattern of Figure 17B.

Detailed Description of Preferred Embodiments

[0040] The continual reduction in feature size places ever greater demands on techniques used to form the features. For example, photolithography is commonly used to pattern features, such as lines, on a substrate. The concept of pitch can be used to describe the size of these features. Due to optical factors such as light or radiation wavelength, however, photolithography techniques have a minimum pitch below which features cannot be formed reliably. Thus, the minimum pitch of a photolithographic technique can limit feature size reduction.

[0041] Pitch doubling is one method proposed for extending the capabilities of photolithographic techniques beyond their minimum pitch. Such a method is illustrated in Figures 1A–1F and is described in U.S. Patent No. 5,328,810 (issued 12 July 1994), the entire disclosure of which is incorporated herein by reference. With reference to Figure 1A, photolithography is first used to form a pattern of lines 10 in a photoresist layer overlying a layer 20 of a temporary or expendable material and a substrate 30. Common wavelengths which are used in performing the photolithography include, but are not limited to, 157 nm, 193 nm, 248 nm or 365 nm. As shown in Figure 1B, the pattern is then transferred by an etch step, such as an anisotropic etch step, to the temporary layer 20, thereby forming placeholders or mandrels 40. The photoresist lines 10 can be stripped and the mandrels 40 can be isotropically etched to increase the distance between neighboring mandrels 40, as shown in Figure 1C. A layer 50 of spacer material is subsequently deposited over the mandrels 40, as shown in Figure 1D. Spacers 60 are

then formed on the sides of the mandrels 40 by preferentially etching the spacer material from the horizontal surfaces in a directional spacer etch, as shown in Figure 1E. The remaining mandrels 40 are then removed, leaving behind only the spacers 60, which together act as a mask for patterning, as shown in Figure 1F. Thus, where a given pattern area formerly defined one feature and one space (each having a width *F*, for a pitch of 2*F*), the same pattern area now includes two features and two spaces, as defined by spacers 60 (each having a width ½*F*, for a pitch of *F*). Consequently, the smallest feature size possible with a photolithographic technique is effectively decreased by using the pitch doubling technique.

[0042] While the pitch is actually halved in the example above, this reduction in pitch is conventionally referred to as pitch "doubling," or, more generally, pitch "multiplication". That is, conventionally "multiplication" of pitch by a certain factor actually involves reducing the pitch by that factor. The conventional terminology is retained herein. Note that by forming spacers upon spacers, the definable feature size can be further decreased. Thus, pitch multiplication refers to the process generally, regardless of the number of times the spacer formation process is employed.

[0043] Because the layer 50 of spacer material typically has a single thickness 90 (see Figures 1D and 1E), and because the sizes of the features formed by the spacers 60 usually corresponds to that thickness 90, the pitch doubling technique typically produces features of only one width. However, integrated circuits often include features of different sizes. For example, random access memory circuits typically contain arrays of memory cells and logic circuits in the so-called "periphery". In the arrays, the memory cells are typically connected by conductive lines and, in the periphery, the conductive lines typically contact landing pads for connecting arrays to logic. Peripheral features such as landing pads, however, can be larger than the conductive lines. Additionally, peripheral electrical devices such as transistors are preferably larger than electrical devices in the array. Moreover, even if peripheral features can be formed with the same pitch as the array, the flexibility required to define circuits will typically not be possible using a single mask, particularly if the patterns are limited to those that can be formed along the sidewalls of resist patterns.

[0044] Some proposed methods for forming patterns at the periphery and at the array involve three separate masks. For example, in one method, a first mask and pitch doubling are used to form a spacer pattern, which typically comprises spacer loops

in one region of a chip, such as the array region of a memory device. Then, a second mask is performed to form a second pattern in another region of the chip, such as the peripheral region of a memory device. This second peripheral pattern is formed in a layer overlying the spacer pattern. This covers the central portion of the spacer loops while the looped ends of the spacers are left exposed to an etching process. Then, a third mask is performed to form a third pattern that includes interconnects in and/or from the peripheral region. Both the "chopped" spacer pattern and the third pattern are then transferred to an underlying masking layer which can be etched relative to an underlying substrate. This allows features having different sizes—as compared to each other and as compared to the spacer loops—to be formed in the circuit peripheral region. Such features include, for example, interconnect patterns. These features can overlap with the spacer loops, can be consolidated with features in the circuit array region, and can be subsequently etched.

[0045] In accordance with the foregoing, improved techniques have been developed for forming features of different sizes, especially pitch-multiplied features having overlapping patterns.

[0046] In certain embodiments, part of the feature pattern to be transferred to a substrate has a pitch below the minimum pitch of the photolithographic technique used for processing the substrate. Additionally, certain embodiments can be used to form devices having arrays of electrical devices, including logic or gate arrays and volatile and non-volatile memory devices such as DRAM, read only memory ("ROM"), flash memory and gate arrays. In such devices, pitch multiplication is usable to form, for example, transistor gate electrodes and conductive lines in the array region of the chips, while conventional photolithography is usable to form larger features, such as contacts, at the peripheries of the chips. Exemplary masking steps in the course of fabricating a memory device are illustrated in the figures and are described herein.

[0047] Figure 2 shows a top view of an exemplary partially fabricated integrated circuit 100, such as a memory chip. A central array region 102 is surrounded by a peripheral region 104. It will be appreciated that, after the integrated circuit 100 is fabricated, the array 102 will typically by densely populated with conducting lines and electrical devices such as transistors and capacitors. Pitch multiplication can be used to form features in the array region 102, as discussed herein. On the other hand, the peripheral region 104 optionally includes features larger than those in the array region 102. Conventional photolithography, rather than pitch multiplication, is typically used to

pattern these larger features, examples of which include various types of logic circuitry. The geometric complexity of the logic circuits located in the peripheral region 104 makes using pitch multiplication difficult. In contrast, the regular grid typical of array patterns is conducive to pitch multiplication. Additionally, some devices in the peripheral region 104 may require larger geometries due to electrical constraints, thereby making pitch multiplication less advantageous than conventional photolithography for such devices. In addition to possible differences in relative scale, the relative positions, and the number of peripheral regions 104 and array regions 102 in the integrated circuit 100 can vary in other embodiments.

[0048] Figure 3 shows a partial cross-sectional view of the partially fabricated integrated circuit of Figure 2, including portions of the array region 102 and the peripheral region 104. Using a photolithography technique, a plurality of trenches are etched into a substrate 108, and these trenches are filled with an insulator 105, such as an oxide. The insulator 105 is a field isolation layer, and in an exemplary embodiment is a shallow trench isolation ("STI") layer deposited in a high density plasma ("HDP"), spin-on dielectric ("SOD"), flow-fill or TEOS process. In an exemplary embodiment, the SOD is deposited and densified.

[0049] An upper interlevel dielectric ("ILD") insulator 106 is formed over the substrate, and contact is made through the ILD 106 by etching contact holes and filling with conductive plugs 110. In one embodiment, the conductive plugs 110 comprise polycrystalline silicon, although other electrically conductive materials can be used in other embodiments. Portions of an etch stop layer 112, such as a nitride layer, are disposed over the insulator 106; the etch stop layer 112 is used in the formation of the conductive plugs 110. In certain embodiments, the insulator 105 is aligned with the substrate/plug interface. However, in other embodiments the insulator 105 extends slightly above the substrate/plug interface, as illustrated in Figure 3.

[0050] In the exemplary embodiment illustrated in Figure 3, the feature size in the array region 102 is smaller than the feature size in the peripheral region 104. In one embodiment, the conductive plugs 110 have a feature size of approximately 50 nm. In a preferred embodiment, the conductive plugs 110 have a feature size between approximately 30 nm and approximately 100 nm. More preferably, the conductive plugs have a feature size between approximately 32.5 nm and approximately 65 nm. Other feature sizes for the conductive plugs 110 can be used in other embodiments. Additional

details regarding the techniques used to form the conductive plugs are provided in U.S. Patent Application _____ (filed concurrently herewith; Attorney Docket MICRON.313A; Micron Docket 2004-1065.00/US).

[0051] As illustrated in Figure 4, an insulator film 114 in which damascene trenches are to be formed is deposited over the film stack illustrated in Figure 3. In one embodiment, the insulator film comprises an un-doped oxide film, such as an oxide film deposited from tetra ethyl ortho-silicate ("TEOS"), while in other embodiments the insulator film comprises a doped oxide film, such as BPSG or PSG. Other non-oxide insulators can be used in still other embodiments. In an exemplary embodiment, the insulator film 114 is deposited to a thickness corresponding to the conductor height to be formed in the integrated circuit.

[0052] As illustrated in Figure 5, a hard mask layer 116 is deposited over the insulator film 114. In one embodiment, the hard mask layer 116 comprises amorphous silicon, although other materials can be used in other embodiments.

[0053] As illustrated in Figure 6A, a plurality of spacers 118 are formed over the hard mask layer 116. In an exemplary embodiment, the spacers are formed using a pitch doubling technique such as that illustrated in Figures 1A through 1F, using the disclosed photoresist mask, transfer to a temporary layer, isotropic etch and spacer process. In an exemplary embodiment, the spacers comprise a low temperature oxide material that can be etched selectively with respect to the underlying hard mask layer 116. For example, in one embodiment the spacers are deposited at a temperature less than about 400°C. In another embodiment, the spacers are deposited using an atomic layer deposition process. Exemplary materials for the spacers include silicon oxide, silicon nitride, polycrystalline silicon and carbon.

[0054] Between the spacers 118 are gaps 120 that correspond to regions of the integrated circuit where conductive material is to be deposited. In the exemplary embodiment illustrated in Figure 6A, the gaps 120 are vertically aligned with the conductive plugs 110.

[0055] In an exemplary embodiment, the spacing between the spacers 118 and the gaps 120 varies between the array region 102 and the peripheral region 104 of the integrated circuit 100. This is further illustrated in Figure 6B, which schematically shows a top view of the spacers 118 and the intervening gaps 120. Figure 6B also illustrates

that the spacers 118 generally follow the outline of the lines formed in the photo definable layer, thereby forming a plurality of looped ends 124.

[0056] As illustrated in Figure 7, a BARC 122 is applied over the spacers 118. The BARC 122 is optionally applied in a spin-on process, thereby providing a substantially planar surface. After the BARC 122 is applied over the spacers 118, a second mask is applied. The second mask results in a pattern of photoresist 126 being deposited over the integrated circuit. The photoresist pattern defines a blocked region that blocks the looped ends 124 of the spacers 118 and defines one or more openings 128 in the peripheral region 104. This is illustrated in Figures 8A (side view) and 8B (top view). As illustrated in Figure 8B, in an exemplary embodiment the second mask is spaced apart from the spacers 118 by a gap 120a, and is spaced apart from the spacer looped ends 124 by a gap 120b. The gaps 120a, 120b accommodate misalignment of the second mask with respect to the spacer pattern.

[0057] In an exemplary embodiment, the minimum width of the openings 128 depends on the native resolution of the photolithographic process, which in one embodiment is as low as 100 nm, which in another embodiment is as low as 65 nm, and which in another embodiment is as low as 45 nm. Other dimensions can be used in other embodiments. In an exemplary embodiment, the spacers 118 in the circuit array region 104 are sufficiently spaced apart to allow contacts 132 to be "landed" to provide interconnections to other levels of the integrated circuit.

[0058] In an exemplary embodiment, after the second mask is performed, the BARC 122 is etched, as illustrated in Figure 9. In a modified embodiment, the pattern defined by the second mask, including the blocked region, is transferred to an intermediate layer before etching the BARC. In such embodiments intermediate layer or the BARC alone is used to block the looped ends 124 of the spacers 118.

[0059] The BARC etch is followed by an etch of the hard mask layer 116, which can be selectively etched with respect to the spacers 118. The resulting structure is illustrated in Figure 10A (which is a cross-sectional view taken along a line perpendicular to a spacer loop) and in Figure 10B (which is a cross-sectional view taken along the length of a spacer loop). In one embodiment, the hard mask etch is a dry etch process. This is followed by successive removal of the photoresist 126 and BARC 122, followed by an oxide etch. In such embodiments, the oxide etch will remove both the spacers 118 and exposed portions of the insulator film 114. The conductive plugs 110 provide an etch

stop. The resulting structure, which is illustrated in Figure 11, includes a pattern of trenches exposing the conductive plugs 110 in the array region 102, and a pattern of other openings 128 in the hard mask layer 116 in the peripheral region 104. This sequence advantageously lowers the effective aspect ratio for the trenches. In a modified embodiment, the insulator film 114 illustrated in Figures 10A and 10B is etched without prior removal of the spacers 118. The BARC 122 is optionally omitted in embodiments wherein the substrate material is not reflective.

[0060] Regardless of how the trenches are formed, the etch processes illustrated in Figures 10A, 10B and 11 advantageously consolidate two mask patterns: the pattern formed by the spacers 118 in the array region 102, and the pattern formed by the photoresist 126 in the peripheral region. This effectively forms a superposition of two distinct patterns, which allows etching through the gaps 120 between the spacers 118 in regions of the integrated circuit 100 not covered by the second photoresist layer 126.

[0061] As illustrated in Figure 12, in an exemplary embodiment conductive material 130 is then deposited over the partially formed integrated circuit. Optionally, the hard mask layer 116 is removed before deposition of the conductive material 130. Suitable conductive materials include, but are not limited to, titanium, titanium nitride, tungsten, tantalum nitride and copper. In an exemplary embodiment, the conductive material 130 is deposited to a thickness sufficient such that the widest trench width in the periphery is filled. After deposition of the conductive material, a chemical mechanical planarization ("CMP") process is used to separate the conductors in the trenches and provide the integrated circuit with a planar surface. The resulting structure is illustrated in Figure 13.

[0062] A flowchart illustrating an exemplary process for forming certain of the integrated circuit structures disclosed herein is provided in Figure 14. As illustrated, a plurality of features are defined in a first resist layer in an array region of the memory device in an operational block 150. Examples of resist layers that can be used to define the features are photoresist layers and imprinted resist layers. Based on these features, pitch multiplication is used to define a plurality of spacer loops in a lower masking layer in an operational block 152. In a modified embodiment, the spacer loops are formed over the patterned resist features, although this is less preferred because resist is generally unable to withstand spacer deposition and etch processes. The ends of the spacer loops are blocked with a second resist layer that also defines features in a periphery region of

the integrated circuit in an operational block 156. After the second resist layer is applied, an insulating layer in the gaps between the spacers is etched, the etching being performed in a pattern defined by the second resist layer in an operational block 158. A metal fill and subsequent CMP process can then be performed over the partially-formed integrated circuit in an operational block 160, thereby allowing metal lines to be formed in the integrated circuit array region (operational block 162) and electrical interconnects to be formed in the integrated circuit peripheral region (operational block 164). The interconnects are optionally used to connect integrated circuit components, such as logic components, within the periphery. Alternatively, the second mask can define other patterns, such as capacitors, contacts, resistors, simultaneously with blocking the spacer loops.

[0063] In certain embodiments, the peripheral interconnects are also optionally used to form electrical connections between the array region 102 and the peripheral region 104. This is illustrated in operational block 166 of Figure 14. For example, such contacts can be formed in a plane above the damascene structure illustrated in Figure 13. An example of such an "overhead" contact is provided in Figure 16. As illustrated, the overhead contact includes a plurality of contacts 146 connected by an interconnect line 148.

[0064] Figure 17A through 17C provide a top-down view of an exemplary embodiment of the methods illustrated in Figure 14. In particular, Figure 17A illustrates a first mask 134 defined by a photolithographic process. In one embodiment, the first mask 134 is defined in a layer of photoresist material, although in other embodiments the first mask 134 is transferred to another layer, such as an amorphous carbon layer. Figure 17B illustrates a spacer pattern 136 created by first shrinking the first mask 134 using an isotropic etch process, and then performing a pitch doubling technique on the shrunken first mask. Application of a second metal mask 138 yields the exemplary structure illustrated in Figure 17C. This structure includes widened portions in the spacer pattern configured to receive contacts 139 from other layers of the integrated circuit.

[0065] Certain of the integrated circuit fabrication techniques disclosed herein offer significant advantages over conventional techniques. For example, conventional methodology requires three separate masks to define the array region, to define the peripheral region, and to remove the looped ends of circuit features. In contrast, certain of the techniques disclosed herein allow pitch reduced features to be formed in a damascene

process that uses only two masks. As described herein, in exemplary embodiments the looped ends of array features can be blocked with the same mask that is used to define periphery features.

[0066] In another aspect of certain embodiments, rules are provided to facilitate circuit designers to implement the integrated circuit fabrication methods disclosed herein. The configuration of the masks indirectly corresponds to the integrated circuit patterns that are formed, particularly when the gaps between the spacer loops, some of which are enclosed and some of which are not, define the circuit features of interest. Such features can be formed as disclosed herein using pitch multiplication and damascene techniques. The rules discussed below provide a circuit designer with guidelines for building a circuit that is formable using the techniques disclosed herein. As described herein, building a circuit is compliance with these rules allows mixed use of interconnects with varying pitch size while using only two masks. Specifically, a spacer layer mask, or "spacer", is used to define pitch-reduced spacers between dense interconnect lines in the circuit array region, and a metal layer mask, or "metal", is used to define the interconnect pattern in the circuit periphery region.

[0067] In an exemplary embodiment, the design rules for defining the spacer and metal are based on two scaling factors. For a given lithography, F is the minimum feature size that can be resolved, and D is the maximum misalignment allowed between the two masks. The variable x is a pitch multiplication scaling constant corresponding to a feature size of the spacer loops used to define the metal lines ($0 < x < 1$). Because a single pitch-multiplication technique is used, the actual interconnect pitch achievable using the techniques disclosed herein is F.

[0068] In one embodiment, the spacer loops are drawn in a plurality of distinct closed loops that to not overlap or cross. Two exemplary spacer loops 140 are illustrated in Figure 15, which is a top view of an exemplary in-process integrated circuit simplified for illustration. As illustrated, the spacer loops have a minimum width of xF, and have a minimum space of $(1-x)F$.

[0069] In such embodiments, a plurality of metal features 144 are defined by a plurality of spacer loops 140. Because a damascene process is used in the preferred embodiments, the gaps between the spacer loops, some of which are enclosed and some of which are not, define the metal features 144 that will subsequently be deposited (for example, by physical vapor deposition or chemical vapor deposition) or electroplated with

conductive material. In addition, metal features 142 are defined only one side by the spacer loops 140. The metal features 144 that are defined on both sides by the spacer loops 140 have a minimum width of $(1-x)F$. The metal features 142 that are defined on only one side by a spacer loop 140 have a minimum width of $((1-x)F + D)$. Metal features can also be formed without restriction by a spacer loop 140 with a minimum width corresponding to the minimum resolution of the lithography technique F. As illustrated in Figure 15, the metal features 144 have a minimum spacing of xF if separated by a spacer loop 140, and the metal features 142 have a minimum spacing of F if separated by empty space or by a spacer loop 140 on only one side. If a metal feature 142 or 144 is present on both sides of a spacer loop 140, then the metal is drawn in contact with (that is, the metal occupies directly adjacent real estate with) the spacer loop 140. If the metal feature 142 is present on only one side of the spacer loop 140, then a minimum space of $\min(D-xF, 0)$ separates the metal feature 144 from the spacer loop 140.

[0070] The circuit design rules expounded herein are based on the integrated circuit fabrication techniques disclosed herein. In particular, using an oversized spacer mask to define subsequently pitch-reduced features limits the spacing of metal lines that are defined by the pitch-reduced features.

[0071] Separately defining the metal and spacer layers according to the rules provided by the exemplary embodiments disclosed herein allows circuit designers to build an integrated circuit based on the actual circuit features that will appear on the wafer. These rules advantageously account for the inherent limitations that arise when pitch multiplication techniques are used to form circuit features. The use of the scaling parameter x allows these design rules to work with future pitch multiplication technologies capable of producing smaller feature sizes.

[0072] Certain embodiments disclosed herein are usable to form a wide variety of integrated circuits. Examples of such integrated circuits include, but are not limited to, circuits having arrays of electrical devices, such as memory cell arrays for volatile and non-volatile memory devices such as DRAM, ROM or flash memory, NAND flash memory, and integrated circuits having logic or gate arrays. For example, the logic array can be a field programmable gate array ("FPGA") having a core array similar to a memory array and a periphery with supporting logic circuitry. Therefore, the integrated circuit formed using the techniques disclosed herein can be, for example, a memory chip

or a processor, which can include both a logic array and embedded memory, or other integrated circuits having a logic or gate array.

Scope of the Invention

[0073] While the foregoing detailed description discloses several embodiments of the present invention, it should be understood that this disclosure is illustrative only and is not limiting of the present invention. It should be appreciated that the specific configurations and operations disclosed can differ from those described above, and that the methods described herein can be used in contexts other than integrated circuit fabrication.

WE CLAIM:

1. A method for defining patterns in an integrated circuit, the method comprising:

defining a plurality of features in a first photoresist layer using photolithography over a first region of a substrate;

using pitch multiplication to produce at least two features in a lower masking layer for each feature in the photoresist layer, the features in the lower masking layer including looped ends;

covering with a second photoresist layer a second region of the substrate including the looped ends in the lower masking layer; and

etching a pattern of trenches in the substrate through the features in the lower masking layer without etching in the second region, the trenches having a trench width.

2. The method of Claim 1, wherein the features in the lower masking layer have a feature size between approximately 30 nm and approximately 100 nm.

3. The method of Claim 1, wherein the features in the lower masking layer have a feature size between approximately 32.5 nm and approximately 65 nm.

4. The method of Claim 1, wherein the substrate includes a component array including a plurality of electrical components, each having a feature size substantially equal to the trench width.

5. The method of Claim 1, wherein the integrated circuit is a flash memory device.

6. The method of Claim 1, wherein defining the features in the first photoresist layer comprises performing photolithography with light having a wavelength chosen from the group consisting of 157 nm, 193 nm, 248 nm or 365 nm.

7. The method of Claim 1, wherein the first and second photoresist layer comprise the same photoresist material.

8. The method of Claim 1, wherein using pitch multiplication comprises:

depositing a spacer material over the features in the first photoresist layer; and

isotropically etching the spacer material.

9. The method of Claim 1, wherein the substrate is an insulator.

10. The method of Claim 1, wherein etching is conducted while the second photoresist layer covers the second region.

11. The method of Claim 1, further comprising patterning the second photoresist layer in a third region of the substrate.

12. The method of Claim 11, wherein the first region includes an array region of a memory device, and the third region includes a periphery region of the memory device.

13. The method of Claim 12, wherein the third region includes an interconnect area in the second photoresist layer adjacent the features in the lower masking layer, wherein a metal is subsequently deposited in the interconnect area to provide an electrical connection from the periphery region of the memory device.

14. The method of Claim 1, wherein the trenches are formed in an insulating layer of the substrate, and further comprising:

filling the trenches with a metal layer; and

forming a planar surface on the metal layer down to the insulating layer in a damascene process.

15. A method of making a plurality of conductive lines in an array, the method comprising:

providing a film stack including a substrate in contact with a plurality of conductive plugs, an insulating film overlying the conductive plugs, a lower mask layer overlying the insulating film, and an array of spacers formed over the lower mask layer;

depositing a sacrificial film over the lower mask layer and the array of spacers;

forming a resist mask over a portion of the sacrificial film, the resist mask defining an opening over the array of spacers, wherein the lower mask layer and the sacrificial film can be etched selectively with respect to the resist mask;

etching the sacrificial film and exposing a portion of the lower mask layer;

etching the lower mask layer and exposing a portion of the insulating film;

etching a plurality of trenches in the exposed portion of the insulating film to expose at least a portion of the conductive plugs;

performing a metal deposition into the plurality of trenches; and

forming a planar surface alternating between the metal and the insulating film in a damascene process.

16. The method of Claim 15, wherein the trenches form an array of overhead bit lines.

17. The method of Claim 15, further comprising removing the spacer array before etching the plurality of trenches.

18. The method of Claim 15, further comprising removing the spacer array, the resist mask and the sacrificial film before etching the plurality of trenches.

19. The method of Claim 15, wherein the array of spacers has a plurality of looped ends, and wherein the resist mask covers the looped ends of the spacer array.

20. The method of Claim 15, wherein the array is a memory array.

21. The method of Claim 15, wherein the array is a logic array.

22. The method of Claim 15, wherein the sacrificial film is an insulating film.

23. The method of Claim 15, wherein the sacrificial film is a bottom antireflective coating.

24. The method of Claim 15, wherein the spacers are selected from the group consisting of silicon oxide, silicon nitride, polycrystalline silicon, and carbon.

25. The method of Claim 15, wherein the spacers are deposited using an atomic layer deposition process.

26. The method of Claim 15, wherein the spacers are deposited at a temperature that is less than approximately 400°C.

27. The method of Claim 15, wherein the spacers have a feature size between approximately 30 nm and approximately 100 nm.

28. The method of Claim 15, wherein the spacers have a feature size between approximately 32.5 nm and approximately 65 nm.

29. The method of Claim 15, wherein the spacers have a feature size substantially equal to a feature size of the conductive plugs.

30. The method of Claim 15, wherein the sacrificial film forms a substantially planar surface over the array of spacers.

31. A method of pitch multiplication for damascene features in an integrated circuit, the method comprising:

providing a substrate;

performing a first masking process to define an array of spacer lines over the substrate, the spacer lines separated by a plurality of gaps;

performing a second masking process that blocks a portion of the spacer lines and that defines a plurality of interconnects in a logic region of the integrated circuit;

etching a plurality of trenches in the gaps between the spacer lines except in the blocked portion;

depositing a metal layer to form a plurality of metal lines in the trenches; and

providing a planar surface on the metal layer to isolate the metal lines in the trenches.

32. The method of Claim 31, wherein the spacer lines have a plurality of looped ends, and wherein the looped ends of the spacer lines are blocked.

33. The method of Claim 31, wherein the integrated circuit is a flash memory device.

34. The method of Claim 31, further comprising connecting the interconnects with a periphery region of the integrated circuit.

35. The method of Claim 31, wherein the spacer lines and the gaps have substantially the same width.

36. The method of Claim 31, wherein the spacer lines comprise an oxide material.

37. A method of forming integrated circuit components on a substrate, the method comprising:

using a lithographic technique to pattern a first resist layer and define a plurality of lines;

using a pitch multiplication technique to form a pattern of spacers around a region defined by the plurality of lines, wherein the spacers comprise elongate loops having loop ends;

depositing a second resist layer over the loop ends to define a blocked region of the substrate; and

selectively etching through the spacers to from a plurality of trenches in the substrate without etching in the blocked regions.

38. The method of Claim 37, further comprising:

transferring a pattern of the blocked region from the second resist layer to a hard mask layer; and

removing the second resist layer before etching the trenches..

39. The method of Claim 37, wherein the second resist layer comprises amorphous carbon.

40. The method of Claim 37, wherein the substrate includes an upper insulator.

41. The method of Claim 37, wherein the first and second resist layers comprise the same resist material.

42. The method of Claim 37, wherein the spacers have a feature size between approximately 22 nm and approximately 45 nm.

43. The method of Claim 37, wherein the spacers have a feature size between approximately 30 nm and approximately 100 nm.

44. The method of Claim 43, wherein the spacers have a feature size between approximately 32.5 nm and approximately 65 nm.

45. The method of Claim 37, wherein the spacers have a feature size substantially equal to a feature size of the trenches.

46. The method of Claim 37, further comprising:

depositing a metal layer into and over the trenches; and

planarizing on the metal layer to form a planar surface that alternates between the metal and an insulator.

47. The method of Claim 46, wherein the metal layer is deposited in an electroplating process.

48. The method of Claim 46, wherein the metal layer comprises a conductor selected from the group consisting of copper and nickel.

49. The method of Claim 37, further comprising patterning the second resist layer in a peripheral region of the substrate adjacent to an array region, wherein the spacers are formed in the array region of a memory device.

50. The method of Claim 37, wherein the integrated circuit components form a flash memory device.

51. A partially formed memory device comprising:

a plurality of patterned mask lines in an array region of the memory device, wherein the patterned mask lines form closed loop ends; and

an optically definable material overlying a portion of the mask lines, including the closed loop ends, wherein the optically definable material extends into a periphery region of the integrated circuit, and further defines a plurality of features in the periphery region.

52. The partially formed memory device of Claim 51, wherein the patterned mask lines overlie a substrate.

53. The partially formed memory device of Claim 51, wherein the patterned mask lines comprise silicon.

54. The partially formed memory device of Claim 51, wherein the patterned mask lines comprise silicon oxide or silicon nitride spacers.

55. The partially formed memory device of Claim 51, wherein the patterned mask lines overlie a substrate that includes an array of conductive lines.

56. The partially formed memory device of Claim 51, wherein the patterned mask lines have a feature size between approximately 30 nm and approximately 100 nm.

57. The partially formed memory device of Claim 51, wherein the patterned mask lines have a feature size between approximately 32.5 nm and approximately 65 nm.

58. The partially formed memory device of Claim 51, wherein the optically definable material comprises photoresist.

59. The partially formed memory device of Claim 51, wherein the patterned mask lines are pitch-multiplied spacer lines.

60. A method of defining an interconnect pattern in an integrated circuit, the method comprising:

designing a plurality of pitch multiplied closed spacer loops that do not overlap each other, wherein

the lithography technique is capable of resolving spacer loops having a minimum feature size F,

the plurality of spacer loops have a loop width xF that is substantially constant, with x defining a pitch multiplication scaling constant corresponding to a feature size of the spacer loops, and

the spacer loops are separated from each other by a variable gap distance, the minimum gap distance being $(1-x)$F; and

define a pattern of metal interconnects to be formed in a damascene process, wherein the pattern of metal interconnects configured to connect to the gaps separating the spacer loops, wherein

the metal interconnects have a minimum width $(1-x)F$ if separated from a spacer loop on two sides, have a minimum width $((1-x)F+D)$ if separated from a spacer loop on one side, and have a minimum width F if spatially unrestricted by a spacer loop, with D defining a maximum misalignment between the spacer loops and the metal interconnects, and

the metal interconnects are separated from each other by a minimum spacing of xF if separated by a spacer and of F if not separated by a spacer.

61. The method of Claim 60, wherein if metal interconnects are present on two sides of one of the plurality of spacer loops, the metal is designed to contact the spacer loop.

62. The method of Claim 60, wherein if metal interconnects are present on one size of one of the plurality of spacer loops, a minimum spacing of $\min(D-xF, 0)$ is designed to separate the metal interconnect and the spacer loop.

63. A masking process comprising:

providing a substrate;

defining a first pattern over a first region of the substrate using a pitch multiplication technique, the first pattern including at least one pair of features connected by a looped end connection;

defining a second pattern over a second region of the substrate; and

defining a derivative pattern of the first pattern, wherein a pair of features corresponding to the at least one pair of features are not connected by the looped end connection;

wherein the first pattern, the second pattern, and the derivative pattern are defined by two masks.

64. The masking process of Claim 63, wherein:

the second region of the substrate is a logic region of an integrated circuit; and

the second pattern defines a plurality of interconnects in the logic region.

65. The masking process of Claim 63, wherein:

the features are separated from each other by a gap having a gap width; and

the features have a feature width that is substantially equal to the gap width.

66. The masking process of Claim 63, wherein the looped end connection is omitted in forming the derivative pattern by performing an etching process using one of the two masks.

67. The masking process of Claim 63, wherein the first and second patterns are defined using photolithographic processes.

68. A method of forming a memory device that includes an array region and a peripheral region, the method comprising:

defining a plurality of patterned mask loops in the array region, the patterned mask loops being separated from each other by a gap region;

overlying a lithographic mask over a portion of the array region and at least a portion of a peripheral region, wherein the lithographic mask covers at least a portion of the patterned mask loops;

forming a conductive material in a region left exposed by the lithographic mask; and

forming a plurality of contacts over the conductive material, wherein at least one of the plurality of contacts is positioned within the patterned mask loops, and wherein at least one of the plurality of contacts is positioned in the gap region separating the patterned mask loops.

69. The method of Claim 68, wherein the lithographic mask intersects the plurality of patterned mask loops at a right angle.

70. The method of Claim 68, wherein a portion of the plurality of patterned mask loops has a first loop width in a first region, and has a second loop width in a second region, wherein the second loop width is greater than the first loop width.

71. The method of Claim 70, wherein a contact is positioned in the second region.

72. The method of Claim 68, wherein the plurality of patterned mask loops comprise silicon oxide or silicon nitride.

73. The method of Claim 68, further comprising connecting at least a portion of the plurality of contacts to an array of conductive lines.