

A pulse width modulation system and a method in relation thereto

Technical field

5 The present disclosure relates to a pulse width modulation system and a method in a pulse width modulation system, and in particular to a system and method using so called soft synchronization of timing between control modules. The system and method is advantageously applied in rail-bound vehicles.

Background

10 Pulse width modulation (PWM) is a method of reducing the average power delivered by an electrical signal, by effectively chopping it up into discrete parts.

In a pulse width modulation system a number of racks are normally provided, each comprising a number of control boards. Each control board is configured to control a
15 module building block that in turn is provided with a number of function modules. Each function module is configured to power and control a load using pulse width modulation. The load may e.g. be one or several traction motors connected in parallel; an auxiliary transformer; a brake chopper resistor; a step-up chopper, and a main transformer winding, for AC system with line converter. The various loads connected to the different module
20 building blocks must be controlled and energized with respect to each other such that the power outtake is relatively even over time. Therefore is the synchronization of the timing applied by the different control boards used to control the functional modules of a rack very important.

The control boards are connected to each other by a communication bus, e.g. an inter
25 converter serial bus (ICE-bus). Conventionally, so-called hard synchronization is applied which means that the clock rate and timer values of the control boards at the same rack are kept the same.

One disadvantage of applying hard synchronization is that the control boards have to be restarted in a certain order in order to get interrupts running.

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More particularly, at the root of the problem is the interrupt handling. For hard synchronized timers, each board needs to change its timer value to get in synchronization

with the master board. However, changing the timer value cannot be done independently from the interrupt handling process.

5 The method to synchronize the board timers and interlace the PWM outputs is relevant to be able to reduce the size of the dc-link capacitor. This is beneficial for both SiC or Si based modules. It could become more important for SiC based inverters as they could be built smaller, due to reduced losses and then the relative size of the capacitor increases.

10 One purpose of the traction convertor is to convert DC voltage to a variable voltage and a variable frequency, e.g. adapted to the engines. A rapid and accurate control of the engine torque may thereby be achieved such that the train have a smooth movement.

15 Related background technology is disclosed in US-2009/0184742 that relates to externally synchronizing multiphase pulse width modulation signals.

The object of the present invention is to achieve an improved pulse width modulation system where the above disadvantage is removed.

Summary

20 The above-mentioned object is achieved by the present invention according to the independent claims.

Preferred embodiments are set forth in the dependent claims.

25 The present invention relates to soft synchronized control board timers.
The benefit of providing soft synchronized control board timers according to the present invention, is that it allows for restarts of the master control board (clock reference board) without having to change the timer (i.e. change interrupts) of the slave control boards. In a soft synchronized system, as the master boards starts up or is changed, the slave boards
30 resynchronize their clock rate towards the clock rate of the master board and updates the offset to the master board timer. The offset towards the master control board is then used to re-interlace the PWMs running on the slave control boards.

By applying the solution according to the present invention, an interlacing procedure may be performed independently of the interrupt handling, which is advantageous.

In addition, it enables to interlace PWMs running on oversampling interrupts.

- 5 Thus, one of the control boards is designated a master control board and the others are slave control boards. The roles of the control boards may change from time to time, and different control boards may take the role of being the master control board.
- For each slave control board is determined a fictive master control board timer based upon a timer offset in relation to the master board timer, wherein the timer offset is received
- 10 from the master control board via a communication bus, e.g. an inter converter serial bus (ICE-bus). By fictive master board timer is meant a re-constructed master timer. The exact value of the master timer is not known, but through the fictive master board timer the value of the master timer is known sufficiently correct.
- The clock rates of slave timers of the slave control boards are adapted to the clock rate of
- 15 the master control board, as it makes it possible to get a relative correct interlacing even though the individual control boards may have different absolute reference timer values.
- By applying the present invention, it is facilitated to interlace PWM connected to the communication bus without having issues related to control board restarts or to handle change of interrupts. The same method may be applied to interlace PWM used by e.g. a
- 20 motor controller.

Brief description of the drawings

Figure 1 is a block diagram schematically illustrating the pulse width modulation system according to the present invention.

- 25 Figure 2 is a block diagram schematically illustrating a rack including control boards according to the present invention.

Figure 3 illustrates a clock pulse applying hard synchronization.

Figure 4 illustrates a clock pulse applying soft synchronization.

Figure 5 illustrates clock pulses applying hard synchronization.

- 30 Figure 6 illustrates clock pulses applying soft synchronization.

Figure 7 is a flow diagram of the method according to the present invention.

Detailed description

The pulse width modulation system, and the method, will now be described in detail with references to the appended figures. Throughout the figures the same, or similar, items have the same reference signs. Moreover, the items and the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

Figures 3-6 show various pulse trains where c1-c4 designate points of time for interlacing points (also referred to as synchronization point), and θ designates an interlacing angle.

Figure 3 illustrates hard synchronized master and slave control board timers.

Regardless of interrupt method, the control boards need a method to synchronize clocks, so that the interlacing points occur correct in physical time. As discussed above, if the control board share the same timer and clock value then the boards are hard synchronized. For hard synchronized boards, the interrupt (interlacing point) can be shifted for the slave board to achieve the desired interlacing angle θ . In figure 3 is also shown the on and off of the PWM, the interrupts, and the digital signal processor (DSP) code execution performed after each interrupt.

Figure 4 illustrates soft synchronized master and slave control board timers having different timers but have same clock frequency.

In case the boards are soft synchronized, the clocks are controlled such that there exist a near constant offset between the control board timers.

In figure 5 is illustrated a pulse train in a pulse width modulation system, where an interlacing point is illustrated for a master board timer and a slave board timer. The interlacing angle, denoted θ , is also indicated. The interlacing angle θ is applied to define the timing between different connected loads.

The interlacing point is normally symmetrically located on the pulse, i.e. having essentially equal time length to the leading and lagging edge of the pulse. However, the position of the interlacing point may be freely chosen within the PWM period, positive or negative zero vector is preferable. The zero vector point is relatively shifted in time to achieve a certain harmonic spectrum.

One alternative is to run the interrupts in the middle of the pulse period and in this case the zero vector/interlacing point can coincide with the interrupt. The interlacing angles can then be controlled by controlling the interrupt points.

Another alternative is to use an oversampling task and let the interrupts run faster than the pulse period. In this case the zero vector/interlacing point needs to be controlled by the PWM control boards.

As stated above, regardless of interrupt method, the control boards need a method to synchronize clocks, so that the interlacing points occur correct in physical time.

Hard synchronized pulse trains for a master and slave timer are illustrated in figure 5. For hard synchronized boards the interrupt and thereby the interlacing point can be shifted for the slave board to achieve the desired interlacing angle, denoted θ .

If the control boards have different timers, i.e. each control board has its own timer, but have the same clock frequency, the boards are considered to be soft synchronized. This is illustrated in figure 6. As mentioned above, the present invention relates to soft synchronized control board timers. Relationships between the timing of interlacing points c_1 - c_4 , the offset, and the interlacing angle θ are shown in figure 6.

Now with references to the block diagrams of figures 1 and 2, a pulse width modulation system 2 comprising a plurality of module building blocks 4₁-4₄ is provided. The number of module building blocks is in the disclosed example four, but may naturally be higher or lower.

Each building block 4₁-4₄ is connected to, and controlled by a control board 6₁-6₄, and each module building block comprises a set of function modules 8₁-8₅, provided with pulse width modulated phase outputs 10₁-10₅ adapted to be connected to predetermined loads. The control boards 6₁-6₄ are preferably located in a rack 20.

A single control board thus controls a configurable number of function modules in one module building block, depending on the application.

The loads connected to the function modules may be one or many of the following: one or several traction motors, e.g. connected in parallel; an auxiliary transformer; a brake chopper resistor; a step-up chopper, and a main transformer winding, for AC system with line converter.

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Furthermore, each module building block 4₁-4₄ is connected to a direct current (DC) link, and that the control boards 6₁-6₄ are connected to each other via a communication bus 12, preferably an inter converter serial bus (ICE-bus).

10 In an exemplary setup, the pulse width modulation system 2 comprises four module building blocks - three for a motor converter and one for a brake chopper. The latter has the task of taking care of the energy from braking motors in cases where the energy cannot be supplied back to the line voltage.

15 The control boards use a pulse width modulation method to control the pulse width modulated phase outputs 10₁-10₅, i.e. the output of each of the function modules in a module building block. Depending on the application and type of PWM method, it is desirable to control the phase of the harmonics in relation to the other control boards connected to the same communication bus.

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One of the control boards is a master control board 6₁ and the others are slave control boards 6₂, 6₃, 6₄.

25 The master control board 6₁ comprises a master board timer 14₁ (see figure 2) configured to generate a clock signal having a master timer rate, wherein each of the slave control boards 6₂, 6₃, 6₄ comprises a slave board timer 14₂, 14₃, 14₄.

Each slave control board 6₂, 6₃, 6₄ is configured to determine a fictive master board timer based upon timer information received from the master control board 6₁ via the
30 communication bus 12, and is further configured to synchronize the timer rate of the slave board timer 14₂, 14₃, 14₄ to the master timer rate.

In addition, the timer information also comprises timer offset information defining a time offset between the master board timer 14₁ and each of the slave board timers 14₂, 14₃, 14₄. Each of the slave control board 6₂, 6₃, 6₄ is then configured to apply the received time offset in the control of the pulse width modulated phase outputs 10₁-10₅, such that the position of a slave pulse width modulated phase output signal of the function module is controlled in relation to the fictive master board timer.

According to one embodiment, the slave board timers 14₂, 14₃, 14₄ are configured to continue running independently if the master board timer 14₁ is running or not, using the lastly received master timer rate and timer offset, and to resynchronize to the master timer rate, and to update the timer offset, when the master board timer 14₁ restarts, or changes.

In a further embodiment, each control board 6₁-6₄ is configured to control the set of function modules 8₁-8₅ being e.g. IGBT or MOSFET modules, in the module building block 4₁-4₄ using an optical protocol communication line 16₁-16₅ and applying a gate drive unit 18₁-18₅ for each module in the module building block 4₁-4₄.

In one exemplary function module it comprises two SiC-MOSFETs and two SiC-Schottky diodes that handle 1700 V and 2×900 A. They work in pairs, an upper and a lower, which together form a phase leg. When one leads, the other is off and vice versa. This is how you may control e.g. the power to the motors. The switching frequency may be several kHz.

The present invention also relates to method in a pulse width modulation system 2, which has been described in detail above, and it is herein referred to that description.

Thus, the pulse width modulation system comprises a plurality of module building blocks 4₁-4₄, where each building block is connected to and controlled by a control board 6₁-6₄. Each module building block comprises a set of function modules 8₁-8₅, provided with pulse width modulated phase outputs 10₁-10₅ adapted to be connected to predetermined loads, and that each module building block 4₁-4₄ is connected to a direct current (DC) link.

The control boards 6₁-6₄ are connected to each other via a communication bus 12, preferably an inter converter serial bus (ICE-bus).

One of the control boards is a master control board 6₁ and the others are slave control

boards 6₂, 6₃, 6₄. The master control board 6₁ comprises a master board timer 14₁ configured to generate a clock signal having a master timer rate, wherein each of the slave control boards 6₂, 6₃, 6₄ comprises a slave board timer 14₂, 14₃, 14₄.

- 5 With references to the flow diagram shown in figure 7, the method comprises:
- determining, by each slave control board 6₂, 6₃, 6₄, a fictive master board timer based upon timer information received from said master control board 6₁ via the communication bus 12,
 - synchronizing the timer rate of the slave board timer 14₂, 14₃, 14₄ to the master timer rate.
- 10 The timer information also comprises timer offset information defining a time offset between the master board timer 14₁ and the slave board timer 14₂, 14₃, 14₄. The method further comprises:
- applying, by each slave control boards 6₂, 6₃, 6₄ the time offset when controlling the pulse width modulated phase outputs 10₁-10₅, such that the position of a slave pulse width
- 15 modulated phase output signal is controlled in relation to the fictive master board timer.

According to a further embodiment, illustrated by a dashed box in the flow diagram of figure 5, the method also comprises continue running the slave board timers 14₂, 14₃, 14₄ independently if the master board timer 14₁ is running or not, using the lastly received

20 master timer rate and timer offset, and resynchronizing to the master timer rate, and updating the timer offset, when the master board timer 14₁ restarts, or changes.

The present invention also relates to a rail-bound vehicle comprising one or many pulse width modulation systems as described above.

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The present invention is not limited to the above-described preferred embodiments. Various alternatives, modifications and equivalents may be used. Therefore, the above embodiments should not be taken as limiting the scope of the invention, which is defined by the appending claims.

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Claims

1. A pulse width modulation system (2) comprising a plurality of module building blocks (4₁-4₄), where each building block is connected to and controlled by a control board (6₁-6₄), each module building block comprises a set of function modules (8₁-8₅), provided with pulse width modulated phase outputs (10₁-10₅) adapted to be connected to predetermined loads, and wherein each module building block (4₁-4₄) is connected to a direct current (DC) link, and that the control boards (6₁-6₄) are connected to each other via a communication bus (12),
- one of the control boards is a master control board (6₁) and the others are slave control boards (6₂, 6₃, 6₄), the master control board (6₁) comprises a master board timer (14₁) configured to generate a clock signal having a master timer rate, wherein each of the slave control boards (6₂, 6₃, 6₄) comprises a slave board timer (14₂, 14₃, 14₄),
- characterized in that
- each slave control board (6₂, 6₃, 6₄) is configured to determine a fictive master board timer based upon timer information received from said master control board (6₁) via said communication bus (12), and is further configured to synchronize the timer rate of the slave board timer (14₂, 14₃, 14₄) to the master timer rate,
- wherein said timer information also comprises timer offset information defining a time offset between the master board timer (14₁) and the slave board timer (14₂, 14₃, 14₄), and
- wherein the slave control board (6₂, 6₃, 6₄) is configured to apply said time offset in the control of the pulse width modulated phase outputs (10₁-10₅), such that the position of a slave pulse width modulated phase output signal is controlled in relation to the fictive master board timer.
2. The system (2) according to claim 1, wherein said slave board timers (14₂, 14₃, 14₄) are configured to continue running independently if the master board timer (14₁) is running or not, using the lastly received master timer rate and timer offset, and to resynchronize to the master timer rate, and to update the timer offset, when the master board timer (14₁) restarts, or changes.
3. The system (2) according to claim 1 or 2, wherein said communication bus (12) is an inter converter serial bus (ICE-bus).

4. The system (2) according to any of claims 1-3, wherein said loads may comprise one or many of the following:

- one or several traction motors connected in parallel;
- 5 -an auxiliary transformer;
- a brake chopper resistor;
- a step-up chopper, and
- a main transformer winding, for AC system with line converter.

10 5. The system (2) according to any of claims 1-4, wherein each control board (6₁-6₄) is configured to control said set of function modules (8₁-8₅) being IGBT or MOSFET modules, in the module building block (4₁-4₄) using an optical protocol communication line (16₁-16₅) and applying a gate drive unit (18₁-18₅) for each module in the module building block (4₁-4₄).

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6. The system (2) according to any of claims 1-5, wherein said control boards (6₁-6₄) are located in a rack (20).

7. A method in a pulse width modulation system (2) comprising a plurality of
20 module building blocks (4₁-4₄), where each building block is connected to and controlled by a control board (6₁-6₄), each module building block comprises a set of function modules (8₁-8₅), provided with pulse width modulated phase outputs (10₁-10₅) adapted to be connected to predetermined loads, and wherein each module building block (4₁-4₄) is connected to a direct current (DC) link, and that the control boards (6₁-6₄) are connected to
25 each other via a communication bus (12),

one of the control boards is a master control board (6₁) and the others are slave control boards (6₂, 6₃, 6₄), the master control board (6₁) comprises a master board timer (14₁) configured to generate a clock signal having a master timer rate, wherein each of the slave control boards (6₂, 6₃, 6₄) comprises a slave board timer (14₂, 14₃, 14₄),

30 c h a r a c t e r i z e d i n that the method comprises:

- determining, by each slave control board (6₂, 6₃, 6₄), a fictive master board timer based upon timer information received from said master control board (6₁) via said

communication bus (12),
-synchronizing the timer rate of the slave board timer (14₂, 14₃, 14₄) to the master timer rate,
wherein said timer information also comprises timer offset information defining a time
5 offset between the master board timer (14₁) and the slave board timer (14₂, 14₃, 14₄), the method further comprises:
-applying, by each slave control boards (6₂, 6₃, 6₄), said time offset when controlling the pulse width modulated phase outputs (10₁-10₅), such that the position of a slave pulse width modulated phase output signal is controlled in relation to the fictive master board
10 timer.

8. The method according to claim 7, comprising continue running said slave board timers (14₂, 14₃, 14₄) independently if the master board timer (14₁) is running or not, using the lastly received master timer rate and timer offset, and resynchronizing to the
15 master timer rate, and updating the timer offset, when the master board timer (14₁) restarts, or changes.

9. A rail-bound vehicle comprising one or many pulse width modulation systems (2) according to any of claims 1-6.