~~What is claimed is:~~

CLAIMS

1. A device comprising:

a substrate having a device region;

a recess in the substrate; and

a discontinuous layer in the recess comprising quantum dots, wherein the discontinuous layer induces a strain in the substrate.

2. The device of claim 1 wherein the device region comprises a gate of a transistor and a channel beneath the gate.

3. The device of claim 1 wherein the substrate comprises a first material and the discontinuous layer comprises a second material.

4. The device of claim 2 wherein the discontinuous layer is in source/drain regions adjacent to the gate.

5. A device comprising:

a substrate formed from a first material having a transistor region, the transistor region comprises a gate and a channel region under the gate; and

source/drain regions adjacent to the gate, wherein the source/drain regions comprises a first discontinuous layer, the first discontinuous layer comprising quantum dots for inducing a strain in the channel region of the transistor.

~~6. The device of claim 5 wherein the first discontinuous layer comprises a crystalline~~ material.

7. The device of claim 5 wherein the first discontinuous layer of the second material is formed directly on the first material.

8. The device of claim 5 wherein the discontinuous layer is selectively formed on the first material in the source/drain regions.

9. The device of claim 5 wherein the first discontinuous layer is coated with a capping layer.

10. The device of claim 9 wherein the capping layer comprises the first material.

11. The device of claim 10 wherein the capping layer comprises a doped first material.

12. The device of claim 11 wherein the source/drain regions further comprise a second discontinuous layer selectively formed on the capping layer and the first material.

13. The device of claim 5 comprising a multilayer structure of discontinuous layers with a capping layer provided between adjacent discontinuous layers.

14. The device of claim 5 wherein the first material comprises silicon and the second material comprises an alloy having any combination of Si, Ge, In, As, P, C, and Sn, including SiGe, InAs, INP, SiC and SiSn.

~~15. The device of claim 5 wherein the discontinuous layer comprises a doped second~~ material.

16. A device comprising:

a substrate comprising a first material, the substrate includes a device region prepared with a gate of a transistor and a channel beneath the gate; and

a discontinuous layer of a second material only in source/drain regions adjacent to the gate, the discontinuous layer comprises quantum dots, the second material is different from the first material, wherein the discontinuous layer induces a first stress on the channel region.

17. The device of claim 16 wherein the discontinuous layer is selectively formed on the first material in the source/drain regions.

18. The device of claim 17 wherein the discontinuous layer comprises multiple discontinuous layers in the source/drain regions, wherein adjacent discontinuous layers are separated by a capping layer formed over a lower adjacent discontinuous layer.

19. The device of claim 16 wherein the discontinuous layer comprises multiple discontinuous layers in the source/drain regions, wherein adjacent discontinuous layers are separated by a capping layer formed over a lower adjacent discontinuous layer.

20. The device of claim 16 wherein the discontinuous layer comprises a crystalline material.

What is claimed is:

CLAIMS

1. A device comprising:

a substrate comprising a semiconductor material having a device region;

a recess having surfaces which include sidewalls and bottom disposed in the substrate of the device region; and

a plurality of quantum dots lining all the surfaces of the recess comprising the semiconductor material, the quantum dots form a discontinuous layer without filling the recess, wherein the discontinuous layer induces a strain in the substrate.

2. The device of claim 1 wherein the device region comprises a gate of a transistor and a channel beneath the gate.

3. The device of claim 1 wherein the substrate comprises a first material and the discontinuous layer comprises a second material.

4. The device of claim 2 wherein the discontinuous layer lines the sidewall and bottom of first and second recesses adjacent to the gate comprising the semiconductor material, the first and second recesses include source/drain regions of the transistor.

5. A device comprising:

a substrate formed from a first semiconductor material having a transistor region, the transistor region comprises a gate and a channel region under the gate; and

source/drain regions in recesses in the substrate adjacent to the gate, wherein

a recess of the recesses comprises surfaces which include sidewalls and bottom,

the source/drain regions comprises a plurality of quantum dots lining only sidewall and bottom surfaces of the recesses comprising the first semiconductor material, the quantum dots form a first discontinuous layer without filling the recesses, the first discontinuous layer inducing a strain in the channel region of the transistor.

6. The device of claim 5 wherein the first discontinuous layer comprises a crystalline material.

7. The device of claim 5 wherein the first discontinuous layer of a second material is disposed on the first semiconductor material of the substrate.

8. The device of claim 5 wherein the discontinuous layer is selectively disposed on the first semiconductor material in the source/drain regions.

9. The device of claim 5 wherein the first discontinuous layer and exposed sidewalls of the recesses are coated with a capping layer.

10. The device of claim 9 wherein the capping layer comprises the first semiconductor material.

11. The device of claim 10 wherein the capping layer comprises a doped first material.

12. The device of claim 11 wherein the source/drain regions further comprise a second discontinuous layer selectively formed on the capping layer and the first semiconductor material.

13. The device of claim 5 comprising a multilayer structure of discontinuous layers with a capping layer provided between adjacent discontinuous layers.

14. The device of claim 7 wherein the first semiconductor material comprises silicon and the second material comprises an alloy having any combination of Si, Ge, In, As, P, C, and Sn, including SiGe, InAs, INP, SiC and SiSn.

15. The device of claim 5 wherein the discontinuous layer comprises a doped second material.

16. A device comprising:

a substrate comprising a first semiconductor material, the substrate includes a device region prepared with a gate of a transistor and a channel beneath the gate; and

a plurality of quantum dots of a second material in source/drain regions in recesses in the substrate adjacent to the gate, wherein

a recess of the recesses comprises surfaces which include sidewalls and bottom,

the quantum dots lining only the sidewall of the recesses adjacent to the channel and bottom of the recesses having surfaces comprising the first semiconductor material, the quantum dots form a discontinuous layer without filling the recess, the second material is different from the first material, wherein the discontinuous layer induces a first stress on the channel region.

17. The device of claim 16 wherein the discontinuous layer is selectively formed on the first semiconductor material in the source/drain regions.

18. The device of claim 17 wherein the discontinuous layer comprises multiple discontinuous layers in the source/drain regions, wherein adjacent discontinuous layers are separated by a capping layer formed over a lower adjacent discontinuous layer.

19. The device of claim 16 wherein the discontinuous layer comprises multiple discontinuous layers in the source/drain regions, wherein adjacent discontinuous layers are separated by a capping layer formed over a lower adjacent discontinuous layer.

20. The device of claim 16 wherein the discontinuous layer comprises a crystalline material.

21. The device of claim 5 wherein the first discontinuous layer is formed by epitaxial growth.

22. The device of claim 21 wherein the epitaxial growth comprises molecular beam epitaxy.

23. The device of claim 5 wherein the first discontinuous layer is formed by Stranski-Krastanov (SK) mode or Volmer-Weber (VW) mode.

24. The device of claim 5 wherein the recesses further comprise a semiconductor crystalline fill material.

25. The device of claim 16 wherein the first semiconductor material comprises silicon and the second material comprises an alloy having any combination of Si, Ge, In, As, P, C, and Sn, including SiGe, InAs, INP, SiC and SiSn.