METHODS OF MANUFACTURING SEMICONDUCTOR CIRCUIT DEVICES

The present invention relates to a method of manufacturing a semiconductor integrated circuit device having a complementary insulated gate field effect transistor circuit and an integrated injection logic circuit on the same semiconductor substrate.

In prior art publications concerned with a CMISFET-I^2L IC such as United States Patent No. 4122481 or Japanese Patent Laid-Open No. 52482/1979, the CMISFET-I^2L IC is manufactured by a complicated process. Therefore, attempts have been made to form those semiconductor regions which constitute the CMISFET circuit and those semiconductor regions which constitute the I^2L circuit using the same steps as far as possible. For example, according to Japanese Patent Laid-Open No. 52482/1979, the well region for the I^2L and the well region for an N-channel MOSFET are formed simultaneously.

In a CMISFET-I^2L obtained by the above-mentioned method, however, the electrical characteristics

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of either the CMISFET or the I^2L must be sacrificed.

According to the present invention there is provided a method of manufacturing semiconductor integrated circuit devices comprising:

(a) a step of preparing a substrate of a semiconductor of a first conductivity type;

(b) a step of forming first and second semiconductor regions in said semiconductor, said first and second semiconductor regions being separated from each other and being of a second conductivity type that is opposite to said first conductivity type;

(c) a step of selectively oxidizing the substrate after the formation of the first and second semiconductor regions;

(d) a step of forming a plurality of third semiconductor regions having the first conductivity type in said first semiconductor region to form the elements of an I^2L circuit; and

(e) a step of forming a plurality of fourth semiconductor regions having the first type of conductivity in said second semiconductor region to form the elements of a MISFET circuit.

According to a study conducted by the inventors of the present invention, in order to improve the electrical characteristics without reducing the degree of integration, it has been confirmed that the impurity concentration plays a very important role in the emitter region of inverse

transistors that may operate as driver transistors in the I^2L, and in the semiconductor region (well region) where channels may be formed in the CMISFET among the plurality of semiconductor regions that constitute the integrated circuit. These inverse transistors may each have a collector region, a base region and an emitter region formed in the semiconductor substrate in that order from the main surface toward the inside of the substrate. Thus an inverse transistor may be constructed in the opposite way to an ordinary transistor, which is why it is so called.

If the emitter and well regions are formed simultaneously, and the impurity concentration is increased in order to increase the current amplification factor βi of the inverse transistors in an I^2L, the operating frequency of the CMISFET decreases. That is, if the impurity concentration in the well region is high, the depletion layer spreads less easily. Therefore, the junction capacity increases so that the switching operations of the CMISFET are no longer capable of following high-frequency signals. To increase the operating frequency, the gate width of the MISFETs should be increased to increase the current capacity. Therefore, the MISFETs may occupy an increased area and the degree of integration decreases. On the other hand, if the impurity concentrations in these regions are small in order to improve the operating frequency of the CMISFET, the current amplification factor βi becomes small, the operating speed of the I^2L decreases, and the power

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consumption increases.

In Japanese Patent Laid-Open No. 52482/1979, the source and drain regions of the MISFETs are formed prior to the formation of the gate electrodes, and are not self-aligned relative to the gate electrodes. Similarly, the well region in the I^2L and the semiconductor region formed in the well region are not self-aligned, either. Therefore, a sufficient masking margin must be provided. Accordingly, it becomes difficult to obtain CMISFET-I^2L ICs in a highly integrated form.

An embodiment of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is a sectional view of an integrated

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circuit produced by the embodiment;

Figs. 2A to 2H are sectional views of the steps comprising the embodiment.

Fig. 1 is a diagram showing the construction of a CMISFET-I^2L IC fabricated according to an embodiment of the present invention, in which the region X_1 shows the construction of the complementary MISFETs, and the region X_2 shows the construction of the I^2L elements.

As shown in Fig. 1, unlike conventional devices, the integrated circuit of this embodiment makes use of a substrate which is prepared by growing a p-type epitaxial layer 2 of a low impurity concentration on a p-type silicon substrate 1 of a low impurity concentration. Reference number 16 denotes an n^+-type buried layer formed under the well region that will form the I^2L circuit, 3 denotes a first n-type well region of a low concentration formed in the p-type layer 2, and 4 denotes a second n-type well region having an impurity concentration smaller than that of the first n-type well region 3. An I^2L consists of a

p-type injector region 5, a p-type base region 6 of an npn inverse transistor, an n^+-type collector region 7 of the npn inverse transistor and an n^+-type emitter contact region 8 formed in the first n-type well region 3. The n-type well region 3 forms an emitter region for the npn inverse transistor. A p-channel MISFET consists of p^+-type source and drain regions 9 formed in the second n-type well region 4, a gate insulation film 11, and a polycrystalline silicon layer 14 that serves as a gate electrode. An n-channel MISFET consists of n^+-type source and drain regions 10 formed in the p^--type layer where no well region is formed, a gate insulation film 12, and a polycrystalline silicon layer 15 that serves as a gate electrode.

Figs. 2A to 2H are diagrams illustrating the process for producing the integrated circuit of Fig. 1. Complementary MISFETs are formed in the area X_1, and I^2L elements are formed in the area X_2.

Referring to Fig. 2A, first, n-type impurities such as arsenic impurities are selectively introduced into a predetermined portion of a p-type silicon substrate 1 by diffusion techniques or ion implantation techniques, and p-type doped silicon is deposited on the substrate by epitaxial growth to form a p^--type layer 2 (impurity concentration N: 10^{15} atoms/cm^3). At the same time, an n^+-type buried layer 16 is also formed owing to the diffusion of the n-type impurities.

As shown in Fig. 2B, an n-type well region 4 is

selectively formed in the p^--type layer 2 in order to form p-channel MISFETs. In order to selectively form the n-type well region 4, an oxide film 30 of a thickness of 500 angstroms is first formed by thermal oxidation on the whole surface of the p-type epitaxial layer 2, and an Si_3N_4 film 31 of a thickness of 1500 angstroms is formed thereon by the chemical vapor deposition method (hereinafter referred to as the CVD method). Then the oxide film 30 on that portion where the n-type well region is to be formed and the Si_3N_4 film 31, are selectively removed by plasma etching using a photoresist film (not shown) as a mask, such that the surface of the p-type epitaxial layer 2 is exposed. Masks for forming all the n-type well regions are completed in this step so that all the positions of all the well regions are determined by the masks. Thereafter, the windows for forming the n-type well regions that form the low-concentration I^2L are covered with a suitable mask such as a thick photoresist film 32 as shown in Fig. 2B, and n-type impurities such as phosphorus ions are implanted (N: 10^{16} atoms/cm^3) to form the n^--type well region 4 which has a low impurity concentration. Although the impurity concentration is low, the well region 4 should preferably be formed by the ion implantation method since it is possible to control the concentration precisely.

Then, the low-concentration n-type well region 3 is formed as shown in Fig. 2C. After the photoresist film 32 is removed, the n-type well region 4 is covered with a

thick photoresist film 33, and n-type impurities such as phosphorus ions are implanted (N: 10^7 atoms/cm^3) to form the low-concentration n-type well region 3. The well region 3 should preferably be formed by the ion implantation technique since it is possible to control the impurity concentration precisely as mentioned above.

A field oxide film is then formed as shown in Fig. 2D. After the photoresist film 33, the Si_3N_4 film 31 and the SiO_2 film 30 are removed in succession, an oxide film (SiO_2 film) 34 of a thickness of 500 angstroms is formed by thermal oxidation on the exposed surfaces of the epitaxial layer 2, and then an Si_3N_4 film 35 of a thickness of 1500 angstroms is formed by the CVD method. The Si_3N_4 film 35 is then selectively removed by plasma etching using a photoresist film (not shown) as a mask, so that the SiO_2 film 34 is partially exposed. To prevent the formation of an inversion layer under the field oxide film under this condition, p-type impurities such as boron ions are implanted while the photoresist film is still in place. The photoresist film is then removed, and a field oxide film (SiO_2 film) 17 is formed by thermal oxidation to a thickness of 9000 angstroms using the Si_3N_4 film 35, which is not permeable to oxygen, as a mask.

Then, as shown in Fig. 2E, the gate insulation films and the gate electrodes of the MISFETs are formed. After the SiO_2 film 34 and the Si_3N_4 film 35 are removed, a gate insulation film (SiO_2 film) is formed to a thickness of 500

angstroms by thermal oxidation on the whole surface of the exposed epitaxial layer 2. A polycrystalline silicon layer is then formed to a thickness of 3500 angstroms on the whole surface of the substrate by the CVD method. Phosphorus impurities are introduced into the polycrystalline silicon layer by diffusion to decrease its sheet resistance to such a level that it can be used as gate electrodes. To complete the gate electrodes, the polycrystalline silicon layer and the gate insulation film are selectively removed by plasma etching using a photoresist film as a mask. The gate insulation films 11,12 and the gate electrodes 14,15 of the MISFETs are thus completed. At the same time, the surface of the epitaxial layer 2 on the I^2L side is exposed.

Next, a p-type semiconductor region is formed as shown in Fig. 2F. First, to prevent the exposed epitaxial layer 2 from being contaminated, an SiO_2 film 25 is formed to a thickness of 100 to 200 angstroms by thermal oxidation on the surface of the epitaxial layer 2, and also on the surfaces of the polycrystalline silicon layers 14,15. Then an SiO_2 film 36 is formed to a thickness of 1500 angstroms by the CVD method. The SiO_2 film 36 is selectively removed by plasma etching using a photoresist film (not shown) as a mask, to complete the mask for forming the p-type regions. When forming the mask 36, the processing with photoresist does not require so high a precision. That is, the mask may be slightly shifted provided that its ends 36a,36b and

36c are on the field oxide film 17. Then p-type impurities such as boron ions are implanted (or diffused) into the surfaces of the n-type well regions 3,4 not covered by the polycrystalline silicon layer 14, the field oxide film 17 and the mask 36, in order to form the p-type regions 5 and 6 that serve as the injector and base of the I^2L, and to form the p^+-type source and drain regions 9 of the p-channel MISFETs. As will be obvious from Fig. 2F, the p-type region 5 is self-aligned by the field oxide film 17, and the p^+-type source and drain regions 9 are self-aligned by the field oxide film 17 and by the polycrystalline silicon 14.

Next, as shown in Fig. 2G, n-type semiconductor regions are selectively formed in the epitaxial layer 2 and in the n-type well region 3. First, the SiO_2 film 36 is removed, and a new SiO_2 film 37 is formed to a thickness of 1500 angstroms by the CVD method. The SiO_2 film 37 is then selectively removed by plasma etching using a photoresist film (not shown) as a mask, to complete the mask for forming the n-type regions. When forming the mask 37, the processing with photoresist does not require a high precision, as when forming the mask 36. Then n-type impurities such as phosphorus ions are implanted into the surface of the epitaxial layer 2 where the polycrystalline silicon layer 15 and the field oxide film 17 have not been formed, and into the surface of the well region 3 where the mask 37 and the field oxide film 17 have not been

formed, thereby forming the emitter contact region 8 of the I^2L, and the n^+-type source and drain regions 10 of the n-channel MISFETs.

Next, an n-type collector region is formed as shown in Fig. 2H. That is, after the SiO_2 film 37 is removed, a new SiO_2 film 38 is formed to a thickness of 1500 angstroms by the CVD method. The SiO_2 film 38 is then selectively removed by plasma etching using a photoresist film (not shown) as a mask, to complete the mask for forming the n-type collector region. Then n-type impurities such as phosphorus ions are introduced by implantation (or diffusion) to form an n-type collector 7.

After the SiO_2 film 38 is removed, an SiO_2 film 18 (see Fig. 1) is formed on the whole surface of the substrate to a thickness of 1500 angstroms as an interlayer insulation film by the CVD method. After contact holes have been formed in the SiO_2 film 18, aluminum is deposited thereon to a thickness of 8000 angstroms by the vacuum evaporation method. The aluminum layer is patterned to the desired shape to form the aluminum electrodes 19 to 24 that are in ohmic contact with each region. Thus, the CMISFET-I^2L IC of the construction shown in Fig. 1 is completed.

According to this construction, use is made of a p^--type silicon layer of a low impurity concentration as a substrate, and the I^2L circuit and the p-channel MISFETs are formed in the n-type well regions that are separately formed in the substrate. Therefore, the impurity

concentration can be controlled for each of the well regions. By making the impurity concentration in the n-type well region 3 on the I^2L side greater than the impurity concentration of the well region 4, therefore, the inverse current amplification factor βi of the inverse transistors in the I^2L circuit can be enhanced to realize a I^2L which operates at high speeds and which consumes a reduced amount of electric power. With the impurity concentration being made low in the n-type well region 4 on the p-channel MISFET side, furthermore, high-speed operation can be realized even when the gate width of the MISFET is reduced. Accordingly, the chip size can be reduced but the high-speed operation is maintained.

Further, as will be obvious from the method of manufacturing the integrated circuits explained in conjunction with Figs. 2A to 2H, the well regions 3,4 are formed in the epitaxial layer 2 before forming the field oxide film 17 by the selective oxidation technique. In the well region 4 constituting the I^2L, therefore, a field oxide film can be formed in the I^2L elements to prevent the formation of parasitic transistors. The surface of the well region 3 under such a thick field oxide film is difficult to invert. Therefore, a wide range of power-supply voltages can be applied, and increased freedom is provided for laying out the wiring. Further, the surface of the well region 4 is also difficult to invert. Accordingly, the above-mentioned advantages are brought

about.

When forming the CMISFETs, furthermore, employment of the silicon gate processing technique makes it possible to obtain a CMISFET-I^2L IC of a high density.

The invention can further be put into practice in a variety of ways and is not limited to the embodiment described. The high impurity concentration n-type well region where the I^2L circuit will be formed, may be formed in the following manner. Ions are implanted simultaneously with the formation of the n-type well region 4 where the p-channel MISFETs will be formed, and ions are again implanted into the well region 3 while the well region 4 is covered by a mask. The above-mentioned order may of course be reversed. Further, the conductivity types of the semiconductor regions may be reversed.

Another possibility is to have a process wherein the I^2L circuit is formed in an epitaxial layer that is grown on the substrate, and the n-channel MISFETs are formed in the epitaxial layer, in order to increase the local impurity concentration in the epitaxial layer where the I^2L circuit will be formed. That is, use is made of epitaxial layers that are insulated and separated as semiconductor regions that correspond to the well regions in the aforementioned embodiments, and the impurity concentrations are changed.

This application was divided out of U.K. Patent Application NO. 82.27060 (Published under No. 2107117) and contains matter also described in that application. Also divided out of that application was U.K. Patent Application NO. 85.02453 . Attention is drawn to these applications.

CLAIMS:

1. A method of manufacturing semiconductor integrated circuit devices comprising:

(a) a step of preparing a substrate of a semiconductor of a first conductivity type;

(b) a step of forming first and second semiconductor regions in said semiconductor, said first and second semiconductor regions being separated from each other and being of a second conductivity type that is opposite to said first conductivity type;

(c) a step of selectively oxidizing the substrate after the formation of the first and second semiconductor regions;

(d) a step of forming a plurality of third semiconductor regions having the first conductivity type in said first semiconductor region to form the elements of an I^2L circuit; and

(e) a step of forming a plurality of fourth semiconductor regions having the first type of conductivity in said second semiconductor region to form the elements of a MISFET circuit.

2. A method of manufacturing semiconductor integrated circuit devices according to claim 1, wherein the first semiconductor region is formed by introducing impurities of the second conductivity type into the semiconductor of the

first conductivity type such that the impurity concentration therein becomes greater than the impurity concentration in the second semiconductor region.

3. A method of manufacturing semiconductor integrated circuit devices according to claim 2, wherein said impurities are introduced by implanting ions.

4. A method of manufacturing semiconductor integrated circuit devices, substantially as any described herein with reference to the accompanying drawings.