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(54) Title: NANOSHEET TRANSISTOR WITH ASYMMETRIC GATE STACK

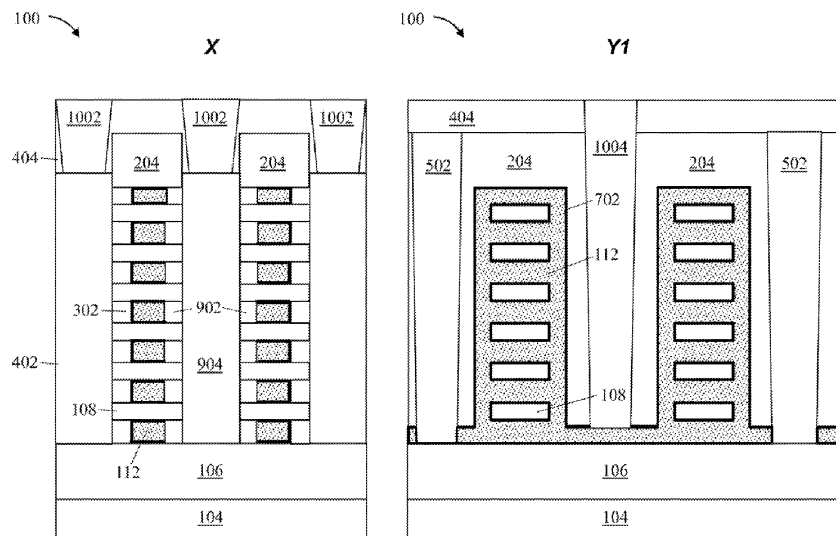


FIG. 10

(57) Abstract: Methods and resulting structures for nanosheet devices having asymmetric gate stacks are disclosed. A nanosheet stack (102) is formed over a substrate (104). The nanosheet stack (102) includes alternating semiconductor layers (108) and sacrificial layers (110). A sacrificial liner (202) is formed over the nanosheet stack (102) and a dielectric gate structure (204) is formed over the nanosheet stack (102) and the sacrificial liner (202). A first inner spacer (302) is formed on a sidewall of the sacrificial layers (110). A gate (112) is formed over channel regions of the nanosheet stack (102). The gate (112) includes a conductive bridge that extends over the substrate (104) in a direction orthogonal to the nanosheet stack (102). A second inner spacer (902) is formed on a sidewall of the gate (112). The first inner spacer (302) is formed prior to the gate (112) stack, while the second inner spacer (902) is formed after, and consequently, the gate (112) stack is asymmetrical.

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