

ABSTRACT

Disclosed in the present invention are a timing calibration method and system. The timing calibration method is used for performing timing calibration on test signals in a plurality of test channels of a digital test machine. The method comprises: gating any two test channels
5 of a digital test machine, so as to output test signals; comparing, by using a window comparator, the test signals output by the two gated test channels, and outputting a comparison result to an FPGA; transmitting, to the FPGA and via a clock buffer, the test signal output by one of the two gated test channels, and taking the test signal as a sampling clock; the FPGA collecting the output result of the window comparator according to the
10 sampling clock, and sending result information to a control terminal; and the control terminal adjusting a clock phase of the test signal in the corresponding test channel according to an output structure of the FPGA, so as to complete timing calibration of the test channel.

15 [Fig. 2]