

The invention concerns a circuit for generating very small currents.

State of the Art

In DE-A-3124289 a circuit is described which contains a current mirror. EP-A-0366253 described a circuit containing a noise-insensitive current mirror for generating a mirrored output current. DE-A-3139166 describes a current source which can be controlled by a current mirror and which has a limiter feature. US-A-4,673,867 describes a current mirror circuit the output current of which has a temperature-dependent behaviour with respect to a reference current. None of these documents contains a staged current mirror for generating very small currents.

Invention

The invention is based on the problem of providing a circuit with which very small currents can be generated. This task is solved by the circuit according to the invention specified in claim 1.

For generating very small currents, for example in the nA range, a multiple current mirroring with the aid of multiple emitters can be utilised, but the currents generated in such a way are dependent upon parameter tolerances and temperature. Apart from that, such circuits require a relatively large chip area if they are implemented in an integrated circuit.

In principle, the solution according to the invention consists of the fact that current mirror means (13, 23, 33) are coupled with means for modifying the amount (14, 24, 34) of the mirrored current, whereby the ratio between a reference current (I_{ref}) fed into the current mirror means and a current (I_{out} , I_{out}') made available by the amount modification means can be adjusted using one or more components (R, R')

contained in the amount modification means, whereby the means for current reflection can contain one or more transistors (13, 23, 28, 33, 38) and the means for modifying the size can contain one or more transistors (14, 24, 27, 34, 37), and the adjustment component contained within the size modification means can consist of one resistor (R) or several resistors (R, R').

Advantageous further developments of the circuit according to the invention result from the subclaims 2 through 9.

The relationship of the reference current of the current mirror circuit to the first output current at the collector of the output transistor can be adjusted by the dimensioning of a first resistance R in the emitter of the output transistor of a current balancing circuit. By adding a second current mirror stage with a second resistor R' contained therein and with a second output current, there results, for $R = R'$, the relationship of the first output current to the second output current corresponding to the relationship of the reference current to the first output current, whereby only a relatively small chip area is necessary when using an integrated circuit.

Advantageously, this reduction of the currents can be further enhanced in that a transistor in the second current mirror stage is incorporated as a multiple transistor.

Drawings

Exemplary embodiments of the invention are described by means of the drawings. The drawings show in:

Fig. 1 a current mirror stage

Fig. 2 a current mirror circuit extended by a second current mirror stage,

Fig. 3 a current mirror circuit extended by a second current mirror stage providing an option of disconnecting the output current.

Exemplary Embodiment

A current mirror circuit with a first current mirror transistor 13 and a first transistor 14 is illustrated in Fig. 1. Starting from an operating voltage 10, the collector of the first current mirror transistor is fed with a reference current I_{ref} via a current source 11. The base and the collector of the first current mirror transistor are connected to the base of the first transistor. The emitter of the first current mirror transistor is connected directly to ground and the emitter of the first transistor is connected to ground via a first resistor R. The open collector of the first transistor supplies the output current I_{out} . The ratio of I_{ref} to I_{out} can be adjusted by the dimensioning of the first resistor R:

$$I_{out} * R = U_r * \ln(I_{ref}/I_{out}),$$

where U_r is the temperature.

Advantageously, I_{out} can be further reduced in that the first transistor 14 is designed as a multiple transistor. Then the following is valid:

$$I_{out} * R = U_r * \ln(I_{ref} * k / I_{out}),$$

where k is the number of transistors connected in parallel in the place of the first transistor.

A graded current mirror circuit having a first current mirror transistor 23 and a first transistor 24 is illustrated in Fig. 2. Starting from an operating voltage 20, the collector of the first current mirror transistor is fed with a reference current I_{ref} via a current source 21. The base and the collector of the first current mirror transistor

are connected to the base of the first transistor and to a second resistor R' . The emitter of the first current mirror transistor is connected directly to ground and the emitter of the first transistor is connected to ground via a first resistor R . The open collector of the first transistor supplies the output current I_{out} .

The other side of the second transistor R' is connected to the base of a second transistor 27 and with collector and base of a second current mirror transistor 28. The emitter of the second current mirror transistor is connected to ground and the emitter of the second transistor is connected to the emitter of the first transistor. The open collector of the second transistor supplies the reduced output current I_{out}' . Then (for $R = R'$) the following is valid:

$$I_{out} * R = U_r * \ln(I_{out}/I_{out}')$$

Advantageously, I_{out}' can be further reduced in that the second current mirror transistor 28 is designed as a multiple transistor. Then ($R = R'$) the following is valid:

$$I_{out} * R = U_r * \ln(I_{ref}/(I_{out}' * n))$$

where n is the number of transistors connected in parallel in the place of the second current mirror transistor.

If not only the first transistor 24 but also the second current mirror transistor 28 is replaced by k , or respectively, n multiple transistors, then (for $R = R'$) the following is valid:

$$I_{out} * R = U_r * \ln(I_{ref} * k / I_{out}),$$

$$I_{out} * R = U_r * \ln(I_{ref} / (I_{out}' * n)).$$

Advantageously, with $R = R'$ and $k = n = 1$, there results for I_{out}/I_{out}' the same current ratio as for I_{ref}/I_{out} .

In this way, current sources, for example, for the range 1 ... 500 nA, can be produced with little chip surface. Such current sources can, for example, be used for producing fully integrated integrator circuits with long integration times, for example, in the range 0.015 ... 0.06 s, and very small integration capacitances, for example, in the range 5 ... 20 pF.

A graded current mirror circuit having a first current mirror transistor 33 and a first transistor 34 is illustrated in Fig. 3. Starting from an operating voltage 30, the collector of the first current mirror transistor is fed with a reference current I_{ref} via a current source 31. The base and the collector of the first current mirror transistor are connected to the base of the first transistor and to a second resistor R' . The emitter of the first current mirror transistor is connected directly to ground and the emitter of the first transistor is connected to ground via a first resistor R . The open collector of the first transistor supplies the output current I_{out} .

The other side of the second resistor R' is connected to the base of a second transistor 37 and to collector and base of a second current mirror transistor 38. The emitter of the second current mirror transistor is connected to ground and the emitter of the second transistor is connected to the emitter of the first transistor. The open collector of the second transistor supplies the reduced output current I_{out}' .

The relationships of Fig. 2 are also valid here but the currents I_{out} and I_{out}' can be disconnected by means of the additional switching current I_{off} . Valid here is:

$$I_{off} * R \text{ approximately } \geq 0.5 \text{ V.}$$



CLAIMS

1. Circuit for generating a reduced current (I_{out}) with means for current reflection (13, 23, 33) and means for modifying the size (14, 24, 34) of the reflected current connected thereto, whereby the ratio of a reference current (I_{ref}) fed into the current reflection means to the reduced current (I_{out}) and can be adjusted using a component (R) contained within the size modification means, characterised in that second current mirror means (28, 38) is connected via a second component (R') to the current reflection means (23, 33) which second means controls second size modification means (27, 37) - in particular a transistor - which is connected to the component (R) in the size modification means and which makes available a current (I_{out}') further reduced compared with the reduced current (I_{out}) and dependent on the reference current (I_{ref}), the further reduced current being variable dependent upon the size of the component (R) and/or the second component (R') in the size modification means, such that in the case of equality of these components the ratio of the reference current (I_{ref}) to the reduced current (I_{out}) is equal to the ratio of the reduced current (I_{out}) to the further reduced current (I_{out}').
2. A circuit according to claim 1, characterised in that the size modifications means contains a transistor or a multiple transistor (24, 34).
3. A circuit according to claim 1 or 2, characterised in that the second current reflection means contains a multiple transistor (28, 38) or a corresponding number of current mirrors connected in parallel.
4. A circuit according to one or more of claims 1 to 3, characterised in that the component and/or the second component is a resistor.
5. A circuit according to one or more of claims 2 to 4, characterised in that the



transistor or the multiple transistor in the size modification means (14, 24, 34) is connected to earth via a resistor (R).

6. A circuit according to one or more of claims 1 to 5, characterised in that the reduced (I_{out}) or the further reduced (I_{out}') current can be switched off by means of a switching current (I_{off}) fed into the size modification means (14, 24, 34) or into the second size modification means (27, 37).

7. A circuit according to one or more of claims 1 to 6, characterised in that the further reduced current (I_{out}') lies in the range 1 nA to 500 nA.

SUMMARY

Conventional current balancing (reflecting) circuits are not optimised for the generation of very small currents in the nA range. In order to generate such currents, multiple current balancing with the aid of multiple emitters can in fact be employed, but the currents generated by this are dependent upon parameter tolerances and temperature. Apart from that, such circuits require a relatively large chip area.

The relationship of the reference current of the current balancing circuit to the first output current at the collector of the output transistor can be adjusted via the dimensioning of a first resistance R in the emitter of the output transistor of a current balancing circuit. By adding a second current balancing circuit with a second resistor R' contained therein with and a second output current, there results, for $R = R'$, the relationship of the first output current to the second output current corresponding to the relationship of the reference current to the first output current.

Fig. 3