18. The method of claim 17, wherein said annealing process comprises at least one of a rapid thermal anneal and a laser spike anneal.

19. The method of claim 17, further comprising forming a silicide at said recess filled with said semiconductor material.

20. The method of claim 7, wherein a plurality of nanowires are formed on a contiguous portion of said first semiconductor layer in the patterning of said second portion of said semiconductor layer, and wherein a channel region of one field effect transistor is formed from said plurality of nanowires, said contiguous portion of said first semiconductor layer providing one of a source and a drain of said field effect transistor.

21. A semiconductor structure formed in accordance with any one of the preceding claims.