

SYSTEM AND METHOD FOR FAST CYCLIC REDUNDANCY CALCULATION

ABSTRACT OF THE DISCLOSURE

Apparatus and methods for rapid cyclic redundancy check calculations in data
5 processing devices. The apparatus comprise a memory, a direct memory access controller
operatively coupled to the memory, and a cyclic redundancy check circuit operatively
coupled to the direct memory access controller, with the direct memory access controller
configured to transfer data from the memory to the cyclic redundancy check circuit, and with
10 the cyclic redundancy check circuit configured to calculate at least one check value for the
data. The methods comprise transferring a data stream from a memory to a cyclic
redundancy check circuit using a direct memory access controller, and calculating a cyclic
redundancy check value for the data stream by the cyclic redundancy check circuit.

Figure 4

