

5 **LIPSEAL EDGE EXCLUSION ENGINEERING TO MAINTAIN**
 MATERIAL INTEGRITY AT WAFER EDGE

INCORPORATION BY REFERENCE

001) A PCT Request Form is filed concurrently with this specification as part of the
10 present application. Each application that the present application claims benefit of or priority
to as identified in the concurrently filed PCT Request Form is incorporated by reference
herein in its entirety and for all purposes.

FIELD OF THE INVENTION

15 **002)** This invention pertains to methods and apparatuses for semiconductor device
manufacturing. Specifically, embodiments of this invention pertain to electrodeposition of
metals, particularly to through-mask electroplating.

BACKGROUND

20 **003)** Through-mask electroplating in semiconductor device fabrication involves
electrodeposition of metals into recessed features that have an exposed conductive layer at
the bottom portions of the recessed features. The sidewalls of the recessed features and the
field region in these substrates are made of a non-conductive mask material, such as
photoresist. During electroplating, the semiconductor substrate is cathodically biased by
25 making an electrical contact to the conductive layer that underlies the mask material and by
applying a negative voltage from a power supply to that layer. The contact is typically made
at the periphery of the semiconductor substrate in the substrate holder assembly.

004) The substrate holder also typically includes a cup holding the semiconductor
substrate and an elastomeric lipseal, which seals the outer edge and backside of the wafer
30 substrate from an electrolyte. During electroplating the cathodically biased substrate is
brought into contact with an electrolyte, which causes electrochemical reduction of ions
contained in the electrolyte upon contact with the cathodically biased metal on the
semiconductor substrate. In some applications, such as in wafer level packaging (WLP) two
metals such as tin and silver are electroplated using an electrolyte containing tin and silver
35 ions. The formed tin-silver (SnAg) bumps can then be used for soldering several substrates
together.

5 **005)** The background description provided herein is for the purposes of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent it is described in this background section, as well as aspects of the description that may not otherwise qualify as prior art at the time of filing, are neither expressly nor impliedly admitted as prior art against the present disclosure.

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SUMMARY

006) Methods and apparatuses for sequential electrodeposition of metals into through-mask recessed features on semiconductor substrates are provided. Provided methods can be used to reduce deleterious consequences of mask material damage during sequential electroplating.

007) In one aspect, a method of electrodepositing a metal onto a semiconductor substrate having a plurality of through-mask recessed features, is provided. The method includes: (a) electrodepositing a first metal into the recessed through-mask features of the semiconductor substrate, without fully filling the recessed through-mask features, in a first electroplating cell using a first lipseal, wherein the first lipseal contacts the semiconductor substrate at a periphery of the semiconductor substrate, and wherein an innermost point of contact between the first lipseal and the semiconductor substrate is located at a first distance from an edge of the semiconductor substrate; and (b) electrodepositing a second metal into the recessed through-mask features of the semiconductor substrate after (a), in a second electroplating cell using a second lipseal, wherein the second lipseal contacts the semiconductor substrate at a periphery of the semiconductor substrate, wherein an innermost point of contact between the second lipseal and the semiconductor substrate is located at a second distance from the edge of the semiconductor substrate, and wherein the second distance is greater than the first distance. In some embodiments the mask material is a photoresist, and the first and second lipseals contact the photoresist material on the semiconductor substrate. In some embodiments electrodeposition of the second metal does not result in protrusion of the electrodeposited second metal above a level of a mask material.

008) In some embodiments, after the first metal has been electrodeposited, the method includes releasing the semiconductor substrate from contact with the first lipseal after, and leaving the semiconductor substrate without contact with a lipseal for a period of time (e.g., at least one hour) prior to electroplating the second metal.

5 **009)** The methods are particularly useful when deposition of the first metal is carried out in a warm electrolyte, because warm electrolyte is more likely to lead to damage of the mask material near the lipseal. In one embodiment the first metal is electrodeposited in a plating bath (electrolyte) having a temperature of greater than 25 °C, such as greater than 40 °C. In one specific implementation, the first metal is nickel, and the nickel is electrodeposited using a plating bath having a temperature of greater than 25 °C, such as greater than 40 °C.

10 **0010)** In one embodiment, the first metal is nickel, and the second metal is tin or a combination of tin and silver. In some embodiments, the first metal is nickel, the second metal is tin or a combination of tin and silver, and the method additionally includes electrodepositing copper into the recessed through-mask features prior to electrodeposition of nickel.

15 **0011)** In some embodiments, the first lipseal and the second lipseal are different lipseals, and the second lipseal has a smaller diameter than the first lipseal (referring to inner diameters of the lipseals).

20 **0012)** In an alternative embodiment, the first lipseal and the second lipseal is the same lipseal that is configured to be adjusted to contact the substrate at different positions.

0013) In one embodiment, the semiconductor substrate used during sequential deposition of metals is a partially fabricated high bandwidth memory (HBM) device.

25 **0014)** In some embodiments provided methods further include the steps of: applying photoresist to the semiconductor substrate; exposing the photoresist to light; patterning the photoresist and transferring the pattern to the semiconductor substrate; and selectively removing the photoresist from the semiconductor substrate.

0015) In another aspect, a system for electroplating a metal onto a semiconductor substrate is provided. The system includes: (a) a first electroplating apparatus configured for electrodepositing a first metal onto the semiconductor substrate, the first electroplating apparatus comprising a substrate holder having a first lipseal; (b) a second electroplating apparatus configured for electrodepositing a second metal onto the semiconductor substrate, the second electroplating apparatus comprising a substrate holder having a second lipseal, wherein the second lipseal has a smaller diameter than the first lipseal; and (c) a controller comprising program instructions. The program instructions are configured to cause the steps of: (i) electroplating the first metal in the first electroplating apparatus to partially fill through-mask recessed features on the semiconductor substrate; and (ii) electroplating the second metal in the second electroplating apparatus after the first metal has been electroplated.

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5 **0016)** In another aspect a system for electroplating a metal onto the semiconductor substrate is provided, where the system includes:(a) a first electroplating apparatus configured for electrodepositing a first metal onto the semiconductor substrate from a heated electrolyte, the first electroplating apparatus comprising a substrate holder having a first lipseal; and (b) a second electroplating apparatus configured for electrodepositing a second
10 metal onto the semiconductor substrate from an unheated electrolyte, the second electroplating apparatus comprising a substrate holder having a second lipseal, wherein the second lipseal has a smaller diameter than the first lipseal.

0017) Any of the apparatuses provided herein can include a controller having program instructions configured to cause any of the steps of the methods provided herein.

15 **0018)** In another aspect, a non-transitory computer machine-readable media is provided, wherein the non-transitory computer machine-readable media includes a code configured to cause the steps of any of the methods provided herein.

0019) These and other aspects of implementations of the subject matter described in this specification are set forth in the accompanying drawings and the description below.

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BRIEF DESCRIPTION OF THE DRAWINGS

0020) Figure 1A provides a schematic cross-sectional view of a portion of a semiconductor substrate in a substrate holder during deposition of a first metal in through-mask recessed features according to an embodiment provided herein.

25 **0021)** Figure 1B provides a schematic cross-sectional view of a portion of a semiconductor substrate in a substrate holder during deposition of a second metal in an absence of lipseal edge exclusion engineering.

0022) Figure 1C provides a schematic cross-sectional view of a portion of a semiconductor substrate in a substrate holder during deposition of a second metal according
30 to an embodiment provided herein.

0023) Figure 2 is a schematic top view of annular portions of two lipseals having different diameters that can be used during electroplating according to embodiments provided herein.

0024) Figure 3 is a process flow diagram for an electrodeposition method according
35 to an embodiment provided herein.

5 **0025)** Figures 4A-4C show schematic cross-sectional views of a portion of modifiable lipseal that can be used in electrodeposition according to embodiments provided herein.

0026) Figures 5A-5B show schematic cross-sectional views of a different modifiable lipseal that can be used in electrodeposition according to embodiments provided herein.

10 **0027)** Figure 6 is a simplified schematic cross-sectional view of an electroplating cell that can be used in electroplating according to embodiments provided herein.

0028) Figure 7 is a schematic top view of a tool that can be used for electroplating according to embodiments provided herein.

15 **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

0029) In some processes used in semiconductor device processing, sequential electrodeposition of several metals into through-mask recessed features on semiconductor substrate is employed. For example, in some processing methods that are used for manufacturing high bandwidth memory (HBM) devices, nickel is electrodeposited into the through-mask features followed by electrodeposition of tin or a tin silver combination into the same recessed features. The process typically involves securing the semiconductor substrate in a substrate holder and immersing the working surface of the semiconductor substrate into an electrolyte containing nickel ions, cathodically biasing the substrate, and electrodepositing nickel into the through mask features. When the semiconductor substrate is secured in the substrate holder, a lipseal presses onto the mask material on the periphery of the semiconductor substrate. After electrodeposition of nickel is completed, the substrate is released from the substrate holder, and is sometimes stored for a period of time (e.g., 1 – 24 hours), before electrodeposition of a second metal is started. After storage, the semiconductor substrate is placed into a substrate holder again, where a lipseal presses again onto the mask material at the periphery of the substrate. The substrate is then brought into contact with a second electrolyte (e.g., with an electrolyte containing Sn^{2+} ions or a mixture of Sn^{2+} and Ag^+ ions) and is cathodically biased to deposit a second metal (e.g., tin or tin-silver combination) into the through-mask recessed features.

0030) One of the problems encountered during sequential electrodeposition of metals in through-mask (e.g., through-photoresist) features is inadvertent formation of cracks in the mask material during electrodeposition of a first metal, which may lead to defective plating at the periphery of the substrate during subsequent electrodeposition of a second metal. The

5 cracks can form due to the compression of the mask material by the lipseal in the substrate holder, and by subsequent release of this compression after the substrate is removed from the substrate holder and is placed into storage before plating of a second metal. The cracking is exacerbated when warm or hot electrolytes are used during electrodeposition of the first metal. It was discovered that an electrolyte can permeate into the cracks during
10 electrodeposition of the second metal, which may lead to unwanted electrodeposition of the second metal under the mask material with subsequent peeling or flaking of the mask material. These problems lead to non-uniformity of electrodeposition of the second metal.

0031) Methods and apparatuses for preventing or minimizing defective electroplating of the second metal are provided. The methods and apparatuses are particularly
15 useful for electroplating on semiconductor substrates, where the first electrodeposition is conducted at a high temperature (e.g., where electrolyte temperature in a first electrodeposition is greater than about 25 °C, such as greater than about 30 °C, or greater than about 40 °C) but are not limited to these applications. Provided methods can be used during fabrication of HBM memory, but are generally applicable to any process that utilizes
20 sequential electrodeposition of metals into recessed features. The methods can be used for minimizing plating defects during electrodeposition of a variety of metals, but will be primarily illustrated with reference to sequential electrodeposition of nickel (Ni) followed by tin silver (SnAg).

0032) The term “a metal” as used in the claims, refers to one or more metals, and
25 “electrodeposition of a metal” is not limited to electrodeposition of a single metal. For example, “a metal” can be a combination of tin and silver. In some embodiments, the methods are used for electrodeposition of nickel (Ni) followed by electrodeposition of tin (Sn) as a single metal. In some embodiments, the methods are used for electrodeposition of copper (Cu), followed by electrodeposition of nickel (Ni), and followed by electrodeposition
30 of tin (Sn) or tin silver (SnAg).

0033) The term “semiconductor substrate” as used herein refers to a substrate at any stage of semiconductor device fabrication containing a semiconductor material anywhere within its structure. It is understood that the semiconductor material in the semiconductor substrate does not need to be exposed. Semiconductor wafers having a plurality of layers of
35 other materials (e.g., dielectrics) covering the semiconductor material, are examples of semiconductor substrates. The following detailed description assumes the disclosed implementations are implemented on a semiconductor wafer, such as on a 200 mm, 300 mm,

5 or 450 mm semiconductor wafer. However, the disclosed implementations are not so limited. The work piece may be of various shapes, sizes, and materials. In addition to semiconductor wafers, other work pieces that may take advantage of the disclosed implementations include various articles such as printed circuit boards and the like.

0034) The term “about” when used in reference to numerical values includes a range
10 of $\pm 10\%$ of the recited numerical value, unless otherwise specified.

0035) According to provided methods, sequential electrodeposition of metals into through-mask features on a semiconductor substrate is conducted such as to reduce the deleterious consequences of lipseal’s pressure onto the mask material. In a first electroplating step, a first metal (e.g., nickel) is electrodeposited using a lipseal that has an innermost point
15 of contact with the semiconductor substrate at a first distance from the edge of the substrate. In a second electroplating step, a second metal (e.g., tin silver) is electrodeposited using a lipseal that has an innermost point of contact with the semiconductor substrate at a greater distance from the edge of the substrate than the first distance. This sequence results in reduced pressure on at least some of the portions of the mask that may be damaged during
20 deposition of the first metal, and can also shield these portions from electrolyte.

0036) The methods are illustrated by Figures 1A, 1B, and 1C which show schematic cross-sectional views of a peripheral portion of a semiconductor substrate in a substrate holder during electrodeposition of metals into through-mask features, where the substrate is held in a face-down orientation. Figure 1A illustrates electrodeposition of a first metal (e.g.,
25 nickel) into through-mask features. The substrate 101 is typically a semiconductor wafer, which has a portion 103 (which may include a combination of semiconductor, dielectric and conductive layers), and a conductive seed layer 105 in direct contact with the portion 103. The conductive seed layer 105 can include a variety of metals, such as copper (including copper alloys), cobalt, ruthenium, etc. The seed layer at the periphery of the semiconductor
30 substrate is used for making an electrical contact and for negatively biasing the substrate during electroplating. The first metal layer 107 (e.g., a nickel layer) is deposited into the recessed through-mask features which are formed by a patterned mask layer 109 (e.g., a photoresist layer) over the seed layer 105. Prior to electrodeposition of the first metal layer, the seed layer 105 was exposed to the electrolyte at the bottom portions of the through-mask
35 recessed features. During electroplating of the first metal, the semiconductor substrate 101 is placed into the substrate holder such that an electrically conductive contact 111 (electrically connected to a power supply) contacts the seed layer 105 at the periphery of the substrate,

5 and is configured to negatively bias the semiconductor substrate 101 during electroplating. The semiconductor substrate is pressed into a lipseal 113, where the innermost point of contact 115 of the lipseal 113 with the semiconductor substrate 101 is located at the periphery of the substrate, as illustrated at a distance D1 from the edge of the semiconductor substrate 101. The semiconductor substrate 101 is supported by a cup 117 of the substrate holder. The
10 lipseal 113 is typically made of an elastomeric material and has an annular portion that presses onto the mask material 109 at the periphery of the substrate. It can be seen that due to the compression of the mask material 109, a crack is formed in the mask material 109 near the point of contact with the lipseal 133.

0037) If no action is taken to mitigate the consequences of the damage to the mask
15 material, and without engineering of the edge exclusion zone (the zone from the edge of the substrate to the innermost point of contact of the substrate with the lipseal), a lipseal of the same diameter as the first lipseal is used during deposition of the second metal. For example, after electrodeposition of the first metal (as shown in Figure 1A), the substrate is removed from the wafer holder, and, after optional storage, may be transferred to a second wafer
20 holder that has an identical lipseal that presses onto the same positions of the mask material as the lipseal that was used during electroplating of the first metal. This is illustrated by Figure 2A which shows a schematic cross-sectional view of an edge portion of the wafer substrate undergoing electrodeposition of a second metal over the first metal. The second metal 119 (e.g., tin silver) is deposited over the first metal 107 (e.g., nickel) while the
25 substrate's working surface is immersed into an electrolyte containing ions of a second metal. In this case the distance D2 from the edge of the substrate to the innermost point of contact of the lipseal 133 with the substrate 101 is the same as distance D1 used during deposition of the first metal. This arrangement can lead to undesired electrodeposition of the second metal underneath the mask material, flaking of the mask material, and non-uniform
30 electrodeposition of the second metal near the edge of the substrate.

0038) In the embodiments provided herein, the edge exclusion zone is engineered such that during electrodeposition of the second metal the lipseal is configured such that there is a larger distance from the edge of the substrate to the innermost point of contact of the lipseal with the substrate than the distance from an edge of the substrate to the innermost
35 point of contact of the lipseal that was used during the first metal electrodeposition. This can be accomplished, for example, by using a lipseal having a smaller diameter (referring to inner diameter of an annular portion of a lipseal that comes in contact with the substrate) than the

5 lipseal that was used during electrodeposition of a first metal. This is illustrated by Figure 1C, which shows a schematic partial cross-sectional view of an edge of a substrate undergoing electrodeposition of a second metal. In this implementation a lipseal 114 having a smaller diameter than the lipseal 113 shown in Figure 1A is used. The distance D3 from the innermost point of contact 116 of the lipseal 114 with the wafer substrate 101 is greater than
10 the distance D1 illustrated in Figure 1A. In some embodiments the distance D4 from the edge of the wafer to the outer point of contact of the lipseal 114 with the substrate 101 is also larger than an equivalent distance from the edge of the wafer to the outer point of contact of the lipseal 113 and the substrate 101 used during electrodeposition of the first metal. By using a lipseal of a smaller diameter during electrodeposition of a second metal, the deleterious effects of cracks in the mask material and subsequent plating non-uniformity can
15 be reduced or avoided.

0039) In a specific implementation a lipseal used during electrodeposition of nickel (a first metal) has an innermost point of contact with the substrate at 2.25 mm from the edge of the substrate, and a lipseal used during electrodeposition of tin silver (a second metal) has
20 an innermost point of contact with the substrate at 2.40 mm from the edge of the substrate.

0040) In some embodiments the distance from the edge of the substrate to an innermost point of contact of a lipseal with the substrate during the electrodeposition of the second metal is greater than a distance from the edge of the substrate to an innermost point of contact of a lipseal with the substrate during the electrodeposition of the first metal by about
25 0.1 – 0.5 mm such as by about 0.15 – 0.25 mm. In other words, referring to Figures 1A and 1C, in some embodiments D3 minus D1 is about 0.1 – 0.5 mm such as about 0.15 – 0.25 mm. This can also be illustrated by Figure 2, which shows a schematic top view of innermost diameters of two lipseals. The lipseal 201 is a larger-diameter lipseal that is used during electrodeposition of a first metal. The lipseal 203 is a smaller-diameter lipseal that is used
30 during electrodeposition of a second metal. The difference of the radiuses of the two lipseals, L, is in some embodiments about 0.1 – 0.5 mm, such as about 0.15 – 0.25 mm, and corresponds to the difference of D3 and D1 described above with reference to cross-sectional views shown in Figure 1A and 1C.

0041) Figure 3 provides an exemplary process flow diagram for conducting
35 electroplating using edge exclusion zone engineering in accordance with embodiments provided herein. The process starts in step 301 by providing a semiconductor substrate having through-mask recessed features to an electroplating apparatus. The substrate (e.g., a partially

5 fabricated HBM device) is secured in a substrate holder having a lipseal that presses onto the mask material at the edge of the substrate, and is immersed into an electroplating solution configured for electroplating a metal into the through-resist recessed features. The electroplating solution contains ions of the metal that is being plated, and, optionally may contain an acid. In step 303, a first metal is electrodeposited into the recessed features
10 without fully filling the recessed features, using a lipseal configured such that an innermost point of contact between the lipseal and the semiconductor substrate is located at a first distance from an edge of the semiconductor substrate. Next, in step 305, a second metal is electrodeposited into the recessed features using a lipseal configured such that an innermost point of contact between the lipseal and the semiconductor substrate is located at a greater
15 distance from an edge of the semiconductor substrate. In some embodiments, electrodeposition of a first and second metals is performed using two different substrate holders, where the substrate holder used for electrodeposition of a first metal has a lipseal of a larger diameter than a lipseal used in electrodeposition of a second metal.

0042) While in some embodiments the edge exclusion zone can be engineered by using lipseals of different diameters, in other embodiments, the same effect can be obtained
20 by using a single lipseal that is configured to be modified using torque or compression..

0043) In some embodiments the lipseal is changed from a first configuration to a second configuration using torque. An example of such a lipseal 407 is illustrated in Figures 4A-4C, where the location of the innermost lipseal-wafer contact 401, 403, and 405 can be
25 changed by using a torque on a cup 411 holding the substrate 409 between configuration of Figure 4A, configuration of Figure 4B, and configuration of Figure 4C. For example, plating of a first metal can be conducted when the lipseal 407 is in position shown in Figure 4A, where the lipseal 407 contacts the semiconductor substrate 409 at position 401 (referring to the innermost point of contact). Next, the substrate may be transferred to contact a different
30 electrolyte, and the lipseal may be configured into a position shown in Figure 4C using torque, such that the innermost point of contact 405 between the lipseal and the substrate is further inward from the edge of the wafer than the contact point 401 shown in Figure 4A. A second metal can be electroplated in this configuration. Alternatively, the first metal can be electroplated in the configuration shown in Figure 4B, where the innermost point of contact
35 403 between the lipseal and the substrate is closer to the edge of the substrate than in both the configuration shown in Figure 4A and in Figure 4C. After the first metal has been electroplated using the configuration shown in Figure 4B, the substrate can be transferred to a

5 second electrolyte and the lipseal configuration can be changed to one shown in Figure 4A or Figure 4C that both provide larger edge exclusion zone (distance from the edge of the substrate to the innermost point of contact between the lipseal and the substrate). Then, a second metal is electroplated into the recessed features using the lipseal configuration shown in Figure 4A or Figure 4C. Different steps may have variations in lipseal supporting hardware
10 that drive different exclusion via torquing the identical lipseals in different ways.

0044) In some embodiments the lipseal is changed from a first configuration to a second configuration using compression. An example of such a lipseal is illustrated in Figures 5A-5B, where the point of lipseal-wafer contact can be changed by using cup compression force or contacts spring compression force. For example, plating of a first metal
15 can be conducted when the lipseal 501 is in position shown in Figure 5A (uncompressed state), and has an innermost point of contact with the substrate 503 at point 505. Next, the substrate can be transferred to a different electrolyte (without changing the lipseal) and the configuration of the lipseal 501 can be changed to a configuration shown in Figure 6B (compressed), such that an innermost point of contact 507 of the lipseal 501 with the
20 substrate 503 is further away from the edge of the substrate than in the configuration shown in Figure 6A.

0045) It is noted that the described methods are illustrated using sequential deposition of two metals as an example, but provided embodiments are not limited to electrodeposition of two metals, and can be used for sequential electrodeposition of a larger
25 number of metals (e.g., 3, 4, or 5 metals), where the edge exclusion zone may be engineered during all or at least some steps. For example, if three metals are sequentially deposited, a lipseal used during deposition of a first metal may have larger diameter than a lipseal used during deposition of a second metal, which in turn may have a larger diameter than a lipseal used during deposition of a third metal. In another implementation, lipseals used during
30 deposition of a first and second metal may have the same diameter, and a lipseal used during deposition of a third metal may have a smaller diameter than both of these lipseals. An example of sequential electrodeposition, where three metals are plated into through mask features includes sequential electrodeposition of copper followed by nickel followed by tin or tin silver.

35 **0046)** Provided methods are particularly useful when electrodeposition of the first metal is conducted at an elevated temperature (e.g., at least about 25 °C, such as at least about 30 °C, or at least about 40 °C). This is because warm or hot electrolyte is capable of damaging

5 the mask material (e.g., organic photoresist material) to a greater extent than cold electrolyte. Examples of metals that are often electroplated at elevated temperature include nickel and cobalt. In some embodiments the first metal is electrodeposited at an elevated temperature and the second metal is electrodeposited at room temperature.

10 **0047)** In some embodiments provided methods are used for sequential electroplating of metals into through-mask features, where the electrodeposited metals are not formed above the field region defined by the plane of the photoresist. Such plating is used in some embodiments because it minimizes the risks of metal plating on a lipseal material.

Apparatus

15 **0048)** The deposition methods described herein can be carried out in a variety of electroplating apparatuses. In some embodiments, electroplating of a first metal (e.g., nickel) is conducted in first electroplating apparatus having a first plating chamber and a first substrate holder with a first lipseal, and electroplating of a second metal is conducted in a second electroplating apparatus having a second plating chamber, and a second substrate holder with a second lipseal (e.g., a lipseal of a smaller diameter than
20 the first lipseal).

0049) A suitable apparatus for deposition of a first or second metal includes a plating chamber configured for holding an electrolyte and an anode, and a substrate holder having contacts for cathodically biasing the substrate, a cup for holding the substrate and a lipseal. Deposition can be conducted in a face-up or a face-down
25 orientation. Some plating tools may be also run vertically. An example of a suitable apparatus is a SABRE 3D tool available from Lam Research Corp. of Fremont, CA. In some embodiments the electroplating tool includes multiple plating cells (for electrodepositing identical or different metals) and a robotic tool for transferring the substrate between the individual plating cells.

30 **0050)** A schematic cross-sectional view of an apparatus that can be used for electrodeposition of a first or second metal in a face-down orientation is shown in Figure 6. The apparatus includes a plating chamber 601 configured to hold electrolyte 603, and an anode 605. The substrate holder 607 is configured to hold the semiconductor substrate 609 in a face-down orientation and to rotate the substrate 609 during electroplating. The
35 substrate holder 607 further includes electrical contacts that are configured to cathodically (negatively) bias the substrate during electroplating. In the illustrated embodiment the apparatus further includes an ionically resistive ionically permeable

5 element 611 proximate the substrate 609 (e.g., within about 10 mm of the substrate). The ionically resistive ionically permeable element 611 is typically a plate made of a non-conductive material that has a plurality of through-channels or a 3D porous network that allows for flow of electrolyte. The ionically resistive ionically permeable element 611 is often used to improve the uniformity of plating on the semiconductor substrate 609. The
10 plating chamber 601 includes an opening 613 for introduction of electrolyte. In the depicted embodiment, the electrolyte is admitted at the bottom portion of the plating chamber and then flows as depicted by arrows 615 through the channels of the ionically resistive ionically permeable element 611 towards the semiconductor substrate 609. In other embodiments the electrolyte can be injected laterally in a direction that is
15 substantially parallel to the working surface of the semiconductor substrate 609 in addition to, or instead of the flow of electrolyte that is substantially perpendicular to the working surface of the semiconductor substrate 609.

0051) In some embodiments the apparatus further includes an ionically permeable membrane between the anode and a cathodically biased substrate, which
20 separates the plating chamber into an anolyte chamber and a catholyte chamber, where electrolyte in the anolyte chamber and catholyte chamber may have different compositions. For example during electrodeposition of tin silver, the catholyte includes both tin and silver ions, while the anolyte may include only tin ions.

0052) The apparatus in some embodiments further includes a heater and a
25 temperature sensor to maintain the electrolyte at an elevated temperature, e.g., a temperature of at least about 30 °C. For example, in some embodiments the apparatus used for electrodeposition of nickel has a heater and is configured for electroplating using a nickel electrolyte at a temperature of at least about 30 °C.

0053) In some embodiments the apparatus further includes a controller having
30 program instructions for causing performance any of the method steps described herein.

0054) An integrated apparatus configured for electrodeposition of multiple metals is illustrated in Figure 7. In this embodiment, the apparatus 700 has a set of electroplating cells 707, each containing an electrolyte-containing bath, in a paired or multiple “duet” configuration. In addition to electroplating *per se*, the apparatus 700 may perform a variety
35 of other electroplating or electroplanarization related processes and sub-steps, such as spin-rinsing, spin-drying, metal and silicon wet etching, electroless deposition, pre-wetting and pre-chemical treating, reducing, annealing, photoresist stripping, and surface pre-activation,

5 for example. The apparatus 700 is shown schematically looking top down in Figure 7, and only a single level or “floor” is revealed in the figure, but it is to be readily understood by one having ordinary skill in the art that such an apparatus, e.g. the Lam Research Sabre™ 3D tool, can have two or more levels “stacked” on top of each other, each potentially having identical or different types of processing stations. In some embodiments electroplating
10 stations for different metals are arranged on different levels of the tool. In other embodiments a single level may include stations for electroplating both a first and a second metal.

0055) Referring once again to Figure 7, the substrates 706 that are to be electroplated are generally fed to the apparatus 700 through a front end loading FOUP (front loading unified pod) 701 and, in this example, are brought from the FOUP to the main substrate
15 processing area of the apparatus 700 via a front-end robot 702 that can retract and move a substrate 706 driven by a spindle 703 in multiple dimensions from one station to another of the accessible stations - two front-end accessible stations 704 and also two front-end accessible stations 708 are shown in this example. The front-end accessible stations 704 and 708 may include, for example, pre-treatment stations, and spin rinse drying (SRD) stations.
20 Lateral movement from side-to-side of the front-end robot 702 is accomplished utilizing robot track 702a. Each of the substrates 706 may be held by a cup/cone assembly (not shown) driven by a spindle connected to a motor (not shown), and the motor may be attached to a mounting bracket 709. Also shown in this example are the four “duets” of electroplating cells 707, for a total of eight cells 707. The electroplating cells 707 may be used for
25 electroplating the first and second metals. After a first metal has been electroplated in one of the plating stations 707, the substrate is transferred to a plating cell configured for electroplating of a second metal either on the same level of the apparatus or on a different level of the apparatus 700. A system controller (not shown) may be coupled to the electrodeposition apparatus 700 to control some or all of the properties of the
30 electrodeposition apparatus 700. The system controller may be programmed or otherwise configured to execute instructions according to processes described earlier herein.

0056) The system controller will typically include one or more memory devices and one or more processors configured to execute the instructions so that the apparatus will perform a method in accordance with the present invention. Machine-readable media
35 containing instructions for controlling process operations in accordance with the present invention may be coupled to the system controller.

0057) In some implementations, a controller is part of a system, which may be part

5 of the above-described examples. Such systems can include semiconductor processing equipment, including a processing tool or tools, chamber or chambers, a platform or platforms for processing, and/or specific processing components (a wafer pedestal, a gas flow system, etc.). These systems may be integrated with electronics for controlling their operation before, during, and after processing of a semiconductor wafer or substrate. The
10 electronics may be referred to as the “controller,” which may control various components or subparts of the system or systems. The controller, depending on the processing requirements and/or the type of system, may be programmed to control any of the processes disclosed herein, including the delivery of electrolytes, temperature settings (e.g., heating and/or cooling), voltage delivered to the cathode, wafer transfers into and out of a tool and other
15 transfer tools and/or load locks connected to or interfaced with a specific system.

0058) Broadly speaking, the controller may be defined as electronics having various integrated circuits, logic, memory, and/or software that receive instructions, issue instructions, control operation, enable cleaning operations, enable endpoint measurements, and the like. The integrated circuits may include chips in the form of firmware that store
20 program instructions, digital signal processors (DSPs), chips defined as application specific integrated circuits (ASICs), and/or one or more microprocessors, or microcontrollers that execute program instructions (e.g., software). Program instructions may be instructions communicated to the controller in the form of various individual settings (or program files), defining operational parameters for carrying out a particular process on or for a
25 semiconductor wafer or to a system. The operational parameters may, in some embodiments, be part of a recipe defined by process engineers to accomplish one or more processing steps during the fabrication of one or more layers, materials, metals, oxides, silicon, silicon dioxide, surfaces, circuits, and/or dies of a wafer.

0059) The controller, in some implementations, may be a part of or coupled to a
30 computer that is integrated with, coupled to the system, otherwise networked to the system, or a combination thereof. For example, the controller may be in the “cloud” or all or a part of a fab host computer system, which can allow for remote access of the wafer processing. The computer may enable remote access to the system to monitor current progress of fabrication operations, examine a history of past fabrication operations, examine trends or performance
35 metrics from a plurality of fabrication operations, to change parameters of current processing, to set processing steps to follow a current processing, or to start a new process. In some examples, a remote computer (e.g. a server) can provide process recipes to a system over a

5 network, which may include a local network or the Internet. The remote computer may include a user interface that enables entry or programming of parameters and/or settings, which are then communicated to the system from the remote computer. In some examples, the controller receives instructions in the form of data, which specify parameters for each of the processing steps to be performed during one or more operations. It should be understood
10 that the parameters may be specific to the type of process to be performed and the type of tool that the controller is configured to interface with or control. Thus as described above, the controller may be distributed, such as by comprising one or more discrete controllers that are networked together and working towards a common purpose, such as the processes and controls described herein. An example of a distributed controller for such purposes would be
15 one or more integrated circuits on a chamber in communication with one or more integrated circuits located remotely (such as at the platform level or as part of a remote computer) that combine to control a process on the chamber.

0060) Without limitation, example systems may include a plasma etch chamber or module, a deposition chamber or module, a spin-rinse chamber or module, a metal plating
20 chamber or module, a clean chamber or module, a bevel edge etch chamber or module, a physical vapor deposition (PVD) chamber or module, a chemical vapor deposition (CVD) chamber or module, an atomic layer deposition (ALD) chamber or module, an atomic layer etch (ALE) chamber or module, an ion implantation chamber or module, a track chamber or module, and any other semiconductor processing systems that may be associated or used in
25 the fabrication and/or manufacturing of semiconductor wafers.

0061) As noted above, depending on the process step or steps to be performed by the tool, the controller might communicate with one or more of other tool circuits or modules, other tool components, cluster tools, other tool interfaces, adjacent tools, neighboring tools, tools located throughout a factory, a main computer, another controller, or tools used in
30 material transport that bring containers of wafers to and from tool locations and/or load ports in a semiconductor manufacturing factory.

Patterning Method/Apparatus

0062) The apparatus/process described hereinabove may be used in conjunction with lithographic patterning tools or processes, for example, for the fabrication or manufacture of
35 semiconductor devices, displays, LEDs, photovoltaic panels and the like. Typically, though not necessarily, such tools/processes will be used or conducted together in a common fabrication facility. Lithographic patterning of a film typically comprises some or all of the

- 5 following steps, each step enabled with a number of possible tools: (1) application of photoresist on a workpiece, i.e., substrate, using a spin-on or spray-on tool; (2) curing of photoresist using a hot plate or furnace or UV curing tool; (3) exposing the photoresist to visible or UV or EUV or x-ray light with a tool such as a wafer stepper; (4) developing the resist so as to selectively remove resist and thereby pattern it using a tool such as a wet
- 10 bench; (5) transferring the resist pattern into an underlying film or workpiece by using a dry or plasma-assisted etching tool; and (6) removing the resist using a tool such as an RF or microwave plasma resist stripper.

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