ABSTRACT

A METHOD OF INTEGRATING L - SHAPED SPACERS IN A HIGH PERFORMANCE CMOS PROCESS VIA USE OF AN OXIDE - NITRIDE - DOPED OXIDE SPACER

A process for fabricating a complimentary metal oxide semiconductor (CMOS), device featuring composite insulator spacer shapes which allow P channel (PMOS), short channel effects to be minimized, and allow reductions in resistance for N channel (NMOS), source/drain extension regions to be realized, has been developed. The process features initial composite insulator spacers formed in the sides of gate structures after definition of the NMOS and PMOS source/drain extension regions. The initial composite insulator spacer, comprised of an underlying silicon oxide component, an L- shaped silicon nitride component, and an overlying doped oxide component, is then used for definition of the PMOS heavily doped source/drain region, allowing for adequate space between the heavily doped source/drain and channel regions, thus reducing the risk of short channel effects. After removal of the doped oxide component, the L - shaped composite insulator spacer is used to define, via ion implantation procedures, an NMOS heavily doped region, featuring a portion of the heavily doped source/drain region formed underlying a horizontal feature of the L - shaped silicon nitride component, therefore compensating a portion of the NMOS source/drain extension region, and resulting in the desired reduction in source/drain resistance.

FIGURE 8