METHOD OF FORMING AN INTEGRATED CIRCUIT ASSEMBLY OR PART THEREOF.

The present invention relates to a method of forming an integrated circuit assembly or part thereof and, although the invention is not so restricted, it relates more particularly to a method of forming a circuit substrate with leads having projections known as "bumps".

According to the present invention, there is provided a method of forming an integrated circuit assembly or part thereof comprising providing an insulating substrate having holes disposed adjacent opposite sides thereof; providing a conductive layer on and extending from the insulating substrate and entirely disposed between said holes; providing front and back surfaces of the conductive layer with photo-resist layers; patterning both the photo-resist layers by simultaneous exposure and development so as to form lead patterns; subjecting portions of the said front and back surfaces to partial etching; applying a protective resist layer to the said back surface; completing the etching of the conductive layer by effecting further etching of the said front surface so as to provide the conductive layer with a plurality of separate leads; and removing the photo-resist and protective resist layers.

Preferably, as a result of the said further etching, the conductive layer is provided with a plurality of separate leads.

Each said lead preferably has a projection at its

distal end.

Each projection may have an outer surface constituted by that of a gold plating.

The gold plating may be provided on a nickel plating which is itself provided on the distal end of the respective lead.

The said outer surface may be chemically etched.

The method may comprise connecting each said lead to a connector portion of an electronic element.

Preferably, at least the surface of each connector portion is formed of aluminium or an aluminium alloy.

Each lead may be connected to its respective connector portion by the application of heat and pressure so as to produce an alloy connection therebetween.

The substrate may be constituted by an insulating film of resin, the leads being formed from a conductive layer of metal foil which is mounted on the substrate. The metal foil may be made of copper.

The substrate may be provided with an opening for housing an electronic element, the said conductive layer extending over said opening.

The partial etching may be effected with ferric chloride solution.

The back surface of each lead may be etched to produce a curved surface adjacent its projection. Moreover, the back surface of each lead may be etched to provide a lead which tapers towards its projection.

The invention also comprises an integrated circuit assembly or part thereof when made by the method set forth above.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 is a broken away cross-sectional view of a part of an integrated circuit assembly known to the Applicants and not forming part of the present invention;

Figure 2 illustrates the steps in a method of forming a part of an integrated circuit assembly, the said method being known to the Applicants and not forming part of the present invention;

Figure 3 illustrates the steps in a method according to the present invention of forming a part of an integrated circuit assembly;

Figures 4-6 are plan views of photo-masks which may be used in the method illustrated in Figure 3;

Figures 7-9 are broken away sectional views illustrating alternative forms of leads forming portions of the said part of an integrated circuit assembly which may be made by the method illustrated in Figure 3;

Figure 10 is a broken away sectional view of an

integrated circuit assembly incorporating the said part which may be made by the method illustrated in Figure 3;

Figure 11 is a view similar to that of Figure 10 but illustrating a modification, and

Figure 12 is a broken away cross sectional view of another part of an integrated circuit assembly made by the method of the present invention.

Reference is made to Figure 1 which is a cross sectional view of a part of an integrated circuit assembly known to the Applicants and not forming part of the present invention.

In Figure 1 there is shown a circuit substrate base film 1 on which is mounted a film 3 which is provided with a conductive pattern (not shown), the film 3 being secured to the circuit substrate base film 1 by a layer 2 of adhesive. The circuit substrate base film 1 has an aperture 1a therein, the film 3 having a plurality of finger leads 4 each of which extends over part of the aperture 1a. An electronic element such as an integrated circuit chip (not shown) may be mounted in the aperture 1a.

Each finger lead 4 is provided with a concave neck-like portion 5 so that a projection, or "bump", 6 is formed at the distal end of the lead. Generally, the surface 8 of the "bump" 6 which is to be connected to an aluminium pad of the integrated circuit chip is substantially planar such that the roughness, as defined

below, is less than 3 microns.

The term "roughness" as used herein is to be understood to mean the distance, in a direction at right angles to the contact surface, between the deepest trough and the highest crest in the said contact surface.

The roughness may be between 5 and 20 microns and is preferably between 5 and 15 microns.

The construction shown in Figure 1, however, has some disadvantages. For example, when the integrated circuit (hereinafter "IC") chip is attached at its aluminium pads to the "bumps" 6., the connection between the IC chip and the circuit substrate base film 1 is often unstable, weak or even cannot be made at all, especially when the oxide film on the surface of the aluminium pad is relatively thick.

In Japanese Patent Application No. 59-17981 there is disclosed a method of forming a projection for making an electrical connection between, for example, an inner lead of a substrate and an electronic element. This method, as illustrated in the accompanying Figure 2, involves the steps of:-

a) coating a front surface 22a of a conductive layer 22 with a protective resist 27, the conductive layer 22 being provided on a circuit substrate 21 having an aperture 24 for housing an IC chip (not shown) and sprocket holes 25,

b) coating a back surface 22b of the conductive

layer 22 with a photo-resist 23 and forming "bumps" or projections 26 by exposure, development and half etching,

c) removing the protective resist 27 and the photo-resist 23 on the front, and the back surfaces 22a, 22b of the conductive layer 22,

d) coating the front surface 22a of the conductive layer 22 with a photo-resist 31 and patterning the latter by exposure and development,

e) coating the back surface 22b of the conductive layer 22 with a protective resist 32,

f) etching the front surface 22a of the conductive layer 22 to form a circuit pattern having inner leads 28, and

g) removing the photo-resist 31 and the protective resist 32 on the front and the back surfaces 22a, 22b of the conductive layer 22, to form the "bumps" 26 on the back surface 22b of the inner leads 28.

The method illustrated in Figure 2, however, has some defects. Since the front and the back surfaces 22a, 22b of the conductive layer 22 are exposed separately, the positioning of the conductive layer 22 for exposure is likely to be inaccurate, and therefore it is difficult to form the "bumps" 26 accurately at the predetermined positions on the inner leads 28. The patterns on the front and the back surfaces 22a, 22b of the conductive layer 22 can thus be positioned in registration with each other only initially but it is impossible to maintain registration of the patterns on

both surfaces of the subsequent individual substrates. Accordingly, if the accuracy of the positioning of the conductive layer 22 with respect to the exposure apparatus is poor, or if the sprocket holes 25 which are pilot holes, have become deformed, many defects occur such as the fact that the "bumps" fail to be formed and that errors occur in the positioning of the "bumps" and of the electrodes of the semiconductor element and consequently the connection therebetween is unsatisfactory.

Moreover, in the method of Figure 2, the half-etched conductive layer 22 is reduced in strength and since such a weakened layer is coated with the photo-resist, exposed, developed and subjected to other processes, it is likely to become deformed. Consequently cracks of the photo-resist cause the disconnection of the wiring, thereby making it impossible to form the desired patterns with certainty.

Reference is now made to Figure 3 which illustrates successive steps in the production of an embodiment of the present invention in which "bumps" for electrical connection are formed on the inner leads of a substrate.

Figure 3(a) illustrates the step of coating photo-resist 43 onto opposite surfaces 42a, 42b of a conductive layer 42 attached to an insulating layer 41. The insulating layer 41 may be a flexible tape of a material such as polyimide or glass-reinforced epoxy resin having for instance a thickness of between 25 and 125 microns. The insulating layer 41 is provided with an aperture 44 for holding an electronic element such as a

semiconductor chip. The insulating layer 41 is also provided with sprocket holes 45 for positioning or transporting the insulating layer 41 and with other holes (not shown) for the passage therethrough of wires (not shown) which are necessary for the circuits employed. As will be seen, the holes 45 are disposed adjacent opposite sides of the insulating layer 41, and the conductive layer 42 is disposed entirely between the holes 45.

The conductive layer 42 is generally a copper foil having a thickness of between 35 and 70 microns. The back surface 42b is treated to have a roughness as herein defined of about 10 microns in order to improve its adhesiveness with respect to the insulating layer 41. This roughness is retained on the surface of the bumps 46 which are formed in a later step. This roughness is of importance, when connecting an aluminium pad of the semiconductor chip to a bump 46. Accordingly, it is important to maintain the initial surface roughness. Consequently, the thickness of the photo-resist 43 on the back surface 42b of the conductive layer 42 must be sufficient for the convex projecting portions of the surface not to be etched during the subsequent half-etching process and must not be too thick to become non-uniform. Thus the most suitable thickness of the photo-resist 43 on the back surface 42b of the conductive layer 42 is between 1.5 and 4 microns. The thickness of other photo-resist layer 43 on the front surface 42a of the conductive layer 42 is generally between 1 and 3 microns.

The photo-resists 43 on the surfaces 42a, 42b may be coated by a roller coater, spraying and so on.

In the step shown in Figure 3(b), both surfaces 42a, 42b of the conductive layer 42 are simultaneously

exposed to form a circuit pattern including inner leads on the front surface 42a. This may be done by using the photo-mask shown in Figure 4 and to form the "bump" pattern on the back surface 42b by using the photo-mask shown in Figure 5. This simultaneous exposure is performed by using a two-sided exposure apparatus which has been adjusted to form the patterns at the predetermined positions on both surfaces 42a, 42b. Then the two surfaces 42a, 42b are simultaneously developed by spraying or dipping in a specific development solution.

The photo-mask of Figure 4 is designed to be thoroughly conductive so that the circuit pattern including the inner leads are electrically plated in a later step.

With regard to the photo-mask for forming the "bump" pattern, in addition to the one shown in Figure 5 in which separate projection patterns are provided correspondingly to the inner leads, another mask as shown in Figure 6 can also be used in which a part of or all of the "bumps" are connected.

In order to make the condition of both surfaces 42a, 42b of the conductive layer 42 an optimum for development simultaneously, the degree of exposure is adjusted so that, when the thickness of the photo-resists 43 on both surfaces 42a, 42b are equal, the amount of light for the back surface 42b which has a high degree of roughness and which is difficult to develop is 1.5 to 2.5 times as large as that for the front surface 42a.

In the step shown in Figure 3(c), both surfaces

42a, 42b of the conductive layer 42 are partially etched by spraying an etching solution such as ferric chloride. The height of the "bumps" 46 on the back surface 42b of the conductive layer 42 depends on the thickness of the used conductive layer. Generally, when the conductive layer 42 is a copper foil having a thickness of 35 microns, the height is desirably between 5 and 20 microns in order to prevent an edge short circuit of the semiconductor chip and to assure the strength of the inner leads.

Furthermore, in order to prevent the disconnection of the conductive layer 42 at the corners of the partially etched portion on which the stress is concentrated, the spray pressure may be reduced and a side etch effected, mainly to form a large round curve at the corners of the partially etched portion as shown in Figure 7.

Usually, the partial-etching is carried out by spraying a solution of ferric chloride at a solution temperature of between 25 and 40°C, the solution having a specific gravity of between 30 to 60 Be (Baume) at a spraying pressure of 0.5kgf/cm^2 or less. However, if the height of the "bumps" 46 is smaller than half of the thickness of the conductive layer 42, partial etching by a dipping method is also applicable.

In order to obtain adequate strength of the inner leads, it may sometimes be desirable for the photo-mask used when the "bump" pattern is formed on the back surface 42b of the conductive layer 42 by exposure and development to be modified so as progressively to vary the amount of partial etching, as shown in Figure 8 or

to make the partially etched portion as short as possible as shown in Figure 9.

With respect to the partial etching of the front surface 42a of the conductive layer 42, in order to avoid non-uniform etching caused by undesirable flow of the etching solution used for the partial etching of the back surface 42b, the etching solution may be sprayed in the same manner as for the back surface. At this time, it is necessary to adjust the spray pressure and so on so that the portion of the conductive layer 42 which is etched from both surfaces 42a, 42b is not etched sufficiently to form a hole.

In Figure 3(d), the back surface 42b of the conductive layer 42 is coated by means of a roller coater or spraying, with a protective resist 47 such as an etching resist or a photo-resist which can be removed by the same removing solution used for removing the photo-resist formed in the step of Figure 3(a).

In Figure 3(e), the etching solution is sprayed on the front surface 42a of the conductive layer 42 to etch away the unnecessary conductive layer which has remained without being etched in the step of Figure 3(c). Thus a circuit pattern having inner leads 48 is formed.

In Figure 3(f), the photo-resist 43 and the protective resist 47 are removed with a specific removing solution. Finally, there is formed a circuit substrate 41 having inner leads 48 with the "bumps" 46 for electrical connection.

Generally, although not shown in Figure 3 or in

Figures 7-9, the projections or "bumps" 46 are plated with nickel having a thickness of between 0 to 3 microns and then with gold having a thickness of 0.5 to 4 microns, and the "bumps" 46 are positioned in registration with the aluminium pads of the semiconductor chip and are thermally bonded thereto to make electrical connections therebetween.

Figure 10 shows a structure in which a semiconductor chip 51 is connected to "bumps" 53 on the front surfaces of leads 54, the leads 54 being mounted on a substrate 50 and being formed by the method illustrated in Figure 3. 52 is a resin sealing agent.

Figure 11 illustrates a construction generally similar to that of Figure 10, like reference numerals indicating like parts. In the Figure 11 construction, however, the leads 54 have "bumps"" 53a on the rear surfaces, as opposed to the front surfaces, of the leads 54.

The invention is of course applicable to all kinds of print substrates having leads for connection to an electrical element.

By using the method illustrated in Figure 3, the inner leads and the "bump" pattern are formed simultaneously on the front and the back surfaces 42a, 42b of the conductive layer 42 by the common exposure apparatus. Accordingly, if the patterns on both surfaces are initially registered with each other, no relative positioning error between the patterns on the two surfaces occurs thereafter and consequently the formation of the patterns is not affected by the

accuracy of the positioning of the substrate with respect to the exposure apparatus and the accuracy of the positioning holes in the substrate itself. Thus, the "bumps" are always formed accurately at the predetermined position on the inner leads. Moreover, it is easy to position the "bumps" in registration with the electrodes of the electronic element and stable connections therebetween are obtained.

Furthermore, the number of steps in the method illustrated in Figure 3 are greatly reduced in comparison with those employed in the prior art. In particular, after the partial etching of the conductive layer 42, there is only the single step of coating the back surface 42b of the conductive layer 42 with the protective resist 47 before the final etching, and therefore the conductive layer 42 is not likely to be deformed. For this reason, no cracking occurs in the photo-resist and good stable patterns are easily formed.

It is another advantage that the simplification referred to above leads to a large reduction in manufacturing costs.

Figure 12 is an enlarged cross sectional view of the "bump" portion 65 of a finger lead 64 which corresponds to a lead 48 of Figure 3(f). The finger lead 64 and the "bump" 65 are formed from a copper foil 66. The surface of the copper foil 66 is plated with a nickel layer 68 and with a gold layer 69. These plating layers 68, 69 are relatively thick at the projecting portions or crests 67 of the contact surface of the "bump" 65 at which the electrical current is concentrated and are relatively thin around the troughs

70, thus increasing the roughness of the contact surface. Such a phenomenon is more pronounced when the electrical current density employed during the plating is high. Accordingly, it is desirable to make the electrical current density as high as possible but is not so high as to produce plating stains.

In the embodiment illustrated in Figure 12, the nickel layer 68 can have a thickness of between 0.5 and 1 micron, and gold can be plated thereon at an electrical current density of 2.5A/dm for 1 minute. The mean total thickness of the nickel and gold platings collectively may be 1.5 microns and the increase in the roughness Rmax of various portions of the contact surface of the "bump" is between 2 and 6 microns.

The plating conditions are not limited to those mentioned above and the conditions depend on the plating apparatus or the plating solution used. When a plating layer of the same thickness as that mentioned above is to be obtained, if the plating is effected with an electric current whose current density is almost at the upper limit of the practically tolerated current density for a short time, a large degree of surface roughness can be provided.

The above embodiment concerns the case where the "bump" is formed on the back surface of the electrolytic copper foil 66 which has a large surface roughness. In the case where a "bump" is to be formed on the front surface of a copper foil whose roughness is less than 3 microns or where a rolled copper foil is used, the surface can be made rough by a mechanical method such as using brush-polishing or sand blasting or by a chemical

method such as using an aqueous solution of ammonium persulfate or sodium persulfate and by increasing the roughness of plating thereafter. By performing such a treatment, a stable connection between the "bump" and the aluminium pad can be provided which is as good as what can be provided when the bump is formed on the back surface of the electrolytic copper foil.

Thus it is within the scope of the present invention that in contrast to what is shown in Figure 1, the "bump" 6 of each finger lead 4 is provided on the side of the latter opposite to the substrate 1, the pad of the IC chip being mounted on the "bump" 6 and bonded thereto. An arrangement of this kind is illustrated in Figure 11.

Although the above description refers to the said pads as being made of aluminium, they may also be made of an aluminium alloy or of some other metal.

In our co-pending British Patent Application No. 8704425 (Serial No. 2,187,331), from which the present application has been divided, we have claimed a method of forming at least a part of an integrated circuit assembly comprising forming said part with at least one lead whose distal end is provided with a contact surface at least a portion of which has a roughness as therein defined of at least 5 microns, the or each contact surface being adapted to be connected to a connector portion of an electronic element.



CLAIMS

1. A method of forming an integrated circuit assembly or part thereof comprising providing an insulating substrate having holes disposed adjacent opposite sides thereof; providing a conductive layer on and extending from the insulating substrate and entirely disposed between said holes; providing front and back surfaces of the conductive layer with photo-resist layers; patterning both the photo-resist layers by simultaneous exposure and development so as to form lead patterns; subjecting portions of the said front and back surfaces to partial etching; applying a protective resist layer to the said back surface; completing the etching of the conductive layer by effecting further etching of the said front surface so as to provide the conductive layer with a plurality of separate leads; and removing the photo-resist and protective resist layers.

2. A method as claimed in claim 1 in which, as a result of said further etching, the conductive layer is provided with a plurality of separate leads.

3. A method as claimed in claim 2 in which each said lead has a projection at its distal end.

4. A method as claimed in claim 3 in which each projection has an outer surface constituted by that of a gold plating.

5. A method as claimed in claim 4 in which the gold plating is provided on a nickel plating which is itself provided on the distal end of the respective lead.

6. A method as claimed in claim 4 or 5 in which the said outer surface is chemically etched.

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7. A method as claimed in any of claims 2-6 in which the method comprises connecting each said lead to a connector portion of an electronic element.

8. A method as claimed in claim 7 in which at least the surface of each connector portion is formed of aluminium or an aluminium alloy.

9. A method as claimed in claim 7 or 8 in which each lead is connected to its respective connector portion by the application of heat and pressure so as to produce an alloy connection therebetween.

10. A method as claimed in any of claims 2-9 in which the substrate is constituted by an insulating film of resin, the leads being formed from a conductive layer of metal foil which is mounted on the substrate.

11. A method as claimed in claim 10 in which the metal foil is made of copper.

12. A method as claimed in claim 10 or 11 in which the substrate is provided with an opening for housing an electronic element, the said conductive layer extending over said opening.

13. A method as claimed in any preceding claim in which the partial etching is effected with ferric chloride solution.

14. A method as claimed in claim 3 or any claim dependent thereon in which the back surface of each lead is etched to produce a curved surface adjacent its

projection.

15. A method as claimed in claim 3 or any claim dependent thereon in which the back surface of each lead is etched to provide a lead which tapers towards its projection.

16. A method of forming an integrated circuit assembly or part thereof as claimed in claim 1 and substantially as hereinbefore described with reference to Figures 3-12 of the accompanying drawings.

17. An integrated circuit assembly or part thereof when made by the method claimed in any preceding claim.