DESCRIPTION

METHOD FOR PRODUCING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE

Technical Field

[0001]

The present invention relates to a method for producing a semiconductor device and a semiconductor device.

Background Art

[0002]

The degree of integration of semiconductor integrated circuits, in particular, integrated circuits using MOS transistors has been increasing. With the increasing degree of integration, the size of MOS transistors used in integrated circuits has been decreased to nano-scale dimensions. Such a decrease in the size of MOS transistors causes difficulty in suppressing leak currents, which poses a problem in that it is hard to reduce the area occupied by the circuits because of the requirements of the secure retention of necessary currents. To address the problem, a surrounding gate transistor (hereinafter referred to as "SGT") having a structure in which a source, a gate, and a drain are arranged vertically with respect to a substrate and a gate electrode surrounds a pillar-shaped semiconductor layer has been proposed (e.g., refer to PTL 1, PTL 2, and PTL 3).

[0003]

In an existing method for producing an SGT, a silicon pillar on which a nitride film hard mask is formed in a pillar shape is formed, a diffusion layer is formed in a lower portion of the silicon pillar, a gate material is then deposited, the gate material is then planarized and etched back, and an insulating film sidewall is formed on the side wall of the silicon pillar and the nitride film hard mask. Subsequently, a resist pattern for forming a gate line is formed, the gate material is etched, the nitride film hard mask is then removed, and a diffusion layer is formed in an upper portion of the silicon pillar (e.g., refer to PTL 4).

[0004]

In such a method, when the distance between the silicon pillars is decreased, a thick gate material needs to be deposited between the silicon pillars and thus holes called voids may be formed between the silicon pillars. If voids are formed, holes are made in the gate material after the etching back. When an insulating film is then deposited to form an insulating film sidewall, the insulating film is deposited in the voids. This causes difficulty in gate material processing.

[0005]

In view of the foregoing, it has been disclosed that a silicon pillar is formed, a gate oxide film is then formed,

a thin polysilicon is deposited, a resist that covers an upper portion of the silicon pillar and is used to form a gate line is then formed, a gate line is etched, a thick oxide film is then deposited, the upper portion of the silicon pillar is caused to be exposed, the thin polysilicon on the upper portion of the silicon pillar is removed, and the thick oxide film is removed by wet etching (e.g., refer to NPL 1).

[0006]

However, a method in which a metal is used for gate electrodes is not described. In addition, a resist that covers an upper portion of the silicon pillar and is used to form a gate line needs to be formed. Therefore, the upper portion of the silicon pillar needs to be covered and thus such a method is not performed in a self-aligned process.

Citation List

Patent Literature

[0007]

PTL 1: Japanese Unexamined Patent Application Publication No. 2-71556

PTL 2: Japanese Unexamined Patent Application Publication No. 2-188966

PTL 3: Japanese Unexamined Patent Application Publication No. 3-145761

PTL 4: Japanese Unexamined Patent Application Publication No.

2009-182317

Non Patent Literature

[0008]

NPL 1: B. Yang, K.D. Buddharaju, S.H.G. Teo, N. Singh, G.D. Lo, and D.L. Kwong, "Vertical Silicon-Nanowire Formation and Gate-All-Around MOSFET", IEEE Electron Device Letters, VOL. 29, No. 7, July 2008, pp 791-794.

Summary of Invention

Technical Problem

[0009]

It is an object of the present invention to provide a method for producing an SGT in which a thin gate material is used, a metal gate is employed, and a self-aligned process is performed and an SGT structure obtained by the method.

Solution to Problem

[0010]

A method for producing a semiconductor device according to a first aspect of the present invention includes:

a first step including forming a planar silicon layer on a silicon substrate, and

forming a first pillar-shaped silicon layer and a second pillar-shaped silicon layer on the planar silicon layer;

a second step including, after the first step, forming a gate insulating film around each of the first pillar-

shaped silicon layer and second pillar-shaped silicon layer,

forming a metal film and a polysilicon film around the gate insulating film,

the thickness of the polysilicon film being smaller than half of a distance between the first pillar-shaped silicon layer and the second pillar-shaped silicon layer,

forming a third resist for forming a gate line, and

forming the gate line by performing anisotropic etching; and

a third step including, after the second step, depositing a fourth resist so that a portion of the polysilicon film on an upper side wall of each of the first pillar-shaped silicon layer and second pillar-shaped silicon layer is exposed, removing the exposed portion of the polysilicon film by etching, removing the fourth resist, and removing the metal film by etching to form a first gate electrode and a second gate electrode connected to the gate line.

[0011]

In the method, upper portions of the first pillar-shaped silicon layer and second pillar-shaped silicon layer are etched by the anisotropic etching.

[0012]

In the method, an upper surface of the third resist for forming the gate line is located at a lower position than an

upper surface of the polysilicon film on each of the first pillar-shaped silicon layer and second pillar-shaped silicon layer.

[0013]

The method further includes a fourth step including forming a first n-type diffusion layer in an upper portion of the first pillar-shaped silicon layer,

forming a second n-type diffusion layer in a lower portion of the first pillar-shaped silicon layer and in an upper portion of the planar silicon layer,

forming a first p-type diffusion layer in an upper portion of the second pillar-shaped silicon layer, and

forming a second p-type diffusion layer in a lower portion of the second pillar-shaped silicon layer and in an upper portion of the planar silicon layer.

[0014]

The method further includes a fifth step including forming silicides on the first n-type diffusion layer, the second n-type diffusion layer, the first p-type diffusion layer, the second p-type diffusion layer, and the gate line.

[0015]

A semiconductor device according to a second aspect of the present invention includes:

a planar silicon layer formed on a silicon substrate;

first and second pillar-shaped silicon layers formed on

the planar silicon layer;

a gate insulating film formed around the first pillar-shaped silicon layer;

a first gate electrode having a laminated structure of a metal film and a polysilicon film, both of which are formed around the gate insulating film;

a gate insulating film formed around the second pillar-shaped silicon layer;

a second gate electrode having a laminated structure of a metal film and a polysilicon film, both of which are formed around the gate insulating film;

the thickness of each of the polysilicon films being smaller than half of a distance between the first pillar-shaped silicon layer and the second pillar-shaped silicon layer;

a gate line connected to the first and second gate electrodes;

an upper surface of the gate line being located at a lower position than upper surfaces of the first and second gate electrodes;

a first n-type diffusion layer formed in an upper portion of the first pillar-shaped silicon layer;

a second n-type diffusion layer formed in a lower portion of the first pillar-shaped silicon layer and in an upper portion of the planar silicon layer;

a first p-type diffusion layer formed in an upper portion of the second pillar-shaped silicon layer; and

a second p-type diffusion layer formed in a lower portion of the second pillar-shaped silicon layer and in an upper portion of the planar silicon layer.

[0016]

In the semiconductor device, the gate line has a laminated structure of the metal film and a silicide.

[0017]

In the semiconductor device, the thickness of the insulating film sidewall formed on a side wall of the first n-type diffusion layer is larger than the sum of the thicknesses of the metal film and polysilicon film.

[0018]

In the semiconductor device, the center line of the gate line is displaced from a line that connects a center point of the first pillar-shaped silicon layer to a center point of the second pillar-shaped silicon layer by a first predetermined distance.

[0019]

The semiconductor device further includes silicides formed on the first and second n-type diffusion layers and the first and second p-type diffusion layers.

Advantageous Effects of Invention

[0020]

According to the present invention, there can be provided a method for producing an SGT in which a thin gate material is used, a metal gate is employed, and a self-aligned process is performed and an SGT structure obtained by the method.

The height of each of the first pillar-shaped silicon layer 104 and second pillar-shaped silicon layer 105 is set to be the sum of a desired height of the pillar-shaped silicon layer and the height of a portion removed by gate-line etching performed later, whereby a self-aligned process is achieved.

[0021]

The method for producing an SGT includes:

a second step including forming a gate insulating film around each of the first pillar-shaped silicon layer and second pillar-shaped silicon layer,

forming a metal film and a polysilicon film around the gate insulating film,

the thickness of the polysilicon film being smaller than half of a distance between the first pillar-shaped silicon layer and the second pillar-shaped silicon layer,

forming a third resist for forming a gate line, and

forming the gate line by performing anisotropic etching; and

a third step including, after the second step,

depositing a fourth resist so that a portion of the polysilicon film on an upper side wall of each of the first pillar-shaped silicon layer and second pillar-shaped silicon layer is exposed, removing the exposed portion of the polysilicon film by etching, removing the fourth resist, and removing the metal film by etching to form a first gate electrode and a second gate electrode connected to the gate line.

Therefore, a self-aligned process is achieved.

Such a self-aligned process allows high degree of integration.

[0022]

The gate line has a laminated structure of the metal film and a silicide. A direct contact between the silicide and the metal film can decrease the resistance.

[0023]

The thickness of the insulating film sidewall formed on a side wall of the first n-type diffusion layer is larger than the sum of the thicknesses of the metal film and polysilicon film.

Even when a seventh resist is formed in a misaligned manner and contact holes are formed by overetching, a short circuit between a contact and the gate electrode can be prevented.

[0024]

The center line of the gate line is displaced from a line that connects a center point of the first pillar-shaped silicon layer to a center point of the second pillar-shaped silicon layer by a first predetermined distance.

A silicide that connects the second n-type diffusion layer to the second p-type diffusion layer is easily formed, which can achieve high degree of integration.

Brief Description of Drawings

[0025]

[Fig. 1] Fig. 1(A) is a plan view of a semiconductor device according to an embodiment of the present invention. Fig. 1(B) is a sectional view taken along line X-X' of Fig. 1(A). Fig. 1(C) is a sectional view taken along line Y-Y' of Fig. 1(A).

[Fig. 2] Fig. 2(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 2(B) is a sectional view taken along line X-X' of Fig. 2(A). Fig. 2(C) is a sectional view taken along line Y-Y' of Fig. 2(A).

[Fig. 3] Fig. 3(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 3(B) is a sectional view taken along line X-X' of Fig. 3(A). Fig. 3(C) is a sectional view taken along line Y-Y' of Fig. 3(A).

[Fig. 4] Fig. 4(A) is a plan view showing a method for

producing a semiconductor device according to this embodiment. Fig. 4(B) is a sectional view taken along line X-X' of Fig. 4(A). Fig. 4(C) is a sectional view taken along line Y-Y' of Fig. 4(A).

[Fig. 5] Fig. 5(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 5(B) is a sectional view taken along line X-X' of Fig. 5(A). Fig. 5(C) is a sectional view taken along line Y-Y' of Fig. 5(A).

[Fig. 6] Fig. 6(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 6(B) is a sectional view taken along line X-X' of Fig. 6(A). Fig. 6(C) is a sectional view taken along line Y-Y' of Fig. 6(A).

[Fig. 7] Fig. 7(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 7(B) is a sectional view taken along line X-X' of Fig. 7(A). Fig. 7(C) is a sectional view taken along line Y-Y' of Fig. 7(A).

[Fig. 8] Fig. 8(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 8(B) is a sectional view taken along line X-X' of Fig. 8(A). Fig. 8(C) is a sectional view taken along line Y-Y' of Fig. 8(A).

[Fig. 9] Fig. 9(A) is a plan view showing a method for

producing a semiconductor device according to this embodiment. Fig. 9(B) is a sectional view taken along line X-X' of Fig. 9(A). Fig. 9(C) is a sectional view taken along line Y-Y' of Fig. 9(A).

[Fig. 10] Fig. 10(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 10(B) is a sectional view taken along line X-X' of Fig. 10(A). Fig. 10(C) is a sectional view taken along line Y-Y' of Fig. 10(A).

[Fig. 11] Fig. 11(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 11(B) is a sectional view taken along line X-X' of Fig. 11(A). Fig. 11(C) is a sectional view taken along line Y-Y' of Fig. 11(A).

[Fig. 12] Fig. 12(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 12(B) is a sectional view taken along line X-X' of Fig. 12(A). Fig. 12(C) is a sectional view taken along line Y-Y' of Fig. 12(A).

[Fig. 13] Fig. 13(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 13(B) is a sectional view taken along line X-X' of Fig. 13(A). Fig. 13(C) is a sectional view taken along line Y-Y' of Fig. 13(A).

[Fig. 14] Fig. 14(A) is a plan view showing a method

for producing a semiconductor device according to this embodiment. Fig. 14(B) is a sectional view taken along line X-X' of Fig. 14(A). Fig. 14(C) is a sectional view taken along line Y-Y' of Fig. 14(A).

[Fig. 15] Fig. 15(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 15(B) is a sectional view taken along line X-X' of Fig. 15(A). Fig. 15(C) is a sectional view taken along line Y-Y' of Fig. 15(A).

[Fig. 16] Fig. 16(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 16(B) is a sectional view taken along line X-X' of Fig. 16(A). Fig. 16(C) is a sectional view taken along line Y-Y' of Fig. 16(A).

[Fig. 17] Fig. 17(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 17(B) is a sectional view taken along line X-X' of Fig. 17(A). Fig. 17(C) is a sectional view taken along line Y-Y' of Fig. 17(A).

[Fig. 18] Fig. 18(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 18(B) is a sectional view taken along line X-X' of Fig. 18(A). Fig. 18(C) is a sectional view taken along line Y-Y' of Fig. 18(A).

[Fig. 19] Fig. 19(A) is a plan view showing a method

for producing a semiconductor device according to this embodiment. Fig. 19(B) is a sectional view taken along line X-X' of Fig. 19(A). Fig. 19(C) is a sectional view taken along line Y-Y' of Fig. 19(A).

[Fig. 20] Fig. 20(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 20(B) is a sectional view taken along line X-X' of Fig. 20(A). Fig. 20(C) is a sectional view taken along line Y-Y' of Fig. 20(A).

[Fig. 21] Fig. 21(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 21(B) is a sectional view taken along line X-X' of Fig. 21(A). Fig. 21(C) is a sectional view taken along line Y-Y' of Fig. 21(A).

[Fig. 22] Fig. 22(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 22(B) is a sectional view taken along line X-X' of Fig. 22(A). Fig. 22(C) is a sectional view taken along line Y-Y' of Fig. 22(A).

[Fig. 23] Fig. 23(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 23(B) is a sectional view taken along line X-X' of Fig. 23(A). Fig. 23(C) is a sectional view taken along line Y-Y' of Fig. 23(A).

[Fig. 24] Fig. 24(A) is a plan view showing a method

for producing a semiconductor device according to this embodiment. Fig. 24(B) is a sectional view taken along line X-X' of Fig. 24(A). Fig. 24(C) is a sectional view taken along line Y-Y' of Fig. 24(A).

[Fig. 25] Fig. 25(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 25(B) is a sectional view taken along line X-X' of Fig. 25(A). Fig. 25(C) is a sectional view taken along line Y-Y' of Fig. 25(A).

[Fig. 26] Fig. 26(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 26(B) is a sectional view taken along line X-X' of Fig. 26(A). Fig. 26(C) is a sectional view taken along line Y-Y' of Fig. 26(A).

[Fig. 27] Fig. 27(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 27(B) is a sectional view taken along line X-X' of Fig. 27(A). Fig. 27(C) is a sectional view taken along line Y-Y' of Fig. 27(A).

[Fig. 28] Fig. 28(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 28(B) is a sectional view taken along line X-X' of Fig. 28(A). Fig. 28(C) is a sectional view taken along line Y-Y' of Fig. 28(A).

[Fig. 29] Fig. 29(A) is a plan view showing a method

for producing a semiconductor device according to this embodiment. Fig. 29(B) is a sectional view taken along line X-X' of Fig. 29(A). Fig. 29(C) is a sectional view taken along line Y-Y' of Fig. 29(A).

[Fig. 30] Fig. 30(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 30(B) is a sectional view taken along line X-X' of Fig. 30(A). Fig. 30(C) is a sectional view taken along line Y-Y' of Fig. 30(A).

[Fig. 31] Fig. 31(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 31(B) is a sectional view taken along line X-X' of Fig. 31(A). Fig. 31(C) is a sectional view taken along line Y-Y' of Fig. 31(A).

[Fig. 32] Fig. 32(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 32(B) is a sectional view taken along line X-X' of Fig. 32(A). Fig. 32(C) is a sectional view taken along line Y-Y' of Fig. 32(A).

[Fig. 33] Fig. 33(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 33(B) is a sectional view taken along line X-X' of Fig. 33(A). Fig. 33(C) is a sectional view taken along line Y-Y' of Fig. 33(A).

[Fig. 34] Fig. 34(A) is a plan view showing a method

for producing a semiconductor device according to this embodiment. Fig. 34(B) is a sectional view taken along line X-X' of Fig. 34(A). Fig. 34(C) is a sectional view taken along line Y-Y' of Fig. 34(A).

[Fig. 35] Fig. 35(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 35(B) is a sectional view taken along line X-X' of Fig. 35(A). Fig. 35(C) is a sectional view taken along line Y-Y' of Fig. 35(A).

[Fig. 36] Fig. 36(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 36(B) is a sectional view taken along line X-X' of Fig. 36(A). Fig. 36(C) is a sectional view taken along line Y-Y' of Fig. 36(A).

[Fig. 37] Fig. 37(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 37(B) is a sectional view taken along line X-X' of Fig. 37(A). Fig. 37(C) is a sectional view taken along line Y-Y' of Fig. 37(A).

[Fig. 38] Fig. 38(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 38(B) is a sectional view taken along line X-X' of Fig. 38(A). Fig. 38(C) is a sectional view taken along line Y-Y' of Fig. 38(A).

[Fig. 39] Fig. 39(A) is a plan view showing a method

for producing a semiconductor device according to this embodiment. Fig. 39(B) is a sectional view taken along line X-X' of Fig. 39(A). Fig. 39(C) is a sectional view taken along line Y-Y' of Fig. 39(A).

[Fig. 40] Fig. 40(A) is a plan view showing a method for producing a semiconductor device according to this embodiment. Fig. 40(B) is a sectional view taken along line X-X' of Fig. 40(A). Fig. 40(C) is a sectional view taken along line Y-Y' of Fig. 40(A).

Description of Embodiments

[0026]

A production process of a semiconductor device having an SGT structure according to an embodiment of the present invention will now be described with reference to Figs. 2 to 40.

[0027]

A first step will now be described. The first step includes forming a planar silicon layer 107 on a silicon substrate 101 and forming a first pillar-shaped silicon layer 104 and a second pillar-shaped silicon layer 105 on the planar silicon layer 107.

[0028]

First, as shown in Fig. 2, first resists 102 and 103 for respectively forming a first pillar-shaped silicon layer 104 and a second pillar-shaped silicon layer 105 are formed

on a silicon substrate 101.

[0029]

Next, as shown in Fig. 3, the silicon substrate 101 is etched to form a first pillar-shaped silicon layer 104 and a second pillar-shaped silicon layer 105. The height of each of the first pillar-shaped silicon layer 104 and second pillar-shaped silicon layer 105 is desirably the sum of a desired height of the pillar-shaped silicon layer and the height of a portion removed by gate-line etching performed later.

[0030]

Next, as shown in Fig. 4, the first resists 102 and 103 are removed.

[0031]

Next, as shown in Fig. 5, a second resist 106 for forming a planar silicon layer 107 is formed.

[0032]

Next, as shown in Fig. 6, the silicon substrate 101 is etched to form a planar silicon layer 107.

[0033]

Next, as shown in Fig. 7, the second resist 106 is removed.

[0034]

Next, as shown in Fig. 8, an element separation film 108 is formed around the planar silicon layer 107.

The first step has been described, the first step including forming a planar silicon layer 107 on a silicon substrate 101 and forming a first pillar-shaped silicon layer 104 and a second pillar-shaped silicon layer 105 on the planar silicon layer 107.

[0035]

A second step will now be described. The second step includes forming a gate insulating film 109 around each of the first pillar-shaped silicon layer 104 and second pillar-shaped silicon layer 105,

forming a metal film 110 and a polysilicon film 111 around the gate insulating film 109,

the thickness of the polysilicon film 111 being smaller than half of a distance between the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105,

forming a third resist 112 for forming a gate line 114c, and

forming the gate line 114c by performing anisotropic etching.

[0036]

As shown in Fig. 9, a gate insulating film 109 is formed around each of the first pillar-shaped silicon layer 104 and second pillar-shaped silicon layer 105.

A metal film 110 and a polysilicon film 111 are formed

around the gate insulating film 109. Herein, a thin polysilicon film is used so that voids can be prevented from being formed in the polysilicon film.

The metal film 110 may be composed of any metal, such as titanium nitride, that is used in a semiconductor process and sets the threshold voltage of a transistor.

The gate insulating film 109 may be any film used in a semiconductor process, such as an oxide film, an oxynitride film, or a high-dielectric film.

[0037]

Next, as shown in Fig. 10, a third resist 112 for forming a gate line 114c is formed. In this embodiment, the description is made so that the height of the resist is smaller than that of each of the pillar-shaped silicon layers. This may be because, when the height of each of the pillar-shaped silicon layers is large, the thickness of a resist on an upper portion of the pillar-shaped silicon layer is decreased or the polysilicon film on an upper portion of the pillar-shaped silicon layer is exposed. As the width of the gate line decreases, the polysilicon film on the upper portion of the pillar-shaped silicon layer tends to be exposed.

The height of the resist may be larger than that of each of the pillar-shaped silicon layers.

[0038]

Furthermore, the third resist 112 is preferably formed so that the center line of the third resist 112 for forming the gate line is displaced from a line that connects the center point of the first pillar-shaped silicon layer 104 to the center point of the second pillar-shaped silicon layer 105. This is because a silicide that connects a second n-type diffusion layer 118 to a second p-type diffusion layer 121 is easily formed.

[0039]

Next, as shown in Fig. 11, the polysilicon film 111 and the metal film 110 are etched.

As a result, a polysilicon film 111a, a polysilicon film 111b, and a polysilicon film 111c are formed. Herein, if the thickness of the resist on the upper portion of each of the pillar-shaped silicon layers is small or the polysilicon film on the upper portion of each of the pillar-shaped silicon layers is exposed, the upper portion of each of the pillar-shaped silicon layers may be etched during the etching. In such a case, when each of the pillar-shaped silicon layers is formed, the height of the pillar-shaped silicon layer may be set to be the sum of a desired height of the pillar-shaped silicon layer and the height of a portion removed by gate-line etching performed later. Therefore, the production process of the present invention is a self-aligned process.

Since the metal film 110 is etched later, only the polysilicon film 111 may be etched in this process.

[0040]

Next, as shown in Fig. 12, the third resist 112 is removed.

The second step has been described, the second step including forming a gate insulating film 109 around each of the first pillar-shaped silicon layer 104 and second pillar-shaped silicon layer 105,

forming a metal film 110 and a polysilicon film 111 around the gate insulating film 109,

the thickness of the polysilicon film 111 being smaller than half of a distance between the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105,

forming a third resist 112 for forming a gate line 114c, and

forming the gate line 114c by performing anisotropic etching.

[0041]

A third step will now be described. The third step includes depositing a fourth resist 113 so that portions of the polysilicon films 111b and 111a on upper side walls of the first pillar-shaped silicon layer 104 and second pillar-shaped silicon layer 105 are exposed, removing the exposed

portions of the polysilicon films 111a and 111b by etching, removing the fourth resist 113, and removing the metal film 110 by etching to form a first gate electrode 114b and a second gate electrode 114a connected to the gate line 114c.

[0042]

As shown in Fig. 13, a fourth resist 113 is deposited so that portions of the polysilicon films 111b and 111a on upper side walls of the first pillar-shaped silicon layer 104 and second pillar-shaped silicon layer 105 are exposed. This is preferably performed by resist etch back. A coating film such as a spin-on-glass film may also be used.

[0043]

Next, as shown in Fig. 14, the exposed portions of the polysilicon films 111a and 111b are removed by etching. This is preferably performed by isotropic dry etching.

[0044]

Next, as shown in Fig. 15, the fourth resist 113 is removed.

[0045]

Next, as shown in Fig. 16, the metal film 110 is removed by etching to form a metal film 110b on a side wall of the first pillar-shaped silicon layer 104, a metal film 110a on a side wall of the second pillar-shaped silicon layer 105, and a metal film 110c below the polysilicon film 111c. This is preferably performed by isotropic etching.

The metal film 110b and the polysilicon film 111b constitute a first gate electrode 114b.

The metal film 110a and the polysilicon film 111a constitute a second gate electrode 114a.

The metal film 110c and the polysilicon film 111c constitute a gate line 114c. Therefore, this process is a self-aligned process.

[0046]

The third step has been described, the third step including depositing a fourth resist 113 so that portions of the polysilicon films 111b and 111a on upper side walls of the first pillar-shaped silicon layer 104 and second pillar-shaped silicon layer 105 are exposed, removing the exposed portions of the polysilicon films 111a and 111b by etching, removing the fourth resist 113, and removing the metal film 110 by etching to form a first gate electrode 114b and a second gate electrode 114a connected to the gate line 114c.

[0047]

A fourth step will now be described. The fourth step includes forming a first n-type diffusion layer 117 in an upper portion of the first pillar-shaped silicon layer 104,

forming a second n-type diffusion layer 118 in a lower portion of the first pillar-shaped silicon layer 104 and in an upper portion of the planar silicon layer 107,

forming a first p-type diffusion layer 120 in an upper

portion of the second pillar-shaped silicon layer 105, and

forming a second p-type diffusion layer 121 in a lower portion of the second pillar-shaped silicon layer 105 and in an upper portion of the planar silicon layer 107.

[0048]

As shown in Fig. 17, an oxide film 115 is deposited.

[0049]

Next, as shown in Fig. 18, a fifth resist 116 for forming a first n-type diffusion layer 117 and a second n-type diffusion layer 118 is formed.

[0050]

Next, as shown in Fig. 19, arsenic is implanted to form a first n-type diffusion layer 117 and a second n-type diffusion layer 118.

[0051]

Next, as shown in Fig. 20, the fifth resist 116 is removed.

[0052]

Next, as shown in Fig. 21, a sixth resist 119 for forming a first p-type diffusion layer 120 and a second p-type diffusion layer 121 is formed.

[0053]

Next, as shown in Fig. 22, boron or boron fluoride is implanted to form a first p-type diffusion layer 120 and a second p-type diffusion layer 121.

[0054]

Next, as shown in Fig. 23, the sixth resist 119 is removed.

[0055]

Next, as shown in Fig. 24, a nitride film 122 is deposited and a heat treatment is performed.

The fourth step has been described, the fourth step including forming a first n-type diffusion layer 117 in an upper portion of the first pillar-shaped silicon layer 104,

forming a second n-type diffusion layer 118 in a lower portion of the first pillar-shaped silicon layer 104 and in an upper portion of the planar silicon layer 107,

forming a first p-type diffusion layer 120 in an upper portion of the second pillar-shaped silicon layer 105, and

forming a second p-type diffusion layer 121 in a lower portion of the second pillar-shaped silicon layer 105 and in an upper portion of the planar silicon layer 107.

[0056]

A fifth step will now be described. The fifth step includes forming silicides on the first n-type diffusion layer 117, the second n-type diffusion layer 118, the first p-type diffusion layer 120, the second p-type diffusion layer 121, and the gate line 114c.

[0057]

As shown in Fig. 25, the nitride film 122 is etched to

form nitride film sidewalls 123, 124, and 125.

[0058]

Next, as shown in Fig. 26, the oxide film is etched to form oxide film sidewalls 127, 126, and 128. The nitride film sidewall 123 and the oxide film sidewall 127 constitute an insulating film sidewall 129. The nitride film sidewall 124 and the oxide film sidewall 126 constitute an insulating film sidewall 130. The nitride film sidewall 125 and the oxide film sidewall 128 on a side wall of the first pillar-shaped silicon layer 104 constitute an insulating film sidewall 131. The nitride film sidewall 125 and the oxide film sidewall 128 on a side wall of the second pillar-shaped silicon layer 105 constitute an insulating film sidewall 132.

[0059]

Herein, the thickness of the insulating film sidewall 129 formed on a side wall of the first n-type diffusion layer 117 is preferably larger than the sum of the thicknesses of the metal film 110b and polysilicon film 111b.

When the thickness of the insulating film sidewall 129 formed on a side wall of the first n-type diffusion layer 117 is larger than the sum of the thicknesses of the metal film 110b and polysilicon film 111b, a contact and the gate electrode 114b are easily insulated from each other during the formation of the contact.

[0060]

Next, as shown in Fig. 27, a metal is deposited, a heat treatment is performed, and an unreacted metal is removed to form silicides 134, 138, 136, 137, 133, and 135 on the first n-type diffusion layer 117, the second n-type diffusion layer 118, the first p-type diffusion layer 120, the second p-type diffusion layer 121, and the gate line 114c.

[0061]

The second n-type diffusion layer 118 and the second p-type diffusion layer 121 are connected to each other through the silicide 138. Since the center line of the gate line 114c is displaced from a line that connects the center point of the first pillar-shaped silicon layer 104 to the center point of the second pillar-shaped silicon layer 105, the silicide 138 is easily formed. Therefore, high degree of integration can be achieved.

[0062]

Since the polysilicon film wiring 111c is thin, the gate line 114c tends to have a laminated structure of the metal film 110c and the silicide 133. The silicide 133 and the metal film 110c are in direct contact with each other and thus the resistance can be decreased.

[0063]

The fifth step has been described, the fifth step including forming silicides on the first n-type diffusion layer 117, the second n-type diffusion layer 118, the first

p-type diffusion layer 120, the second p-type diffusion layer 121, and the gate line 114c.

[0064]

Next, as shown in Fig. 28, a contact stopper 139 such as a nitride film is formed and an interlayer insulating film 140 is formed.

[0065]

Next, as shown in Fig. 29, a seventh resist 141 for forming contact holes 142 and 143 is formed.

[0066]

Next, as shown in Fig. 30, the interlayer insulating film 140 is etched to form contact holes 142 and 143. In the case where the thickness of the insulating film sidewall 129 formed on a side wall of the first n-type diffusion layer 117 is larger than the sum of the thicknesses of the metal film 110b and polysilicon film 111b, even if the seventh resist is formed in a misaligned manner and the contact holes are formed by overetching, a short circuit between the contact and the gate electrode 114b can be prevented.

[0067]

Next, as shown in Fig. 31, the seventh resist 141 is removed.

[0068]

Next, as shown in Fig. 32, an eighth resist 144 for

forming contact holes 145 and 146 is formed.

[0069]

Next, as shown in Fig. 33, the interlayer insulating film 140 is etched to form contact holes 145 and 146.

[0070]

Next, as shown in Fig. 34, the eighth resist 144 is removed.

[0071]

Next, as shown in Fig. 35, portions of the contact stopper 139 below the contact holes 142 and 143 and the contact holes 145 and 146 are removed by etching.

[0072]

Next, as shown in Fig. 36, a metal is deposited to form contacts 147, 148, 149, and 150.

[0073]

Next, as shown in Fig. 37, a metal 151 for metal wirings is deposited.

[0074]

Next, as shown in Fig. 38, ninth resists 152, 153, 154, and 155 for forming metal wirings are formed.

[0075]

Next, as shown in Fig. 39, the metal 151 is etched to form metal wirings 156, 157, 158, and 159.

[0076]

Next, as shown in Fig. 40, the ninth resists 152, 153,

154, and 155 are removed.

The method for producing an SGT in which a thin gate material is used, a metal gate is employed, and a self-aligned process is performed has been described.

[0077]

Fig. 1 shows the structure of a semiconductor device produced by the above production method.

As shown in Fig. 1, the semiconductor device includes:

a planar silicon layer 107 formed on a silicon substrate 101;

first and second pillar-shaped silicon layers 104 and 105 formed on the planar silicon layer 107;

a gate insulating film 109 formed around the first pillar-shaped silicon layer 104;

a first gate electrode 114b having a laminated structure of a metal film 110b and a polysilicon film 111b, both of which are formed around the gate insulating film 109;

a gate insulating film 109 formed around the second pillar-shaped silicon layer 105;

a second gate electrode 114a having a laminated structure of a metal film 110a and a polysilicon film 111a, both of which are formed around the gate insulating film 109 formed around the second pillar-shaped silicon layer 105;

the thickness of the polysilicon films 111b and 111a

being smaller than half of a distance between the first pillar-shaped silicon layer 104 and the second pillar-shaped silicon layer 105;

a gate line 114c connected to the first gate electrode 114b and second gate electrode 114a;

an upper surface of the gate line 114c being located at a lower position than those of the first and second gate electrodes 114b and 114a;

a first n-type diffusion layer 117 formed in an upper portion of the first pillar-shaped silicon layer 104;

a second n-type diffusion layer 118 formed in a lower portion of the first pillar-shaped silicon layer 104 and in an upper portion of the planar silicon layer 107;

a first p-type diffusion layer 120 formed in an upper portion of the second pillar-shaped silicon layer 105; and

a second p-type diffusion layer 121 formed in a lower portion of the second pillar-shaped silicon layer 105 and in an upper portion of the planar silicon layer 107.

[0078]

The gate line 114c has a laminated structure of the metal film 110c and the silicide 133. The silicide 133 and the metal film 110c are in direct contact with each other and thus the resistance can be decreased.

[0079]

The thickness of the insulating film sidewall 129

formed on a side wall of the first n-type diffusion layer 117 is larger than the sum of the thicknesses of the metal film 110b and polysilicon film 111b.

Even if the seventh resist is formed in a misaligned manner and the contact holes are formed by overetching, a short circuit between the contact 148 and the gate electrode 114b can be prevented.

[0080]

The center line of the gate line 114c is displaced from a line that connects the center point of the first pillar-shaped silicon layer 104 to the center point of the second pillar-shaped silicon layer 105 by a first predetermined distance.

The silicide 138 that connects the second n-type diffusion layer 118 to the second p-type diffusion layer 121 is easily formed. Therefore, high degree of integration can be achieved.

[0081]

In the present invention, various embodiments and modifications can be made without departing from the broad sprit and scope of the present invention. Furthermore, the above-described embodiment is provided to describe one embodiment of the present invention, and the scope of the present invention is not limited thereto.

[0082]

For example, a method for producing a semiconductor device in which the p-type (including the p^+-type) and the n-type (including the n^+-type) are each changed to the opposite conductivity type in the above embodiment, and a semiconductor device produced by the method are also obviously included in the technical scope of the present invention.

Reference Signs List

[0083]

101. silicon substrate

102. first resist

103. first resist

104. first pillar-shaped silicon layer

105. second pillar-shaped silicon layer

106. second resist

107. planar silicon layer

108. element separation film

109. gate insulating film

110. metal film

110a. metal film

110b. metal film

110c. metal film

111. polysilicon film

111a. polysilicon film

111b. polysilicon film

111c. polysilicon wiring

112. third resist

113. fourth resist

114a. second gate electrode

114b. first gate electrode

114c. gate line

115. oxide film

116. fifth resist

117. first n-type diffusion layer

118. second n-type diffusion layer

119. sixth resist

120. first p-type diffusion layer

121. second p-type diffusion layer

122. nitride film

123. nitride film sidewall

124. nitride film sidewall

125. nitride film sidewall

126. nitride film sidewall

127. oxide film sidewall

128. oxide film sidewall

129. insulating film sidewall

130. insulating film sidewall

131. insulating film sidewall

132. insulating film sidewall

133. silicide

134. silicide

135. silicide

136. silicide

137. silicide

138. silicide

139. contact stopper

140. interlayer insulating film

141. seventh resist

142. contact hole

143. contact hole

144. eighth resist

145. contact hole

146. contact hole

147. contact

148. contact

149. contact

150. contact

151. metal

152. ninth resist

153. ninth resist

154. ninth resist

155. ninth resist

156. metal wiring

157. metal wiring

158. metal wiring

159. metal wiring

CLAIMS

1. A semiconductor device, comprising:

a planar silicon layer formed on a silicon substrate;

first and second pillar-shaped silicon layers formed on the planar silicon layer;

a gate insulating film formed around the first pillar-shaped silicon layer;

a first gate electrode formed around the gate insulating film;

a gate insulating film formed around the second pillar-shaped silicon layer;

a second gate electrode formed around the gate insulating film;

a gate line connected to the first and second gate electrodes, wherein a center line of the gate line is displaced by a predetermined distance from an imaginary line joining a center point of the first pillar-shaped silicon layer to a center point of the second pillar-shaped silicon layer; and wherein the thickness of each of the first and second gate electrodes being smaller than half of a distance between the first pillar-shaped silicon layer and the second pillar-shaped silicon layer so that a portion of the gate line between the first and second pillar-shaped silicon layers also mutually

connects the first and second gate electrodes;

an upper surface of the gate line being located at a lower position than upper surfaces of the first and second gate electrodes;

a first n-type diffusion layer formed in an upper portion of the first pillar-shaped silicon layer;

a second n-type diffusion layer formed in a lower portion of the first pillar-shaped silicon layer and in an upper portion of the planar silicon layer;

a first p-type diffusion layer formed in an upper portion of the second pillar-shaped silicon layer; and

a second p-type diffusion layer formed in a lower portion of the second pillar-shaped silicon layer and in an upper portion of the planar silicon layer.

2. The semiconductor device according to claim 1, wherein the thickness of the insulating film sidewall formed on a side wall of the first n-type diffusion layer is larger than the sum of the thicknesses of the first gate electrode.

3. The semiconductor device according to claim 1, further comprising silicides formed on the first and second n-type diffusion layers and the first and second p-type diffusion layers.