

POWER MANAGEMENT FOR DIGITAL DEVICES

RELATED APPLICATIONS

This application claims priority to U.S. Provisional Application Serial No. 60/562,374 filed April 15, 2004, the teachings of which are hereby incorporated by
5 reference in its entirety.

BACKGROUND OF THE INVENTION

Field

This disclosure relates to power management for digital devices.
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Background Art

Power management for digital devices is increasingly important as devices become smaller and more portable.

BRIEF DESCRIPTION OF THE DRAWINGS

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Features and advantages of embodiments of the claimed subject matter will become apparent as the following Detailed Description proceeds, and upon reference to the Drawings, wherein like numerals depict like parts, and in which:

20 Figure 1 is a diagram illustrating a system embodiment; and

Figure 2 is a block diagram illustrating the internal structure of a power management processor according to one embodiment.

Although the following Detailed Description will proceed with reference being made to illustrative embodiments, many alternatives, modifications, and variations thereof will be apparent to those skilled in the art. Accordingly, it is intended that the claimed subject matter be viewed broadly, and be defined only as set forth in the accompanying claims.

DETAILED DESCRIPTION

Figure 1 illustrates a system embodiment 100 of the claimed subject matter. The system 100 may generally include a host processor 104 and a power management unit 102. The system 100 may comprise a digital device, such as a digital camera. The host processor 104 and power management unit 102 may each comprise one or more integrated circuits, and may form the core electronic components and/or core logic of a digital camera. As used in any embodiment herein, an "integrated circuit" means a semiconductor device and/or microelectronic device, such as, for example, a semiconductor integrated circuit chip. "Digital camera", as used in any embodiment herein, may comprise a still image digital camera or a video digital camera. As will be described in greater detail below, host processor 104 and power management unit 102 may each comprise circuitry. As used in any embodiment herein, "circuitry" may comprise, for example, singly or in any combination, hardwired circuitry, programmable circuitry, state machine circuitry, and/or firmware that stores instructions executed by programmable circuitry.

Although not shown in Figure 1, the system 100 may also comprise memory which may comprise one or more of the following types of memory: semiconductor firmware memory, programmable memory, non-volatile memory, read only memory, electrically programmable memory, random access memory, flash memory, magnetic disk memory, and/or optical disk memory. Either additionally or alternatively, memory
5 may comprise other and/or later-developed types of computer-readable memory. Machine-readable firmware program instructions may be stored in memory. As described below, these instructions may be accessed and executed by power management unit 102 and/or host processor 104 and/or other circuitry comprised in system 100, and
10 these instructions may result in power management unit 102 and/or host processor 104 and/or other circuitry comprised in system 100 performing operations which may be attributed to these components.

The system 100 may comprise one or more sensor circuits 106 which may be
15 capable of sensing, for example, temperature, current, and/or lens position. Power management processor 150 may be capable of receiving signals from one or more sensors 106. Also, the system embodiment may include button input circuitry 108 capable of generating one or more signals from a user interface selector (not shown). Power management processor 150 may be capable of receiving signals from one or more user
20 activated buttons 108. In this embodiment, a power management processor 150 may be provided that may be capable of allocating power from a plurality of sources based on, for example, system power requirements and/or preprogrammed power commands, as will be detailed below. The power management processor 150 may comprise circuitry

capable of generating one or more signals and interfacing to one or more circuit components of the system 100. Power management processor 150 and host processor 104 may be capable of exchanging commands and data with each other. For example, host processor 104 may be capable of communicating data with power management processor 150 regarding power requirements and/or other system aspects of one or more components comprised in a digital camera.

System 100 may also comprise a main battery power supply 110. Battery 110 may comprise one or more rechargeable batteries, as is well understood in the art.

10 Battery 110 may also comprise a temperature sensor 112 which may be capable of generating a signal indicative of temperature conditions at or near one or more battery cells comprised in battery 110. System 100 may also include an adapter power input 114 and one or more interface power inputs 116 (depicted as Interface #1...Interface #N in Figure 1). Adapter power 114 may comprise, for example, an AC/DC adapter or other

15 adapter which may be associated with an electronic device. Interface 116 may comprise, for example, a data interface which may include an I2C interface, FireWire interface, and/or other interface as may be known in the art. Each of the power supplies 110, 114 and 116 may be capable of providing power to one or more components comprised in the system 100. Connecting device circuitry may be coupled to one or more of the power

20 supplies, for example, connecting device circuitry 122 coupled to power supply 110, connecting device circuitry 124 coupled to power supply 114, connecting device circuitry 130 coupled to interface power supply #1, and/or connecting device circuitry 134 coupled to interface power supply #N. One or more of the connecting device circuitry may be

controlled by the power management processor 150 (using analog and/or digital control signals) to couple or decouple a selected power supply (110, 114 and/or 116) from a power rail which may be comprised in system 100.

5 System 100 may also comprise battery charger circuitry 120. Battery charger circuitry 120 may be capable of receiving adapter power 114 and/or power from one or more interfaces 116 and further capable of supplying charging current and/or voltage to one or more batteries comprised in the battery 110. Current sense circuitry 118 may be coupled to the output of battery charger circuitry 120 and may be capable of generating a
10 signal indicative of battery charging current and/or voltage, as may be supplied to battery 110. Battery charger circuitry 120 may be capable of charging the battery 110 when the digital camera is ON, and power processor 150 may be capable of allocating power between the charger 120 (to charge the battery 110) and system power requirements. Another current sense circuitry 126 may be coupled to the adapter power input 114 and
15 capable of generating a signal indicative of external adapter current, as may be provided to one or more components of system 100. Processor 150 may be capable of generating control signals to enable and/or disable operation of the battery charger circuitry 120.

 System 100 may also comprise a suspend power regulator (SUS) 132. An SUS
20 132 may be utilized to provide a regulated output voltage to a load. SUS may be utilized when the regulated voltage level for a particular load of the electronic device is not available from a main supply voltage source and/or the supply voltage is not high enough for the particular load. SUS may comprise an LDO that can typically provide such

regulated output voltage with relatively little voltage drop across it. The SUS circuitry 132 may be coupled to a power bus (connected to IN2) which may comprise power from one or more power supplies. SUS circuitry 132 may also be coupled to a coin cell battery or other back-up power source as the system of Figure 1 comprises such back-up source.

- 5 SUS circuitry may be controlled by processor 150, for example, to select SUS circuitry 132 input power.

- System 100 may also comprise power converter circuitry, as may be embodied by one or more power converter circuits 138, 140, 142 and/or 144. Power converter
- 10 circuitry 138, 140, 142 and/or 144 may be capable of generating a desired power output, for example, as may be required by one or more components of a digital camera. Power converter circuitry 138, 140, 142 and/or 144 may also be capable of generating a voltage and/or current feedback signal indicative of the voltage and/or current being supplied by the power converter circuitry. Such feedback signals may be communicated to power
- 15 management processor 150.

- System 100 may also comprise LED driver circuitry 146 capable of supplying power to one or more white LEDs for lighting an LCD panel (not shown) which may be included with a digital camera. The LED driver circuitry 146 may also be capable of
- 20 generating voltage and/or current feedback information to processor 150. Processor 150 may be capable of generating control signal to LED driver circuitry 146 to control the amount of power delivered to an LED, which may operate to control the brightness and/or contrast of the LCD panel. The system 100 may also comprise photoflash

capacitor charger circuitry 136 which may be capable of charging a photoflash capacitor (not shown) to enable operation of a flash which may be included with a digital camera. The photoflash capacitor charger circuitry 136 may also be capable of generating voltage and/or current feedback information to processor 150. Processor 150 may be capable of
5 generating control signal to photoflash capacitor charger circuitry 136 to control the amount of power delivered by the photoflash capacitor charger circuitry 136.

As stated previously, in this embodiment, power management processor 150 may be capable of allocating power to one or more components depicted in Figure 1. For
10 example, power management processor 150 may be capable of allocating power to one or more components depicted in Figure 1 based on available power from the battery 110, the adapter 114 and/or one or more interface power supplies 116. Power management processor 150 may execute instructions to manage power to one or more components based on, for example, a preprogrammed and/or user-definable priority. Power
15 management processor may be capable of controlling one or more components 136, 138, 140, 142, 144 and/or 146 and/or other components to enable and/or disable these components based on preprogrammed and/or user-definable priority. Accordingly, and using feedback information as may be supplied by one ore more power supplies as set forth above, power management processor 150 may be capable of monitoring power
20 availability from one or more power supplies and allocating power to one or more components based on available power, preprogrammed priority and/or user-defined priority of power usage in the system 100.

Figure 2 illustrates an exemplary power management processor 150 according to one embodiment. Power management processor 150 may comprise core logic circuitry 218 which may be capable of performing one or more operations described herein associated with the processor 150. Memory 234 may comprise instructions and core logic circuitry 218 may be capable of executing instructions stored in memory 234. For example power allocation instructions, as described herein, may be stored in memory 234. Core processor 218 may be capable of exchanging commands and data with the core components of a digital camera.

The power management processor 150 may also comprise communication interface circuitry 232. Core processor 218 may be capable of exchanging commands and data with the core components of a digital camera via communications interface circuitry 232. Additionally, core processor 218 may utilize serial communication interface 232 to obtain information and commands from the system and use them to change the functional characteristics (voltage, current, timing, etc.) of one or more power supplies. The serial interface may also be used in IC testing process to increase the speed and the testability.

Processor 150 may also comprise selector circuitry 202 that selects the system power supply out of two or more internal and/or external power sources, including different interfaces that may provide power. Processor 150 may be capable of managing the priorities and the restrictions associated to these power supplies while assuring the system power integrity. The restrictions associated to the external power supplies could

be, but not limited to, maximum allowed current, minimum and/or maximum voltage, the necessity of an explicitly approval of use, etc.

If power is being provided by an interface, selector circuitry 202 may be capable
5 of detecting the interface connection presence, waiting for hand-shake and usage
approval if necessary, and connecting the interface power to the system's power rail. The
selector 202 may be capable of limiting the current sunk from the interface at a specified
value, and may also be capable of protecting the interface connection against inrush and
reverse current and over-current. In order to fulfill the protection requirements and to
10 assure the system power integrity and the battery protection, the selector circuitry may be
capable of performing "make-before-brake" (MBB) operations in the case of low battery
voltage, and/or "brake-before-make" (BBM) operations in the case of high battery
voltage. After the interface power has been connected to the system, the selector 202
may be capable of protecting the system against over-current by switching back to the
15 battery power if a current limit is exceeded.

Processor 150 may also comprise a switching mode battery charger circuitry 204.
The battery charger may comprise circuitry that supplies a consistent fast charge of the
battery with very low dissipation. The charger may be capable of automatically tuning its
20 charging characteristics to the battery status. Thus, battery charger may be capable of a
low pre-charge current for deeply discharged batteries, a fast, constant current (CC)
charge for a normal discharged battery, followed by a constant voltage (CV) top-off

charge. The charger 204 may terminate the charging when the battery is full by monitoring the charging current in CV mode.

The charger circuitry 204 may be capable of a high level of battery protection by
5 limiting very accurately the charging terminal voltage, the charging time or maximum electrical charge detected by the adaptive battery gas-gauge. Battery temperature may also be monitored and the charging stopped if this temperature is out of the safe range. The charger may also include short-circuit protection circuitry.

10 A Suspend power source (SUS) may be capable of using any of internal and/or external power sources, including a coin-cell battery, if available. SUS may comprise no-reverse-current-circuitry (NRCC) to condition the power. NRCC may comprise a high efficiency voltage boost converter, which works only when need is, and/or a no-reverse-current LDO based on one or more of the following: Sensing the LDO's output current,
15 Sensing the voltage difference between input and output, Using a built-in reverse current blocking switch, and/or Using a reversible serial device for regulation, MOS or Bipolar technology. No reverse current LDO may be capable of saving coin cell energy while any of the other power supplies is not available, blocking the reverse current to the main power rail, and preserving the charge status of the coin cell. Further, no reverse current
20 LDO circuitry may also be capable of controllably recharging the coin cell when one or more power supplies are available.

Button panel interface circuitry 224 may be provided to switch the system power ON and OFF and/or takes other manual user commands. When the power is switched from ON to OFF, logic 218 may communicate beforehand with the host system in order to prevent inadequate power-off operation that may cause data loss.

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The processor 150 may also comprise one or more switching mode power supplies (SMPS) and/or linear regulators 210 which may be capable of conditioning the power available on one or more system power rails, and may provide the appropriate voltages and/or currents to components of the system. SMPSs 210 may comprise, for example, buck converters, boost converters, buck-boost converters, flyback converters, Cuk basic and/or modified converters, SEPIC converters, etc., having one or multiple output voltages. Circuitry 210 may regulate the output voltage or current to correspond to the system load requirements. Circuitry 210 may also comprise controller circuitry which may control the output power, via for example, by controlling the ON/OFF status, voltage, current, duty cycle, etc. Logic 218 may control circuitry 210 to dynamically allocate of the input available power on a time or priority base, as may be programmed and/or user-defined. The output power parameters may be controlled by the LOGIC based on the information it receives from the system and/or using external hardware signals. These signals may come from the system or from sensors, including, but not limiting to voltage, current, and temperature sensors, etc.

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Thus, the power management for digital devices according to the present disclosure may have several advantages over conventional digital devices. For example,

logic circuitry 218 may provide real time adaptive optimization of power consumption, taking into consideration the system power requirement, the priorities as programmed, the available power, and/or any restrictions on power usage. Charger circuitry 208 may be capable of performing battery charging operations, even in the case the system is on.

- 5 External power (as may be provided by an adapter and/or interface power) may be allocated with priority to the system, while the remaining power may be allocated to the charger circuitry 208.

When necessary, logic circuitry 218 may limit and/or prioritize the power for the
10 low priority system blocks, as may be defined. Therefore, logic circuitry 218 may avoid current surge, excessive battery voltage drop, and system shut down caused by these events. For example, when the logic circuitry 218 determines that the battery voltage is too low to support a power converter consumption simultaneously with the photoflash capacitor charging at full speed, it may reduce the photoflash power by increasing the
15 charging time, or may simply stop it until the operation requiring high power has elapsed.

Also, logic circuitry 218 may be capable of managing power from multiple sources, including power provided by one or more interfaces. Logic circuitry may comprise detection circuitry to detect the presence of an interface connection, which may
20 comprise negotiation circuitry to enable handshaking protocols and/or speed negotiation with the interface. Logic circuitry may be capable of monitoring available power and communicating with the system, and obtaining information from the system for appropriate power allocation. Logic circuitry is able to manage the priorities and the

restrictions associated to interface power supplies while assuring the system power integrity.

Logic 218 may also be capable of correlating the working frequencies of the
5 different SMPS circuits to minimize the spectral power density over a large bandwidth and the noise. While correlating the SMPS working frequencies, logic 218 can be programmed to take into consideration the optimum range for each converter. Thus, the operation can be performed without affecting the individual efficiency.

10 The logic 218 may use available information to monitor, for example, temperature, current, and/or voltage, to enable protection of system components. Also, logic has available direct battery current information and an accurate reference voltage, even in the case the power rail has a very low voltage, the processor 150 may also comprise battery gas-gauge circuitry 222. Battery gas gauge circuitry 222 may provide
15 the logic 218 and the charger 208 with battery capacity information used in the power management and for battery protection while charging.

Those skilled in the art may recognize numerous modifications, alterations or enhancements to one or more of the embodiments described herein. The terms and
20 expressions which have been employed herein are used as terms of description and not of limitation, and there is no intention, in the use of such terms and expressions, of excluding any equivalents of the features shown and described (or portions thereof), and it is recognized that various modifications are possible within the scope of the claims.

Other modifications, variations, and alternatives are also possible. Accordingly, the claims are intended to cover all such equivalents.

CLAIMS

What is claimed is:

1. An apparatus, comprising:
an integrated circuit comprising a power management unit capable of coupling at least one power supply to a power bus, said power management unit further capable of allocating power to at least one component of a digital camera by coupling at least one said component to said power bus based on at least one power management priority rule.
2. The apparatus of claim 1, wherein:
said at least one power supply is selected from the group consisting of a battery power supply, and adapter power supply, an interface power supply and a coin cell power supply.
3. The apparatus of claim 1, wherein:
said power management priority rule comprises selecting at least one said component and allocating available power to said at least one selected component.
4. The apparatus of claim 1, wherein:
said integrated circuit is further capable of receiving feedback information from at least one said component, and said power management priority rule comprises allocating power to at least one said component based on, at least in part, said feedback information.

5. The apparatus of claim 1, wherein:

said integrated circuit further comprising battery charger circuitry capable of charging at least one rechargeable battery, said integrated circuit further capable of allocating, at least in part, said at least one power supply, to said battery charger circuitry to charge said rechargeable battery.

6. The apparatus of claim 1, wherein said power management unit is capable of managing priorities in allocating power to components of said digital camera.

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7. The apparatus of claim 1, further comprising:

a selector circuit for performing "make-before-brake" operations in the case of low battery voltage when supplying power to at least one said component.

15 8. A method, comprising:

coupling at least one power supply to a power bus comprised in a digital camera;

and

allocating power to at least one component of said digital camera by coupling at least one said component to said power bus based on at least one power management

20 priority rule.

9. The method of claim 8, wherein:

said power management priority rule comprises selecting at least one said component and allocating available power to said at least one selected component.

10. The method of claim 8, further comprising:
5 receiving feedback information from at least one said component, and said power management priority rule comprises allocating power to at least one said component based on, at least in part, said feedback information.

11. The method of claim 8, further comprising:
10 allocating, at least in part, said at least one power supply, to charge at least one rechargeable battery.

12. The method of claim 8, further comprising:
managing priorities in allocating power to components of said digital camera
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13. The method of claim 8, further comprising:
performing "brake-before-make" operations in the case of high battery voltage when supplying power to at least one said component.

20 14. A system, comprising:
a digital camera comprising an integrated circuit, said integrated circuit comprising a power management unit capable of coupling at least one power supply to a power bus, said power management unit further capable of allocating power to at least

one component of a digital camera by coupling at least one said component to said power bus based on at least one power management priority rule.

15. The system of claim 14, wherein:

5 said at least one power supply is selected from the group consisting of a battery power supply, and adapter power supply, an interface power supply and a coin cell power supply.

16. The system of claim 14, wherein:

10 said power management priority rule comprises selecting at least one said component and allocating available power to said at least one selected component.

17. The system of claim 14, wherein:

15 said integrated circuit is further capable of receiving feedback information from at least one said component, and said power management priority rule comprises allocating power to at least one said component based on, at least in part, said feedback information.

18. The system of claim 14, wherein:

20 said integrated circuit further comprising battery charger circuitry capable of charging at least one rechargeable battery, said integrated circuit further capable of allocating, at least in part, said at least one power supply, to said battery charger circuitry to charge said rechargeable battery.

19. The system of claim 14, wherein:

said digital camera is selected from a still image digital camera and a video digital camera.

5 20. The system of claim 14, wherein said power management unit is capable of managing priorities in allocating power to components of said digital camera.

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