

form a seed layer for the epitaxial growth of the gallium nitride) on a polycrystalline SiC substrate, respectively. Although polycrystalline SiC is a material that is inexpensive, that is available in the form of substrates of large size and that dissipates heat well, these composite structures are penalized by the presence of a layer of silicon oxide at the interface between the layer of single-crystal silicon or SiC and the polycrystalline SiC substrate, which forms a thermal barrier hindering the dissipation of heat from the layer of III-N alloy to the polycrystalline SiC substrate.

Brief description of the invention

- [10] One aim of the invention is therefore to remedy the aforementioned drawbacks and in particular limitations related to the size and cost of semi-insulating SiC substrates.
- [11] The aim of the invention is therefore to provide a process for fabricating a substrate for the epitaxial growth of a III-N alloy based on gallium, in particular with a view to forming HEMTs or other high-frequency, high-power electronic devices in which RF losses ~~are~~ may be minimized and the dissipation of heat ~~is~~ may be maximized.
- [12] ~~To this end,~~ An aspect of the invention provides a process for fabricating a substrate for epitaxial growth of a layer of gallium nitride (GaN), of aluminium gallium nitride (AlGaN) or of indium gallium nitride (InGaN), comprising the following successive steps:
 - providing a single-crystal silicon-carbide donor substrate,
 - implanting ionic species into the donor substrate so as to form a weakened region that defines a thin layer of single-crystal SiC to be transferred,
 - bonding the donor substrate to a first receiver substrate via a bonding layer,
 - detaching the donor substrate along the weakened region so as to transfer the thin layer of SiC to the first receiver substrate,
 - performing epitaxial growth of a layer ~~(30)~~ of semi-insulating SiC having a thickness larger than 1 μm on the thin layer of SiC,
 - bonding the layer of semi-insulating SiC to a second receiver substrate, said second receiver substrate having a high electrical resistivity,
 - removing at least one portion of the bonding layer so as to detach the first receiver substrate,
 - removing the transferred thin layer of single-crystal SiC, so as to uncover the layer of semi-insulating SiC.
- [13] By “high-frequency”, what is meant in the present text is a frequency higher than 3 kHz.
- [14] By “high-power”, what is meant in the present text is a power higher than 0.5 W/mm injected through the gate of the transistor.
- [15] By “high electrical resistivity”, what is meant in the present text is an electrical resistivity higher than or equal to 100 $\Omega\cdot\text{cm}$.
- [16] By “semi-insulating SiC”, what is meant in the present text is silicon carbide having an electrical resistivity higher than or equal to $10^5 \Omega\cdot\text{cm}$.
- [17] This process allows a substrate, based on silicon or another low-cost material of high electrical resistivity available in large size, comprising a layer of semi-insulating SiC

having a crystal quality suitable for the subsequent epitaxial growth of a layer of III-N alloy to be formed and the final structure to benefit from the good properties thereof as regards the dissipation of heat and the limitation of RF losses. Since the layer of semi-insulating SiC makes direct contact with the silicon substrate (or substrate of another material of high electrical resistivity), the structure further contains no thermal barrier.

- [18] A process that consisted in forming the layer of semi-insulating SiC by epitaxy directly on a silicon substrate of high electrical resistivity would lead to the formation of a high number of dislocations in the semi-insulating SiC because of the difference in lattice parameter between silicon and silicon carbide. In contrast, the process according to embodiments of the invention makes it possible to use, as seed for the growth of the semi-insulating SiC, a layer of single-crystal SiC the quality of which ~~is~~ may be optimal because it was obtained via transfer from the donor substrate.
- [19] Moreover, the use of the first receiver substrate, which plays the role of temporary carrier, ~~may allow~~s the silicon face of the SiC to be oriented optimally in the various steps of the process.
- [20] According to advantageous but optional features of the process, which may be implemented separately or in any technically possible combination thereof:
- [21] - the first receiver substrate and the donor substrate have a difference in coefficient of thermal expansion smaller than or equal to $3 \times 10^{-6} \text{ K}^{-1}$;
- [22] - the first receiver substrate is an SiC substrate having a crystal quality lower than that of the donor substrate;
- [23] - the thin layer of single-crystal SiC transferred to the first receiver substrate has a thickness smaller than $1 \text{ }\mu\text{m}$;
- [24] - the bonding layer is formed from a material that remains thermally stable during the epitaxial growth of the layer of semi-insulating SiC and that is able to be removed from the interface between the transferred layer of single-crystal SiC and the first receiver substrate;
- [25] - the bonding layer is a layer of silicon nitride or of gallium nitride;
- [26] - removing at least one portion of the bonding layer comprises a chemical etch, a delamination by laser and/or the application of a mechanical stress;
- [27] - the layer of semi-insulating SiC is formed by doping with vanadium during the epitaxial growth of the SiC;
- [28] - the layer of semi-insulating SiC is formed by simultaneously depositing silicon, carbon and vanadium;
- [29] - the second receiver substrate is a silicon substrate having an electrical resistivity higher than or equal to $100 \text{ }\Omega\cdot\text{cm}$;
- [30] - the epitaxial layer of semi-insulating SiC has a thickness comprised between 1 and $5 \text{ }\mu\text{m}$;
- [31] - the second receiver substrate is a polycrystalline SiC substrate or a polycrystalline AlN substrate having an electrical resistivity higher than or equal to $100 \text{ }\Omega\cdot\text{cm}$;
- [32] - the epitaxial layer of semi-insulating SiC has a thickness smaller than or equal to $80 \text{ }\mu\text{m}$;

- [33] - the process further comprises a step of recycling the segment of the donor substrate detached from the transferred layer, with a view to forming a new donor substrate;
- [34] - the ionic species are implanted through the silicon face of the donor substrate, and the silicon face of the donor substrate is bonded to the first receiver substrate, so that, after the transferred thin layer of single-crystal SiC has been removed, the silicon face of the layer of semi-insulating SiC is uncovered.
- [35] Another ~~subject-aspect~~ of the invention ~~relates to~~provides a process for fabricating by epitaxy a layer of ~~a III-N alloy based on gallium on a substrate obtained using the process that has just been described~~nitride.
- [36] Said process comprises:
- providing a substrate fabricated using the process such as described above,
 - performing epitaxial growth of the layer of gallium nitride on the layer of semi-insulating SiC of said substrate.
- [37] In certain embodiments, the layer of gallium nitride has a thickness comprised between 1 and 2 μm .
- [38] Another ~~subject-aspect~~ of the invention ~~relates to~~provides a process for fabricating a high-electron-mobility transistor (HEMT) ~~in such a layer of III-N alloy~~.
- [39] Said process comprises:
- fabricating by epitaxy a layer of gallium nitride, of aluminium gallium nitride or of indium gallium nitride using the process such as described above,
 - forming a heterojunction by epitaxy, on said layer, of a layer of a III-N material different from the material of said layer,
 - forming a channel of the transistor level with said heterojunction,
 - forming a source, a drain and a gate of the transistor on the channel.

Brief description of the drawings

- [40] Further features and advantages of the invention will become apparent from the following detailed description, with reference to the appended drawings, in which:
- [41] [Fig 1] is a schematic cross-sectional view of a single-crystal SiC donor substrate;
- [42] [Fig 2] is a schematic cross-sectional view of the donor substrate of Figure 1, in which substrate a weakened region has been formed by implanting ionic species in order to define a thin layer to be transferred;
- [43] [Fig 3] is a schematic cross-sectional view of a temporary carrier covered with a removable bonding layer;
- [44] [Fig 4] is a schematic cross-sectional view of the temporary carrier of Figure 3 being joined to the donor substrate of Figure 2 via the removable bonding layer;
- [45] [Fig 5] is a schematic cross-sectional view of the donor substrate being detached along the weakened region in order to transfer the thin layer of single-crystal SiC to the temporary carrier;
- [46] [Fig 6] is a schematic cross-sectional view of the thin layer of single-crystal SiC transferred to the temporary carrier after its free surface has been polished;

Claims

- [Claim 1] A Process for fabricating a substrate for epitaxial growth of a layer of gallium nitride (GaN), of aluminium gallium nitride (AlGaN) or of indium gallium nitride (InGaN), comprising the following successive steps:
- providing a single-crystal silicon-carbide donor substrate ~~(10)~~,
 - implanting ionic species into the donor substrate ~~(10)~~ so as to form a weakened region ~~(12)~~ that defines a thin layer ~~(11)~~ of single-crystal SiC to be transferred,
 - bonding the donor substrate ~~(10)~~ to a first receiver substrate ~~(20)~~ via a bonding layer ~~(21)~~,
 - detaching the donor substrate ~~(10)~~ along the weakened region ~~(12)~~ so as to transfer the thin layer ~~(11)~~ of SiC to the first receiver substrate ~~(20)~~,
 - performing epitaxial growth of a layer ~~(30)~~ of semi-insulating SiC having a thickness larger than 1 μm on the thin layer ~~(11)~~ of SiC,
 - bonding the layer ~~(30)~~ of semi-insulating SiC to a second receiver substrate ~~(40)~~, said second receiver substrate ~~(40)~~ having a high electrical resistivity,
 - removing at least one portion of the bonding layer ~~(21)~~ so as to detach the first receiver substrate ~~(20)~~,
 - removing the transferred thin layer ~~(11)~~ of single-crystal SiC, so as to uncover the layer ~~(30)~~ of semi-insulating SiC.
- [Claim 2] The Process according to Claim 1, wherein the first receiver substrate ~~(20)~~ and the donor substrate ~~(10)~~ have a difference in coefficient of thermal expansion smaller than or equal to $3 \times 10^{-6} \text{ K}^{-1}$.
- [Claim 3] The Process according to either of Claims 1 and 2, wherein the first receiver substrate ~~(20)~~ is an SiC substrate having a crystal quality lower than that of the donor substrate.
- [Claim 4] The Process according to one of Claims 1 to 3, wherein the thin layer ~~(11)~~ of single-crystal SiC transferred to the first receiver substrate ~~(20)~~ has a thickness smaller than 1 μm .
- [Claim 5] The Process according to one of Claims 1 to 4, wherein the bonding layer ~~(21)~~ is formed from a material that remains thermally stable during the epitaxial growth of the layer ~~(30)~~ of semi-insulating SiC and that is able to be removed from the interface between the transferred layer ~~(11)~~ of single-crystal SiC and the first receiver substrate ~~(20)~~.
- [Claim 6] The Process according to one of Claims 1 to 5, wherein the bonding layer ~~(21)~~ is a layer of silicon nitride or of gallium nitride.
- [Claim 7] The Process according to one of Claims 1 to 6, wherein removing at least one portion of the bonding layer ~~(21)~~ comprises a chemical etch, a delamination by laser and/or the application of a mechanical stress.
- [Claim 8] The Process according to one of Claims 1 to 7, wherein the layer ~~(30)~~ of semi-insulating SiC is formed by doping with vanadium during the epitaxial growth of the SiC.

- [Claim 9] The Pprocess according to one of Claims 1 to 7, wherein the layer ~~(30)~~ of semi-insulating SiC is formed by simultaneously depositing silicon, carbon and vanadium.
- [Claim 10] The Pprocess according to one of Claims 1 to 9, wherein the second receiver substrate ~~(40)~~ is a silicon substrate having an electrical resistivity higher than or equal to 100 Ω .cm.
- [Claim 11] The Pprocess according to Claim 10, wherein the epitaxial layer ~~(30)~~ of semi-insulating SiC has a thickness comprised between 1 and 5 μ m.
- [Claim 12] The Pprocess according to one of Claims 1 to 9, wherein the second receiver substrate ~~(40)~~ is a polycrystalline SiC substrate or a polycrystalline AlN substrate having an electrical resistivity higher than or equal to 100 Ω .cm.
- [Claim 13] The Pprocess according to Claim 12, wherein the epitaxial layer ~~(30)~~ of semi-insulating SiC has a thickness smaller than or equal to 80 μ m.
- [Claim 14] The Pprocess according to one of Claims 1 to 13, further comprising a step of recycling the segment ~~(10')~~ of the donor substrate detached from the transferred layer ~~(11)~~, with a view to forming a new donor substrate.
- [Claim 15] The Pprocess according to one of Claims 1 to 14, wherein:
- the ionic species are implanted through the silicon face ~~(10-Si)~~ of the donor substrate ~~(10)~~,
 - the silicon face ~~(10-Si)~~ of the donor substrate ~~(10)~~ is bonded to the first receiver substrate ~~(20)~~,
- so that, after the transferred thin layer ~~(11)~~ of single-crystal SiC has been removed, the silicon face of the layer ~~(30)~~ of semi-insulating SiC is uncovered.
- [Claim 16] A Pprocess for fabricating by epitaxy a layer of gallium nitride, comprising:
- providing a substrate fabricated using the process according to one of Claims 1 to 15,
 - performing epitaxial growth of the layer ~~(50)~~ of gallium nitride on the layer ~~(30)~~ of semi-insulating SiC of said substrate.
- [Claim 17] The Pprocess according to Claim 16, wherein the layer ~~(50)~~ of gallium nitride has a thickness comprised between 1 and 2 μ m.
- [Claim 18] A Pprocess for fabricating a high-electron-mobility transistor (HEMT), comprising:
- fabricating by epitaxy a layer ~~(50)~~ of gallium nitride, of aluminium gallium nitride or of indium gallium nitride using the process according to either of Claims 16 and 17,
 - forming a heterojunction by epitaxy, on said layer ~~(50)~~, of a layer ~~(60)~~ of a III-N material different from the material of said layer ~~(50)~~,
 - forming a channel of the transistor level with said heterojunction,
 - forming a source, a drain and a gate of the transistor on the channel.