WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a channel structure on a substrate and extending in a first direction perpendicular to a top surface of the substrate, the channel structure comprising

a body gate layer extending in the first direction;

a charge storage structure surrounding a sidewall of the body gate layer; and

a channel layer surrounding a sidewall of the charge storage structure;

a plurality of gate electrodes on the substrate and spaced apart from one another in the first direction on a sidewall of the channel structure; and

a gate insulating layer between each of the plurality of gate electrodes and the channel structure,

wherein the channel layer includes a bottom portion in contact with the top surface of the substrate, and

an entirety of a bottom surface of the charge storage structure is covered by the channel layer so that the bottom surface of the charge storage structure is not in contact with the substrate.

2. The semiconductor device of claim 1, wherein

the charge storage structure is between the body gate layer and the channel layer, and

the charge storage structure is in contact with an inner wall of the channel layer.

3. The semiconductor device of claim 1 or claim 2, wherein

the channel layer is on an inner wall of a channel hole penetrating the plurality of gate electrodes and extending in the first direction,

the charge storage structure is conformally along the inner wall of the channel hole on the channel layer, and

the body gate layer fills in the channel hole on the charge storage structure.

4. The semiconductor device of any one of claims 1 to 3, wherein the charge storage structure comprises:

a blocking dielectric layer on the sidewall of the body gate layer,

a charge storage layer on the blocking dielectric layer, and

a tunneling dielectric layer on the charge storage layer and contacting the channel layer.

5. The semiconductor device of any one of claims 1 to 4, further comprising

a plurality of insulating layers, each between two adjacent gate electrodes of the plurality of gate electrodes,

wherein the gate insulating layer covers top and bottom surfaces of each of the plurality of gate electrodes, and

the plurality of insulating layers contact the sidewall of the channel structure.

6. The semiconductor device of any one of claims 1 to 4, further comprising

a plurality of insulating layers, each between two adjacent gate electrodes of the plurality of gate electrodes,

wherein the gate insulating layer is only between each of the plurality of gate electrodes and the channel structure, and

the plurality of insulating layers contact the sidewall of the channel structure.

7. The semiconductor device of any one of claims 1 to 4, further comprising

a plurality of insulating layers, each between two adjacent gate electrodes of the plurality of gate electrodes,

wherein the gate insulating layer extends in the first direction along an entire length of the sidewall of the channel structure, and

the plurality of insulating layers do not contact the sidewall of the channel structure.

8. The semiconductor device of claim 1, further comprising:

a bit line pad at a level higher than an uppermost gate electrode of the plurality of gate electrodes, the bit line pad on the channel layer, wherein an inner wall of the bit line pad defines an opening;

a bit line contact connected to the bit line pad; and

a body gate contact penetrating the opening and connected to the body gate layer.

9. The semiconductor device of claim 8, wherein

the opening vertically overlaps the body gate layer in a plan view, and

the inner wall of the bit line pad surrounds the body gate layer.

10. The semiconductor device of claim 8 or claim 9, further comprising:

a bit line connected to the bit line contact and extending in a second direction parallel to the top surface of the substrate; and

a body gate line connected to the body gate contact, the body gate line extending in the second direction.

11. The semiconductor device of any one of claims 1 to 10, wherein

a top surface of the body gate layer is at a same level as a top surface of the channel layer.

12. The semiconductor device of any one of claims 1 to 10, wherein

a top surface of the body gate layer is at a level lower than a top surface of the channel layer.

13. The semiconductor device of any one of claims 1 to 12, further comprising:

a conductive barrier layer between the body gate layer and the charge storage structure.

14. A semiconductor device comprising:

a plurality of gate electrodes on a substrate and spaced apart from one another in a first direction perpendicular to a top surface of the substrate;

a channel structure in a channel hole penetrating the plurality of gate electrodes and extending in the first direction, the channel structure comprising

a channel layer on an inner wall of the channel hole; and

a charge storage structure on the channel layer on the inner wall of the channel hole; and

a gate insulating layer between each of the plurality of gate electrodes and the channel layer, and the gate insulating layer covering a top surface and a bottom surface of each of the plurality of gate electrodes,

wherein the channel layer is between each of the plurality of gate electrodes and the charge storage structure.

15. The semiconductor device of claim 14, wherein

the channel structure further comprises a body gate layer filling an inside of the channel hole on the charge storage structure.

16. The semiconductor device of claim 15, further comprising:

a bit line pad at a level higher than an uppermost gate electrode of the plurality of gate electrodes and on the channel layer, wherein an inner wall of the bit line pad defines an opening;

a bit line contact connected to the bit line pad; and

a body gate contact penetrating the opening and connected to the body gate layer.

17. The semiconductor device of claim 16, further comprising:

a bit line connected to the bit line contact and extending in a second direction parallel to the top surface of the substrate; and

a body gate line connected to the body gate contact, the body gate line extending in the second direction.

18. The semiconductor device of any one of claims 15 to 17, wherein

the charge storage structure is between the body gate layer and the channel layer,

the channel layer includes a bottom portion in contact with the top surface of the substrate, and

an entirety of a bottom surface of the charge storage structure is covered by the channel layer, so that the bottom surface of the charge storage structure is not in contact with the substrate.

19. A semiconductor device comprising:

a channel structure on a substrate and extending in a first direction perpendicular to a top surface of the substrate; the channel structure comprising

a body gate layer extending in the first direction;

a charge storage structure surrounding a sidewall of the body gate layer; and

a channel layer surrounding a sidewall of the charge storage structure;

a plurality of gate electrodes on the substrate and spaced apart from one another in the first direction on a sidewall of the channel structure;

a gate insulating layer between each of the plurality of gate electrodes and the channel structure;

a bit line pad formed at a level higher than an uppermost gate electrode of the plurality of gate electrodes and on the channel layer;

a bit line contact connected to the bit line pad; and

a bit line connected to the bit line contact and extending in a second direction parallel to the top surface of the substrate,

wherein the channel layer includes a bottom portion in contact with the top surface of the substrate, and

an entirety of a bottom surface of the charge storage structure is covered by the channel layer so that the bottom surface of the charge storage structure is not in contact with the substrate.