METALLIC CARRIER FOR LAYER TRANSFER AND METHODS FOR FORMING THE SAME

FIELD

[0001] The present invention generally relates to the fabrication of engineered substrates for use in the fabrication of semiconductor structures or devices, intermediate structures formed during the fabrication of semiconductor structures or devices, and to semiconductor structures or devices using engineered substrates.

BACKGROUND

[0002] Substrates that include one or more layers of semiconductor material are used to form a wide variety of semiconductor structures and devices including, for example, integrated circuit (IC) devices (e.g., logic processors and memory devices) and discrete devices such as, radiation emitting devices (e.g., light emitting diodes (LEDs), resonant cavity light emitting diodes (RCLEDs), vertical cavity surface emitting lasers (VCSELs)), and radiation sensing devices (e.g., optical sensors). Such semiconductor devices are conventionally formed in a layer-by-layer manner (i.e., lithographically) on and/or in a surface of a semiconductor substrate.

[0003] Historically, a majority of such semiconductor substrates that have been used in the semiconductor device manufacturing industry have comprised thin discs or "wafers" of silicon material. Such wafers of silicon material are fabricated by first forming a large generally cylindrical silicon single crystal ingot and subsequently slicing the single crystal ingot perpendicularly to its longitudinal axis to form a plurality of silicon wafers. Such silicon wafers may have diameters as large as about thirty centimeters (30 cm) or more (about twelve inches (12 in) or more). Although silicon wafers generally have thicknesses of several hundred microns (e.g., about 700 microns) or more, only a very thin layer (e.g., less than about three hundred nanometers (300 nm)) of the semiconductor material on a major surface of the silicon wafer is generally used to form active devices on the silicon wafer. However, in some device applications the majority of the silicon wafer thickness may be included in the electrical path-way of one or more device structures formed from the silicon wafer, such device structures being commonly referred to as "vertical" device structures.

[0004] So-called "engineered substrates" have been developed that include a relatively thin layer of semiconductor material (e.g., a layer having a thickness of less than about three hundred nanometers (300 nm)) disposed on a layer of dielectric material (e.g., silicon dioxide (SiO_2), silicon nitride (Si_3N_4), or aluminum oxide (Al_2O_3)). Optionally, the layer of dielectric material may be relatively thin (e.g., too thin to enable handling by conventional semiconductor device manufacturing equipment), and the semiconductor material and the layer of dielectric material may be disposed on a relatively thicker host or base substrate to facilitate handling of the overall engineered substrate by manufacturing equipment. As a result, the base substrate is often referred to in the art as a "handle" or "handling" substrate. The base substrate may also comprise a semiconductor material other than silicon.

[0005] A wide variety of engineered substrates are known in the art and may include semiconductor materials such as, for example, silicon (Si), germanium (Ge), III-V type semiconductor materials, and II-VI type semiconductor materials.

[0006] For example, an engineered substrate may include an epitaxial layer of III-V type semiconductor material formed on a surface of a base substrate, such as, for example aluminum oxide (Al_2O_3) (which may be referred to as "sapphire"). The epitaxial layer may be formed on the surface of the base substrate by a transfer process from a donor structure, for example a donor substrate or donor ingot. The transfer from a donor structure may be desirable when the donor material is highly valuable or in scarce supply. Using such an engineered substrate, additional layers of material may be formed and processed (e.g., patterned) over the epitaxial layer of III-V type semiconductor material to form one or more devices on the engineered substrate. However, the coefficient of thermal expansion mismatch (or difference) between the epitaxial layer and the base substrate comprising the engineered substrate, may influence the formation and processing of the additional layers of material. For example, if the coefficient of thermal expansion mismatch between the epitaxial layer and the base substrate is substantial then the engineered substrate may be negatively impacted during the formation of additional layers of materials.

[0007] Examples of devices that can take advantage of engineered substrates are high power devices and photonic devices, such as, Light Emitting Diodes (LEDs) and laser diodes. FIG. 1 illustrates a conventional LED. A substrate 110, which may be an engineered substrate, includes an n-type layer 120 disposed thereon. An active region 130, which may include multiple layers, such as, for example, quantum wells, barrier layers, electron blocking layer(s) (EBL) etc., is

disposed between the n-type layer 120 and a p-type layer 140. The result is an LED formed by the n-type layer 120, the active region 130, and the p-type layer 140. A first contact 160 provides an electrical connection to the n-type layer 120 and a second contact 150 provides another electrical connection to the to the p-type layer 140. These contacts may be opaque to the wavelength of light emitted by the LED and, as a result, may diminish the overall amount of light available from the LED. Thus, only the area between the first contact 160 and the second contact 150 may produce significant amounts of light. The physical layout of the second contact 150 relative to the n-type layer 120 may cause current crowding in the current flowing between the p-type layer 140 and the n-type layer 120. In addition, the physical layout may require that both p and n-type contacts are disposed on an upper surface of the LED structure, wherein such a physical layout may require removal of a portion of the device layers to expose regions for contacting. The removal of a portion of the device layers may increase the complexity of device fabrication, may reduce the area available for light generation and may also decrease device yield.

[0008] In view of the above, and for other reasons discussed below, there is a need for a substrate technology that provides a suitable base substrate for donated material from a donor structure. Moreover, there is a need for devices and methods that provide a support substrate with a closely matching Coefficient of Thermal Expansion (CTE) with that of an engineered substrate.

BRIEF SUMMARY

[0009] The various embodiments of the present invention generally relate to engineered substrates and methods of producing the engineered substrates that provide a suitable base substrate with a CTE that closely matches a CTE of the engineered substrate.

[0010] This summary is provided to introduce a selection of concepts in a simplified form that are further described in the detailed description below of some example embodiments of the invention. This summary is not intended to identify key features or essential features of the claimed subject matter, nor is it intended to be used to limit the scope of the claimed subject matter.

[0011] In some embodiments, the present invention includes methods of fabricating a semiconductor substrate, the methods include forming a weakened zone in a donor structure at a predetermined depth to define a transfer layer between an attachment surface and the weakened zone and a residual donor structure between the weakened zone and a surface opposite the attachment surface. A metallic layer is formed on the attachment surface and provides a matched

Coefficient of Thermal Expansion (CTE) for the metallic layer that closely matches a CTE of the transfer layer, and sufficient stiffness to provide structural support to the transfer layer. The transfer layer is separated from the donor structure at the weakened zone to form a composite substrate comprising the transfer layer and the metallic layer.

[0012] In additional embodiments, the present invention includes methods of fabricating a semiconductor substrate, the methods include forming a weakened zone in a donor structure at a predetermined depth to define a transfer layer between an attachment surface and the weakened zone and a residual donor structure between the weakened zone and a surface opposite the attachment surface. An ohmic contact is formed between the transfer layer and a contact layer disposed thereon. A low impedance coupling is formed between a refractory metal layer and the contact layer, wherein the refractory metal layer provides a structural support for the semiconductor substrate. The methods also include separating the transfer layer from the donor structure at the weakened zone to form a composite substrate comprising the transfer layer the contact layer, and the refractory metal layer.

[0013] In other embodiments, the present invention comprises a semiconductor substrate including a metallic support substrate configured to provide a sufficient stiffness to the semiconductor substrate. The semiconductor substrate also includes a transfer layer comprising a semiconductor material in contact with an attachment surface of the metallic support substrate, wherein the transfer layer is detached from a donor structure comprising the semiconductor material and including a weakened zone in the donor structure at a predetermined depth from the attachment surface to define the transfer layer between the attachment surface and the weakened zone. A matched CTE of the metallic support substrate closely matches a CTE of the transfer layer.

[0014] Further aspects, details, and alternate combinations of the elements of embodiments of the invention will be apparent from the following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The present invention may be understood more fully by reference to the following detailed description of example embodiments of the present invention, which are illustrated in the appended figures in which:

[0016] FIG. 1 is a simplified cross-section drawing of a conventional LED structure;

[0017] FIG. 2 is a simplified cross-section drawing of a donor structure with a weakened zone to create a transfer layer;

[0018] FIGS. 3A-3B are simplified cross-section drawings illustrating development of a composite substrate with a refractory metal carrier and a transfer layer according to one or more embodiments of the invention;

[0019] FIGS. 4A-4C are simplified cross-section drawings illustrating development of a composite substrate with a refractory metal carrier, a transfer layer, and a contact layer therebetween according to one or more embodiments of the invention;

[0020] FIGS. 5A-5C illustrate a composite substrate with an n-doped Gallium Nitride (GaN) transfer layer and a photonic device formed on the composite substrate according to one or more embodiments of the invention;

[0021] FIGS. 6A-6C illustrate a composite substrate with a p-doped Gallium Nitride (GaN) transfer layer and a photonic device formed on the composite substrate according to one or more embodiments of the invention;

[0022] FIGS. 7A-7C illustrate a composite substrate with Silicon Carbide (SiC) transfer layer and a high power electronic device formed on the composite substrate according to one or more embodiments of the invention; and

[0023] FIGS. 8A-8D illustrate a composite substrate with an n-doped Gallium Nitride (GaN) transfer layer and a photonic device formed on the composite substrate, which is flipped to form a n-layer up photonic device according to one or more embodiments of the invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0024] The illustrations presented herein are not meant to be actual views of any particular material, device, or method, but are merely idealized representations which are employed to describe embodiments of the present invention.

[0025] It should be understood that any reference to an element herein using a designation such as "first," "second," and so forth does not limit the quantity or order of those elements, unless such limitation is explicitly stated. Rather, these designations may be used herein as a convenient method of distinguishing between two or more elements or instances of an element. Thus, a reference to first and second elements does not mean that only two elements may be employed there

or that the first element must precede the second element in some manner. Also, unless stated otherwise a set of elements may comprise one or more elements.

[0026] Elements described herein may include multiple instances of the same element. These elements may be generically indicated by a numerical designator (e.g. 110) and specifically indicated by the numerical indicator followed by an alphabetic designator (e.g., 110A) or a numeric indicator preceded by a "dash" (e.g., 110-1). For ease of following the description, for the most part, element number indicators begin with the number of the drawing on which the elements are introduced or most fully discussed. Thus, for example, element identifiers on a FIG. 1 will be mostly in the numerical format 1xx and elements on a FIG. 4 will be mostly in the numerical format 4xx.

[0027] The following description provides specific details, such as material types and processing conditions, in order to provide a thorough description of embodiments of the present disclosure and implementation thereof. However, a person of ordinary skill in the art will understand that the embodiments of the present disclosure may be practiced without employing these specific details and in conjunction with conventional fabrication techniques. In addition, the description provided herein does not form a complete process flow for manufacturing a semiconductor device or system. Only those process acts and structures necessary to understand the embodiments of the present invention are described in detail herein. The materials described herein may be formed (e.g., deposited or grown) by any suitable technique including, but not limited to, spin-coating, blanket coating, Bridgeman and Czochralski processes, chemical vapor deposition ("CVD"), plasma enhanced chemical vapor deposition ("PECVD"), atomic layer deposition ("ALD"), plasma enhanced ALD, or physical vapor deposition ("PVD"). While the materials described and illustrated herein may be formed as layers, the materials are not limited to layers and may be formed in other three-dimensional configurations.

[0028] Terms such as "horizontal" and "vertical," as used herein, define relative positions of elements or structures with respect to a major plane or surface of a semiconductor structure (e.g., wafer, die, substrate, etc.), regardless of the orientation of the semiconductor structure, and are orthogonal dimensions interpreted with respect to the orientation of the structure being described. As used herein, the term "vertical" means and includes a dimension substantially perpendicular to the major surface of a semiconductor structure, and the term "horizontal" means a dimension substantially parallel to the major surface of the semiconductor structure.

[0029] As used herein, the term "semiconductor structure" means and includes any structure that is used in the formation of a semiconductor device. Semiconductor structures include, for example, dies and wafers (e.g., carrier substrates and device substrates), as well as assemblies or composite structures that include two or more dies and/or wafers three-dimensionally integrated with one another. Semiconductor structures also include fully fabricated semiconductor devices, as well as intermediate structures formed during fabrication of semiconductor devices. Semiconductor structures may comprise conductive materials, semiconductive materials, non-conductive materials (e.g., electrical insulators), and combinations thereof.

[0030] As used herein, the term "processed semiconductor structure" means and includes any semiconductor structure that includes one or more at least partially formed device structures. Processed semiconductor structures are a subset of semiconductor structures, and all processed semiconductor structures are semiconductor structures.

[0031] As used herein, the term "III-V semiconductor" means and includes any semiconductor material that is at least predominantly comprised of one or more elements from group IIIA of the periodic table (e.g., B, Al, Ga, In, and Ti) and one or more elements from group VA of the periodic table (e.g., N, P, As, Sb, and Bi).

[0032] Unless specified differently, as used herein, the term "coefficient of thermal expansion," when used with respect to a material or structure, means the average linear coefficient of thermal expansion of the material or structure at room temperature.

[0033] As used herein, the term "engineered substrate," in its broadest sense, means and includes any substrate comprising two or more layers of material and that is intended to be used as a substrate for the fabrication of one or more semiconductor devices thereon. Engineered substrates include, as non-limiting examples, semiconductor-on-insulator type substrates.

[0034] As used herein, the term "sufficient stiffness" means a stiffness for a semiconductor structure that provides enough stiffness that structural damage due to plastic or elastic deformation does not occur to the semiconductor structure during subsequent processing or handling. As non-limiting examples, such structural damage may include, dislocations, cracking, crystal lattice damage, warp, bow and layer separation.

[0035] The various embodiments of the present invention are concerned with engineered substrates and methods of producing the engineered substrates that provide a suitable base substrate with a CTE that closely matches a CTE of the engineered substrate

[0036] Embodiments of the invention may have applications to a wide range of silicon, germanium, silicon carbide, and III-V semiconductor materials as substrates. For example, the methods and structures of the embodiments of the invention may be applied to III-Nitrides, III-arsenides, III-phosphides and III-antimonides, in binary, ternary, quaternary and quinary form.

[0037] FIG. 2 is a simplified cross-section drawing of a donor structure 210 with a weakened zone 220 to create a transfer layer 230. As non-limiting examples, a detachment process described herein may use a SMART-CUT™ technology. Such processes are described in detail in, for example, U.S. Patent No. RE39,484 to Bruel, U.S. Patent No. 6,303,468 to Aspar et al.,

[0038] U.S. Patent No. 6,335,258 to Aspar et al., U.S. Patent No. 6,756,286 to Moriceau et al., U.S. Patent No. 6,809,044 to Aspar et al., U.S. Patent No. 6,946,365 to Aspar et al., U.S. Patent No. 7,531,428 to Dupont, U.S. Patent No. 6,858,107 to Ghyselen et al., and U.S. Patent No. 6,867,067 to Ghyselen et al, the disclosures of each of which are incorporated herein in their entirety by this reference. However, it should be understood that other processes suitable for manufacturing a compound material wafer that include utilizing predetermined weakened areas could also be used.

[0039] To perform this detachment process, a predetermined weakened zone 220 may be formed in the donor structure 210. FIG. 2 shows use of the SMART-CUT™ technology wherein atomic species 250, such as one or more of hydrogen ions, helium ions or other inert gas ions, are implanted through an attachment surface 240 with a dose and energy to create the weakened zone 220 in the donor structure 130. The weakened zone 220 is substantially parallel to the main attachment surface 240 and at a predetermined depth based on parameters of the atomic species implant process.

[0040] The transfer layer 230 is thus formed between the attachment surface 240 and the weakened zone 220. In addition, a residual donor structure is formed between the weakened zone 220 and an opposite surface from the attachment surface 240.

[0041] The donor structure 210 includes a semiconductor material and in some embodiments may include silicon, germanium, III-nitride (e.g., GaN, InGaN, AlGaN), and SiC. The semiconductor material may be un-doped or, for some applications, doped n+ or p+. The semiconductor may be a freestanding wafer as shown in Fig. 2 or a template structure, e.g., GaN on a sapphire base. The donor structure 210 may also comprise at least a portion of an ingot (or boule) of semiconductor material and in some embodiments the at least a portion of the ingot (or boule)

may include silicon, germanium, III-nitride (e.g., GaN, InGaN, AlGaN), and SiC. The ingot (or boule) may comprise a structure such as those described in U.S. Patent No. 6,858,107 to Ghyselen et al., and U.S. Patent No. 6,867,067 to Ghyselen et al, the disclosures of each of which are incorporated herein in their entirety by this reference.

[0042] If the donor structure 210 is a III-nitride material, the polarity of the surface being implanted should be considered in determining the polarity of the final composite substrate. As a non-limiting example, a GaN donor structure may be used to develop a Gallium-polar face or a Nitrogen-polar face for subsequent processing. As a further non-limiting example, an InGaN donor structure may be used to develop a metal-polar face or a Nitrogen-polar face for subsequent processing.

[0043] For conventional layer transfer to a carrier wafer, typically a bonding process is used followed by splitting off of the implanted wafer by means of some heat treatment. The bonding process requires a high quality of the surfaces to be bonded to avoid large area defects (non-transferred areas) while the Coefficient of Thermal Expansion (CTE) of both wafers should not be too different to avoid wafer breakage as a result of the splitting process. For some applications, conductive bonding of a semiconductor material to a conductive substrate is desirable to construct vertical device structures, i.e., devices that have the active area near the surface of the semiconductor layer and a contact area near the interface of the semiconductor with the substrate or carrier wafer.

[0044] However, such an approach is difficult to realize as today most bonding processes involve layers of Silicon Dioxide (SiO_2) on the bonding faces to ensure a high quality bond. However, SiO_2 is an insulator and will make electrical conduction difficult, if not impossible and, in addition, impede efficient heat dissipation of the device to the substrate.

[0045] As a result, embodiments of the present invention provide structures and processes for providing a support structure that may provide heat dissipation and with a CTE that closely matches a CTE of the transfer layer 230. In some embodiments, an electrical contact may be developed, for example, an ohmic or Schottky contact, between the transfer layer 230 and a metallic carrier layer. An ohmic contact (i.e., a contact with a voltage independent resistance) is developed at a metal-semiconductor junction if the Schottky barrier height, is zero or negative. In other words, an ohmic contact will have current versus voltage characteristics

that are substantially linear and symmetric. In such cases, the carriers are free to flow in or out of the semiconductor so that there is a minimal resistance across the ohmic contact.

[0046] FIGS. 3A-3B are simplified cross-section drawings illustrating development of a composite substrate with a refractory metal layer 280 and a transfer layer 230 according to one or more embodiments of the invention. The refractory metal layer 310 may be formed to a thickness sufficient to form a metallic support substrate with sufficient stiffness to provide structural support to the transfer layer 230.

[0047] The refractory metal layer 310 is formed on the attachment surface 240 with a process suitable for providing an electrical contact, for example ohmic contact, between the refractory metal layer 310 and the transfer layer 230. Prior to depositing the refractory metal layer 310, the surface of the semiconductor may need treatment to remove any surface oxide or other surface layers which may impact the quality of the refractory metal layer 310, e.g., a thin gallium oxide layer may need to be removed prior to depositing the refractory metal layer 310 and for the formation of an electrical contact, e.g., an ohmic contact.

[0048] The entire structure of the donor structure 210 and the metallic support substrate 310 may be placed into a furnace (not shown) and heated so that the weakened zone 220 may be further weakened. With the weakening, the transfer layer 230 and accompanying metallic support substrate 310 may be separated from the donor structure at the weakened zone 220. Instead of providing thermal energy, additional energy in other forms, for example, mechanical energy, chemical energy, or a combination of thermal, mechanical energy, and chemical energies could be used during the weakening and detachment acts.

[0049] The structures thus formed after the separation are a residual donor structure (not shown) capable of donating further thin transfer layers and a composite substrate 450 including the metallic support substrate 310 and the transfer layer 230. As non-limiting examples, the transfer layer 230 may have a thickness of less than 1000 nanometers and more likely a thickness of about 500 nanometers.

[0050] As shown in FIG. 3B, the composite substrate 450 may be flipped over for additional processing on the exposed surface of the transfer layer 230. Prior to performing any further processing steps, the composite substrate 450 may receive a surface treatment, such as, for example, polishing, cleaning, or combination thereof. Additional processing may include, as a non-limiting example, adding device structures on the composite structure. The device structures may

include multiple layers of doped semiconductor material, un-doped semiconductor material, and active areas as are known in the art to produce electronic elements, photonic elements, and combinations thereof.

[0051] FIGS. 4A-4C are simplified cross-section drawings illustrating development of a composite substrate 450 with a refractory metal layer 310, a transfer layer 230, and a contact layer 410 therebetween according to one or more embodiments of the invention.

[0052] In the embodiments of FIGS. 4A-4C, a contact layer 410 of metal is deposited on the attachment surface 240. This contact layer 410 is configured to provide an ohmic contact that is high quality (e.g., low resistance) between the transfer layer 230 and the contact layer 410. As a non-limiting example, if the donor material is n+ doped GaN than the contact metal layer may be e.g., a Ti/Al/Ni/Au stack or a Ti/Al stack when the use of gold may be detrimental to the device performance. As another non-limiting example, if the donor material is p+ doped GaN then the contact metal layer may be e.g., Ni/Au stack or Ni (the first metal in the list being closest to the semiconductor). Prior to depositing the contact layer 410, the surface of the semiconductor may need treatment to remove any surface oxide or other surface layers which may impact the quality of the contact layer 410, e.g., a thin gallium oxide layer may need to be remove prior to depositing the contact layer 410. The contact layer 410 may be deposited by sputter coating, thermal evaporation, e-beam evaporation, etc. In some embodiments, the contact layer 410 may also function as a seed metal for subsequent deposition of a thick metal support, such a seed may be improve adhesion with the transfer layer 230 and improve electrical conduction properties with the transfer layer 230.

[0053] The contact layer 410 may be as thin as a few monolayers. In some embodiments, the contact layer 410 may have a thickness of about one nanometer to about 50 nanometers.

[0054] As shown in FIG. 4B, a refractory metal layer 310 is formed on the contact layer 410 with a process suitable for providing a low impedance coupling between the refractory metal layer 310 and the contact layer 410. In the embodiments of FIGS. 4A-4C, the combination of the contact layer 410 and the refractory metal layer 310 may be referred to herein as a metallic support substrate 310A.

[0055] The entire structure of the donor structure 210 and the metallic support substrate 310A may be placed into a furnace (not shown) and heated so that the weakened zone 220 may be further weakened. With the weakening, the transfer layer 230 and accompanying metallic support substrate 310A may be separated from the donor structure at the weakened zone 220. Instead of

providing thermal energy, additional energy in other forms, for example, mechanical energy, chemical energy, or a combination of thermal, mechanical energy, and chemical energies could be used during the weakening and detachment steps.

[0056] The structures thus formed after the separation are a residual donor structure (not shown) capable of donating further thin transfer layers and a composite substrate 450 including the refractory metal layer 310, the contact layer 410, and the transfer layer 230. As non-limiting examples, the transfer layer 230 may have a thickness of less than 1000 nanometers and more likely a thickness of about 500 nanometers.

[0057] As shown in FIG. 4C, the composite substrate 450 may be flipped over for additional processing on the exposed surface of the transfer layer 230. Prior to performing any further processing steps, the composite substrate 450 may receive a surface treatment, such as, for example, polishing, cleaning, or combination thereof. Additional processing may include, as a non-limiting example, adding device structures on the composite structure. The device structures may include multiple layers of doped semiconductor material, un-doped semiconductor material, and active areas as are known in the art to produce electronic elements, photonic elements, and combinations thereof.

[0058] The residual donor structure may be re-used for forming additional composite structures by repeating the process as illustrated in FIG. 2 and FIGS. 3A and 3B or in FIG. 2 and FIGS. 4A and 4C. Prior to performing any further processing steps, the residual donor structure may need to receive a surface treatment, such as, for example, polishing, cleaning, or combination thereof in order to restore the original surface quality.

[0059] In both the embodiments of FIGS. 3A-3B and FIGS. 4A-4C, the refractory metal layer 310 should be able to remain chemically and physically stable at temperatures high enough for subsequent processing, such as, for example, the heating for the separation and growth/deposition/processing of additional layers. As a non-limiting example, for subsequent processing of addition GaN layers, the refractory metal layer 310 should be able to withstand temperatures in the range of about 900 °C to about 1100 °C. In addition, for subsequent processing the refractory metal layer 310 should be able to withstand the chemical environment within the additional growth/deposition/processing equipment.

[0060] The refractory metal layer 310 may be thick enough to provide sufficient stiffness to provide structural support to the transfer layer 230. As non-limiting examples, the refractory

metal layer 310 may have a thickness between about 10 microns and about 150 microns and more likely a thickness between about 10 microns and about 20 microns. As non-limiting examples, the refractory metal layer 310 may be deposited by sputter coating, plasma spray coating or plating methods (e.g., electroless plating and electroplating).

[0061] The refractory metal layer 310 may have a matched CTE that closely matches a CTE of the transfer layer 230, for example to prevent strain and cracking during subsequent growth processes. Table 1 lists CTE values for some non-limiting materials for the transfer layer 230 and the refractory metal layer 310.

Material	CTE (10^{-6} /°K)
GaN	5.6
SiC	4.5
Tungsten	4.5
Molybdenum	5.4
Hafnium	6.1
Rhenium	6.2
Tantalum	6.5
Zirconium	5.9

TABLE 1

[0062] In some embodiments, the CTE of the refractory metal layer 310 may be within about **20% of the CTE, or within about 10% of the CTE** of the semiconductor material of the transfer layer 230. Thus, for these embodiments tungsten, molybdenum, and zirconium used as the refractory metal layer 310 would closely match a SiC transfer layer 230 and in some embodiments particularly tungsten. Similarly, for these embodiments zirconium, hafnium, rhenium, and tantalum used as the refractory metal layer 310 would closely match a GaN transfer layer 230 and in some embodiments particularly molybdenum.

[0063] Since the stack of semiconductor/metal is CTE matched, thick epilayers of semiconductor material may be grown on the stack without cracking in order to complete the fabrication of a device structure. If needed, a thick metal wafer of the same kind as the

sputtered/evaporated metal layer may serve as a carrier to add stiffness to the stack without losing its advantageous properties.

[0064] FIGS. 5A-5C illustrate a composite substrate 450N with an n-doped Gallium Nitride (GaN) transfer layer 230N and a photonic device formed on the composite substrate 450N according to one or more embodiments of the invention.

[0065] In FIG. 5A, the composite substrate 450N includes a transfer layer 230N of an n-doped GaN layer that is Ga polar on a Ti/Al/Ni/Au contact layer 410 on a refractory metal layer 310 (e.g., Molybdenum). The transfer layer 230 may be provided from either an n+GaN bulk or n+GaN (Ga polar) on sapphire template. Transfer from the n+GaN bulk may be effected with ion implantation into the n-face polar bulk. Deposition of the contact layer 410 and refractory metal layer 310 are followed by transfer layer separation of the transfer layer 230 from the bulk. Transfer for the n+GaN on sapphire would be effected with a double transfer to provide a Ga polar n+-GaN layer on the composite substrate.

[0066] FIG. 5B illustrates an LED structure, as a type of photonic device, comprised of additional semiconductor device on the composite substrate 450N. The LED structure includes an active region, which may include multiple layers, such as, for example, quantum wells disposed on the n-doped GaN transfer layer 230N. One or more p-type layers 520 are disposed on the active layer 510. The result is an LED formed by the n-doped GaN transfer layer 230N, the active layer 510, and the p-type layer 520. A contact layer 530 provides an electrical connection to the p-type layer 520.

[0067] The resulting LED structure provides a vertical diode structure, which, in contrast to the diode structure in FIG. 1, does not need an additional electrical connection exposed on the top layers for connection to the n-side of the diode.

[0068] FIG. 5C illustrates an optional further act to include a thick metal substrate 550. The supporting metal thickness can be increased by metal to metal bonding between the deposited refractory metal layer 310 and the thick metal substrate 550, this thickening of the metal support may be performed prior to device layer formation if the thick metal substrate 550 is capable of withstanding the corrosive reactor growth conditions.

[0069] FIGS. 6A-6C illustrate a composite substrate 450P with a p-doped Gallium Nitride (GaN) transfer layer 230P and a photonic device formed on the composite substrate 450P according to one or more embodiments of the invention.

[0070] The layers in the embodiments of FIGS. 6A-6C are similar to those of the embodiments of FIGS. 5A-5C except the transfer layer 230 comprises a p-doped GaN transfer layer 230P. A corresponding contact layer 410 may be, for example, Ni/Au.

[0071] FIG. 6B illustrates an LED structure as a photonic device that includes an active region, which may include multiple layers, such as, for example, quantum wells disposed on the p-doped GaN transfer layer 230P. One or more n-type layers 620 are disposed on the active layer 610. The result is an LED formed by the p-doped GaN transfer layer 230P, the active layer 610, and the n-type layer 620. A contact layer 630 provides an electrical connection to the n-type layer 620.

[0072] The resulting LED structure provides a vertical diode structure, which, in contrast to the diode structure in FIG. 1, does not need an additional electrical connection exposed on the top layers for connection to the p-side of the diode.

[0073] FIG. 6C illustrates an optional further act to include a thick metal substrate 650. The supporting metal thickness can be increased by metal to metal bonding between the deposited refractory metal layer 310 and the thick metal substrate 650, this thickening of the metal support may be performed prior to device layer formation if the thick metal substrate 650 is capable of withstanding the corrosive reactor growth conditions.

[0074] FIGS. 7A-7C illustrate a composite substrate 450S with a Silicon Carbide (SiC) transfer layer 230S and a high power electronic device formed on the composite substrate 450S according to one or more embodiments of the invention. The composite substrate 450S includes the SiC transfer layer 230S on the refractory metal layer 310, e.g., Tungsten 310T. As seen from Table 1, the SiC transfer layer 230 and the Tungsten refractory metal layer 310T are matched in CTE such that the SiC transfer layer 230 and high power electronic device formed thereon will experience little or no strain effects due to a CTE mismatch during device formation.

[0075] As illustrated in FIG. 7B, a power device may be formed with one or more power device layers 710 on the SiC transfer layer 230S. A contact layer 730 provides an electrical connection to the power device layer 710.

[0076] FIG. 7C illustrates an optional further act to include a thick metal substrate 750. The supporting metal thickness can be increased by metal to metal bonding between the deposited refractory metal layer 310 and the thick metal substrate 750, this thickening of the metal support may be performed prior to device layer formation if the thick metal substrate 750 is capable of withstanding the corrosive reactor growth conditions.

[0077] FIGS. 8A-8D illustrate a composite substrate with an n-doped Gallium Nitride (GaN) transfer layer 230 and a photonic device formed on the composite substrate 450, which is flipped to form a n-layer up photonic device according to one or more embodiments of the invention.

[0078] The layers in the embodiment of FIG. 8A are similar to those of the embodiments of FIG. 3B. However, in contrast to the embodiments of FIGS. 4A-6C, the embodiments of FIGS. 8A-8D do not include a contact layer adjacent the composite substrate 450. Rather, a photonic device, such as, for example, an LED may be formed on the semiconductor material 230, which formed as an n-doped Gallium Nitride (GaN) transfer layer 230N in this embodiment.

[0079] As shown in FIG. 8B, the photonic device may includes an active region 810, which may include multiple layers, such as, for example, quantum wells disposed on the n-type Gallium Nitride (GaN) transfer layer 230N. One or more p-type GaN layers 820 may be disposed on the active layer 810. The result is an LED formed by the the n-type Gallium Nitride (GaN) transfer layer 230N, the active layer 810, and the p-type layer 820.

[0080] With the photonic device structure formed, a contact layer 840, such as those described above may be formed on the p-type GaN layer 820 providing an electrical connection to the p-type layer 820. A heat sink, such as, for example, a thick metal substrate 850 may be formed on the contact layer 810. The resulting structure may be thought of as flipped. The flipped configuration is illustrated in FIG. 8C. The refractory metal 310 may then be removed to expose the the n-type Gallium Nitride (GaN) transfer layer 230N.

[0081] The resulting LED structure provides a vertical diode structure, which, in contrast to the diode structure in FIG. 1, does not need an additional electrical connection exposed on the top layers for connection to the p-side of the diode. Rather, the p-side of the diode may be contacted through the contact layer 840 and the thick metal substrate 850. A contact layer 850 may be formed to provide an electrical connection to an n-doped Gallium Nitride (GaN) transfer layer 230N.

[0082] The embodiments of the invention described above do not limit the scope the invention, since these embodiments are merely examples of embodiments of the invention, which is defined by the scope of the appended claims and their legal equivalents. Any equivalent embodiments are intended to be within the scope of this invention. Indeed, various modifications of the invention, in addition to those shown and described herein, such as alternate useful combinations of the elements described, will become apparent to those skilled in the art from the description. Such modifications are also intended to fall within the scope of the appended claims.

CLAIMS

What is claimed is:

1. A method of fabricating a semiconductor substrate, comprising:

forming a weakened zone in a donor structure at a predetermined depth to define a transfer layer between an attachment surface and the weakened zone and a residual donor structure between the weakened zone and a surface opposite the attachment surface;

forming a metallic layer on the attachment surface wherein the metallic layer provides:

a matched Coefficient of Thermal Expansion (CTE) for the metallic layer that closely matches a CTE of the transfer layer; and

sufficient stiffness to provide structural support to the transfer layer; and

separating the transfer layer from the donor structure at the weakened zone to form a composite substrate comprising the transfer layer and the metallic layer.

2. The method of claim 1, wherein forming the metallic layer on the attachment surface further comprises forming the metallic layer to provide an ohmic contact between the metallic layer and the transfer layer.

3. The method of claim 1, wherein forming the metallic layer on the attachment surface further comprises forming the metallic layer to provide a Schottky contact between the metallic layer and the transfer layer.

4. The method of any one of the preceding claims, wherein forming the weakened zone in the donor structure comprises forming the weakened zone in at least a portion of an ingot of semiconductor material or a boule of semiconductor material.

5. The method of claim 1, further comprising forming the metallic layer by:

forming a contact layer on the attachment surface wherein the contact layer provides an electrical contact with the transfer layer; and

forming a refractory metal layer conductively coupled with and on the contact layer, wherein the refractory metal layer is relatively thick compared to the contact layer, provides the sufficient stiffness, and provides the matched CTE.

6. The method of any one of the preceding claims, wherein the matched CTE is within 10% of the CTE of the transfer layer.

7. The method of any one of the preceding claims, further comprising selecting the donor structure from the group consisting of silicon, germanium, SiC, GaN, AlN, InGaN and GaAs.

8. The method of any one of claims 1 to 6, further comprising selecting the donor structure to include SiC and selecting the metallic layer to include tungsten or molybdenum.

9. The method of any one of claims 1 to 6, further comprising selecting the donor structure to include GaN and selecting the metallic layer to include molybdenum, zirconium, hafnium, rhenium, or tantalum.

10. The method of any one of the preceding claims, further comprising forming additional semiconductor structures within the transfer layer, on the transfer layer, or a combination thereof.

11. A semiconductor substrate, comprising:

a metallic support substrate configured to provide a sufficient stiffness to the semiconductor substrate; and

a transfer layer comprising a semiconductor material in contact with an attachment surface of the metallic support substrate, wherein the transfer layer is detached from a donor structure comprising the semiconductor material and including a weakened zone in the donor structure at a predetermined depth from the attachment surface to define the transfer layer between the attachment surface and the weakened zone;

wherein a matched Coefficient of Thermal Expansion (CTE) of the metallic support substrate closely matches a CTE of the transfer layer.

12. The semiconductor substrate of claim 11, wherein the metallic support substrate comprises:

a contact layer adjacent the attachment surface and providing a conductive contact with the transfer layer; and

a refractory metal layer conductively coupled with and adjacent the contact layer, wherein the refractory metal layer provides the sufficient stiffness to provide structural support for the semiconductor substrate and provides the matched CTE.

13. The semiconductor substrate of claim 12, wherein the conductive contact comprises an ohmic contact.

14. The semiconductor substrate of claim 12, wherein the matched CTE is within 20% of the CTE of the transfer layer.

15. The semiconductor substrate of any one of claims 12 to 14, wherein the transfer layer comprises SiC and the refractory metal layer includes at least one of tungsten, molybdenum, and zirconium.

16. The semiconductor substrate of any one of claims 12 to 14, wherein the transfer layer comprises GaN and the refractory metal layer includes at least one of zirconium, hafnium, rhenium, and tantalum.

17. The semiconductor substrate of any one of claims 12 to 16, further comprising a thick metal substrate conductively coupled with and adjacent the refractory metal layer.

18. The semiconductor substrate of any one of claims 11 to 14, wherein the transfer layer comprises n-doped GaN and further comprising semiconductor device layers integrated on the transfer layer to form at least one photonic element.

19. The semiconductor substrate of any one of claims 11 to 14, wherein the transfer layer comprises p-doped GaN and further comprising semiconductor device layers integrated on the transfer layer to form at least one photonic element.

20. The semiconductor substrate of any one of claims 11 to 14, wherein the transfer layer comprises SiC and further comprising semiconductor device layers integrated on the transfer layer to form at least one high power electronic device.