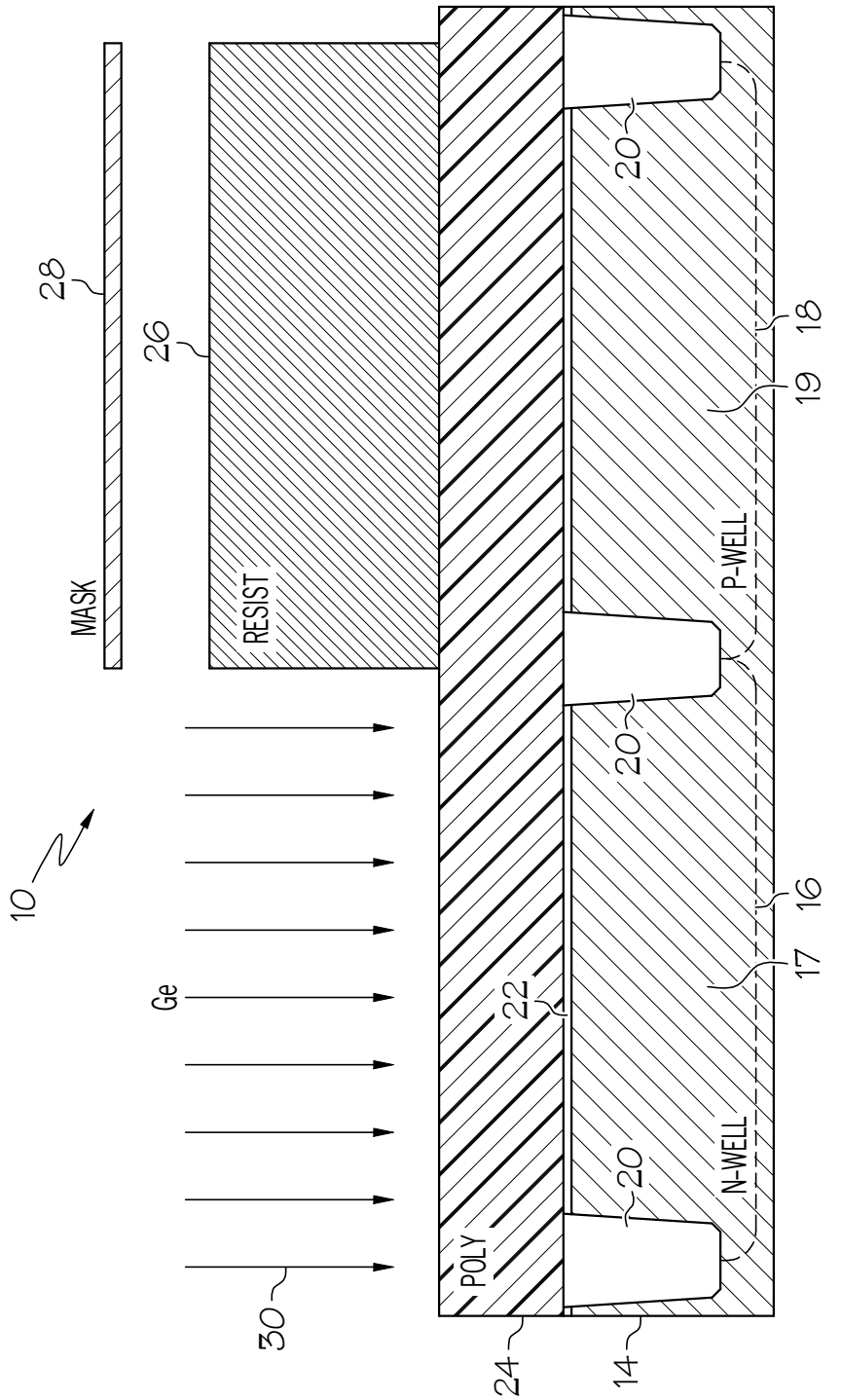

28
26
MASK
RESIST
10
Ge
30
POLY
N-WELL
P-WELL
20
22
24
14
16
17
18
19

FIG. 1A

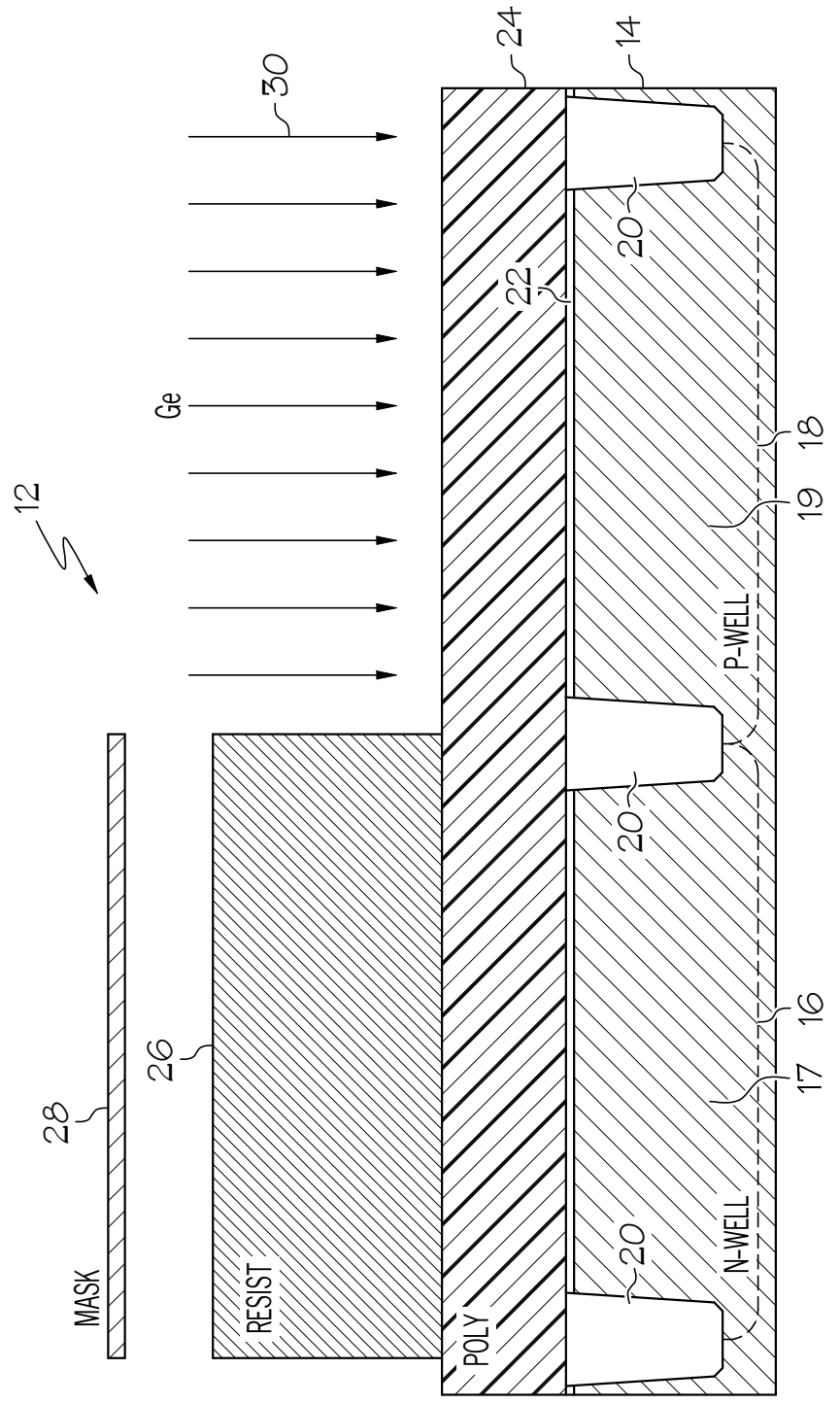

12
Ge
30
24
14
22
20
18
19
P-WELL
20
16
17
N-WELL
20
28
MASK
26
RESIST
POLY

FIG. 1B

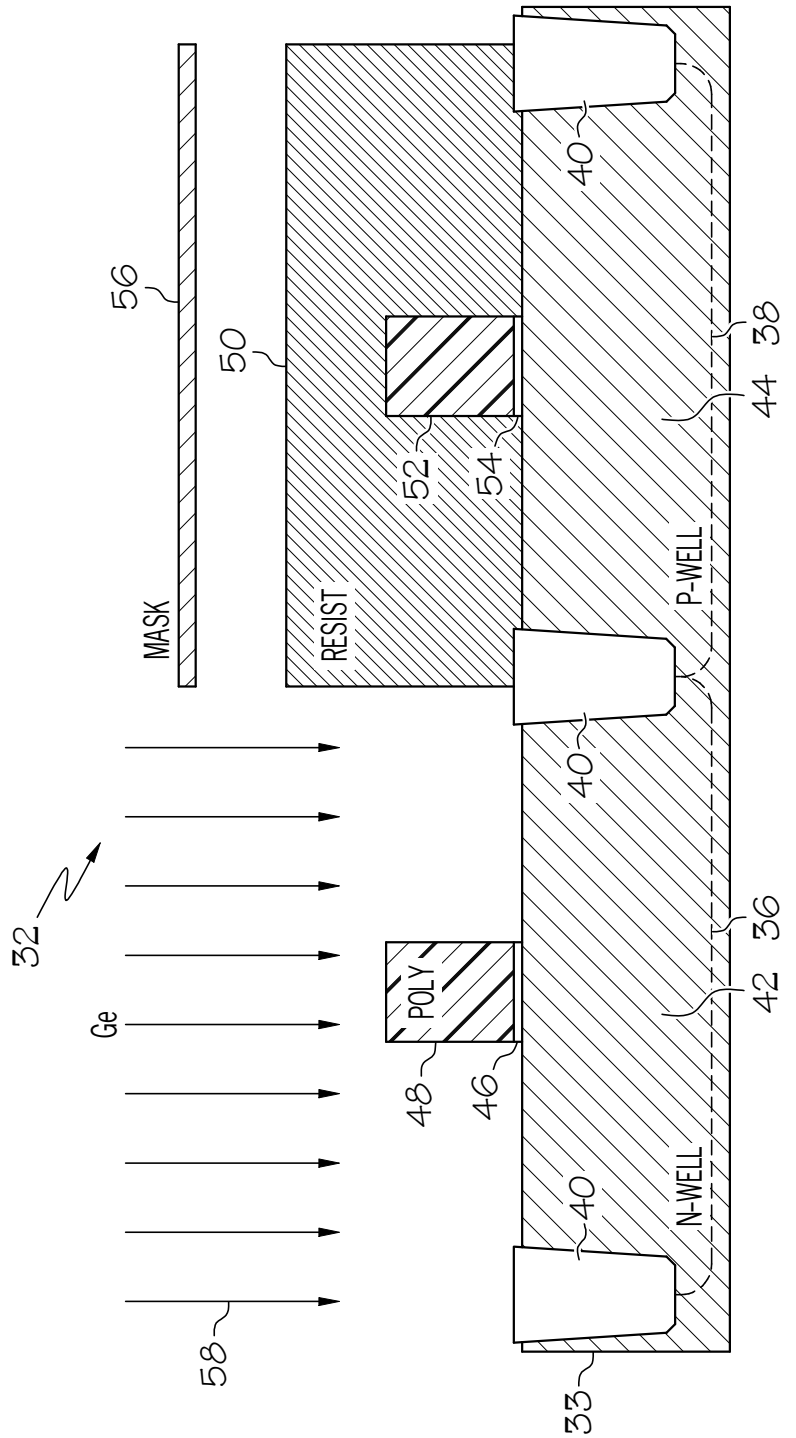

56
50
MASK
RESIST
52
54
40
38
44
P-WELL
40
36
42
32
Ge
POLY
48
46
40
N-WELL
58
33

FIG. 2A

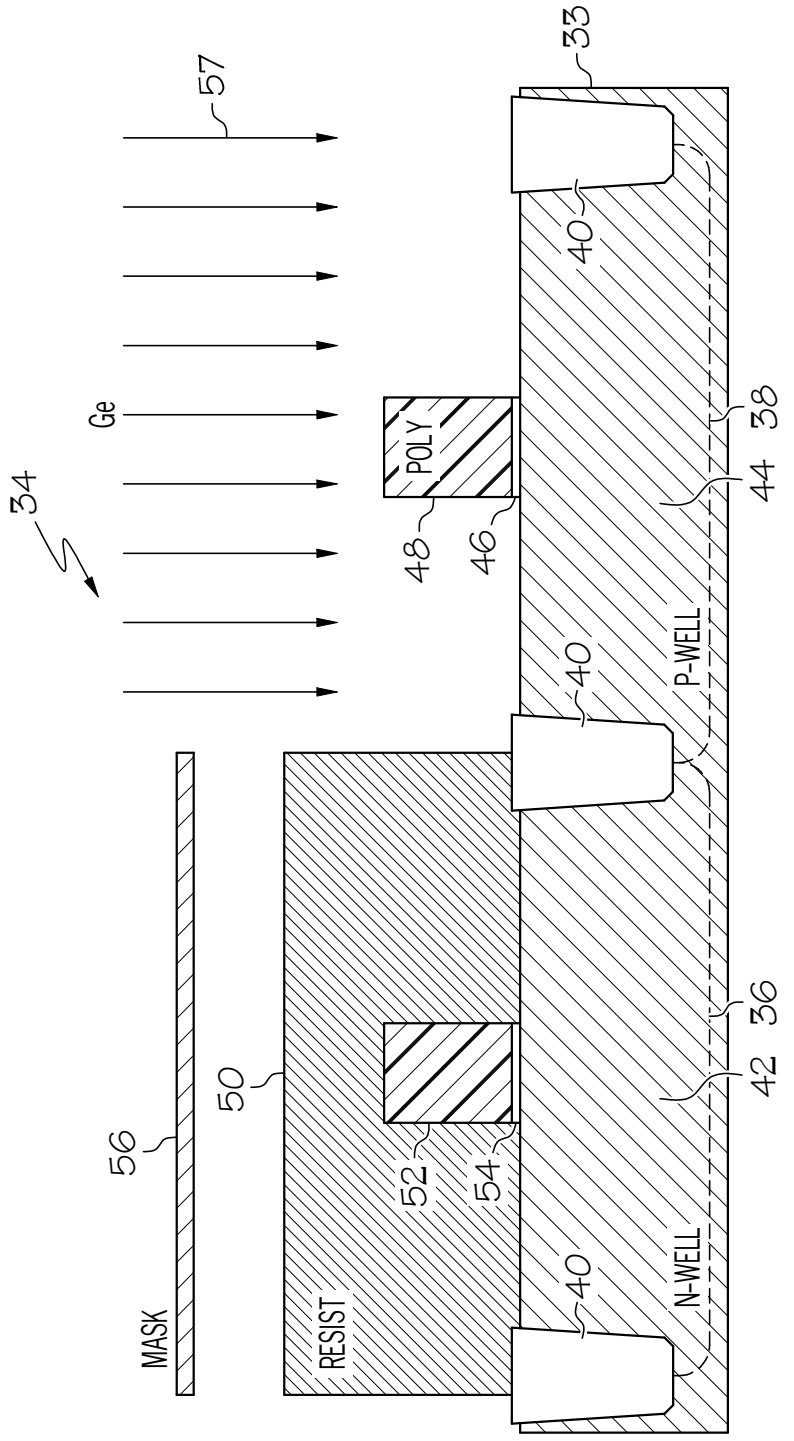

33
57
40
Ge
POLY
38
34
44
48
46
40
P-WELL
36
50
42
56
52
54
40
N-WELL
RESIST
MASK

FIG. 2B

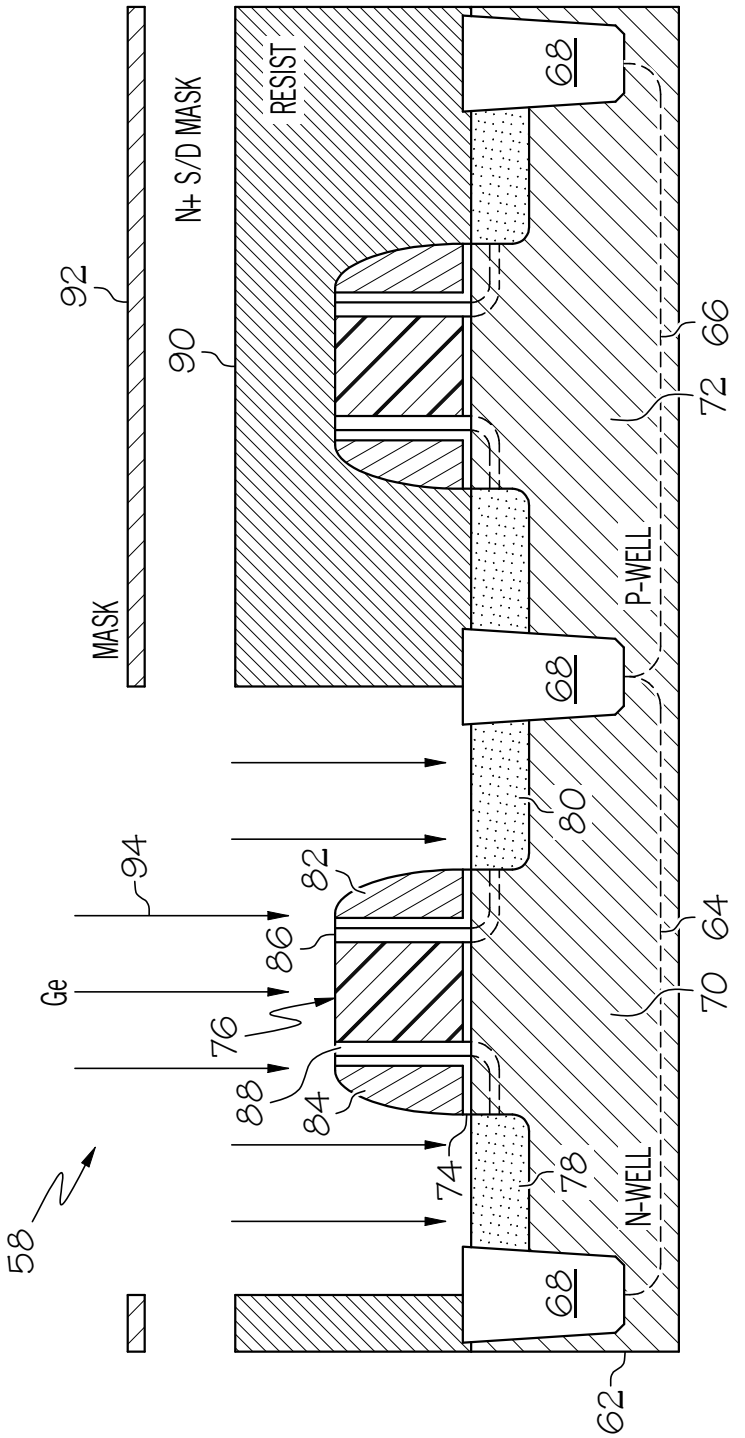

MASK
N+ S/D MASK
RESIST
92
90
68
66
72
P-WELL
80
82
64
70
94
86
Ge
76
88
84
74
78
N-WELL
58
62

FIG. 3A

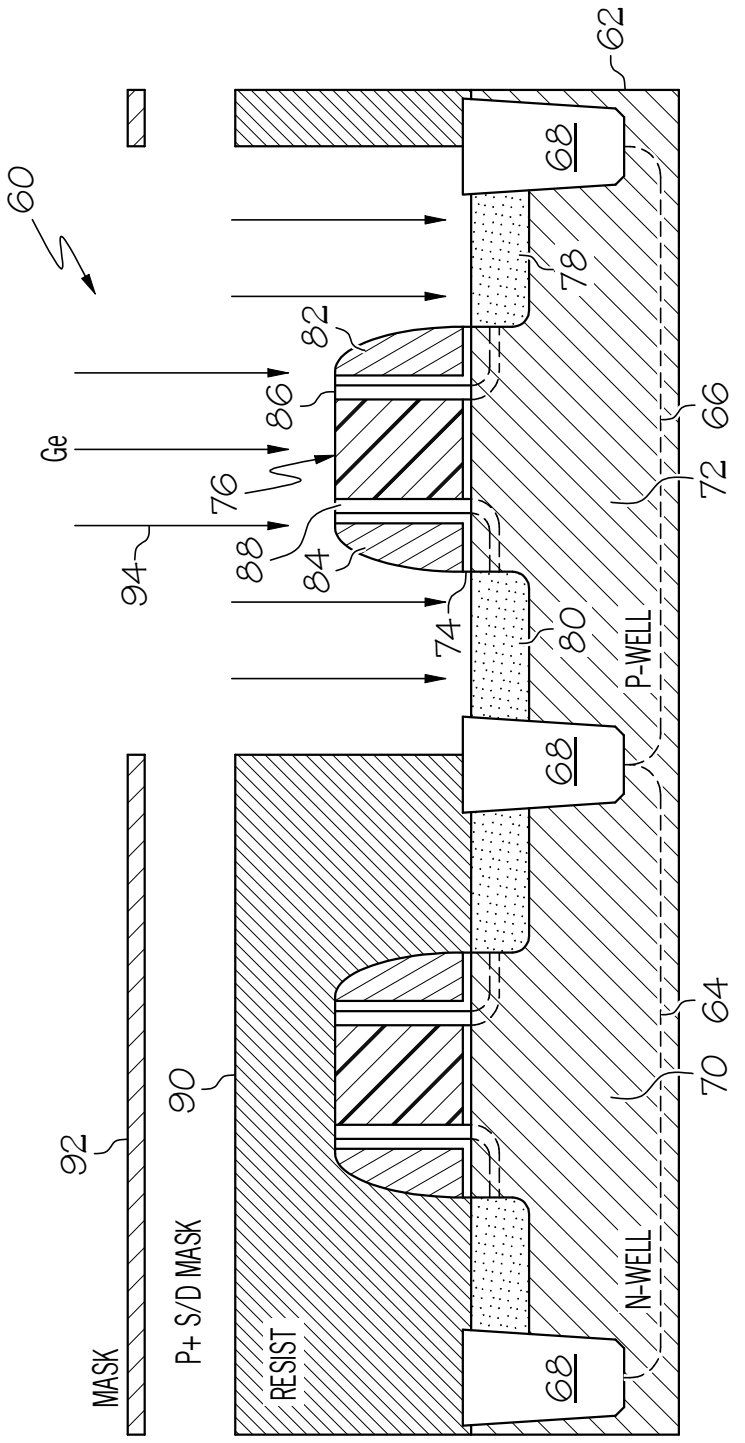

60
62
68
78
82
86
66
Ge
76
72
88
84
94
74
80
P-WELL
68
64
70
90
92
MASK
P+ S/D MASK
RESIST
N-WELL
68

FIG. 3B

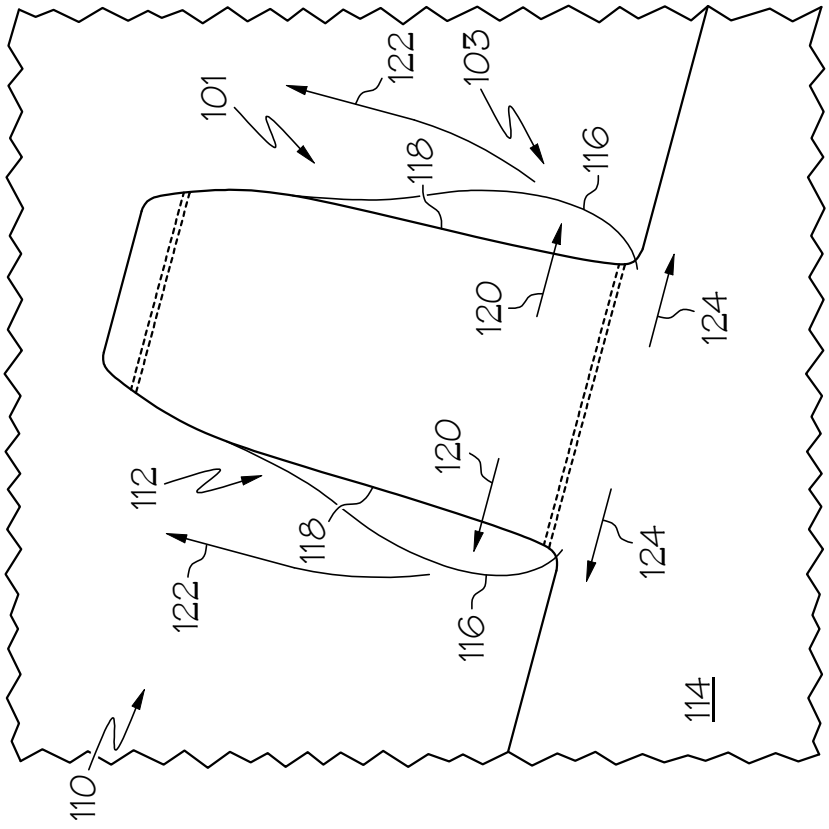

101
122
103
116
118
120
124
112
120
118
122
116
124
114
110

FIG. 5

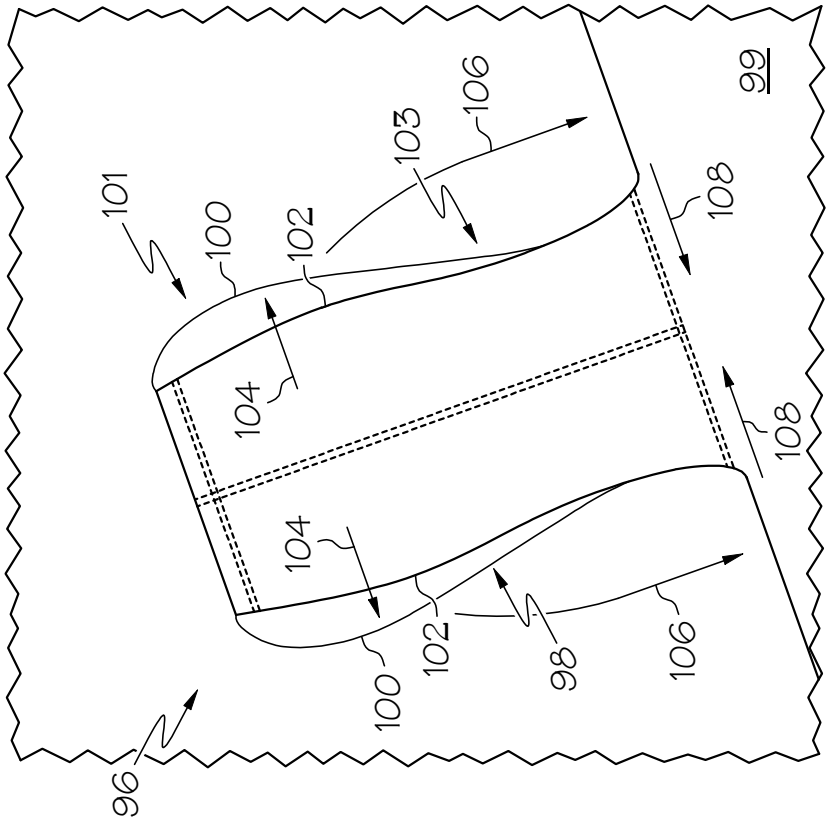

101
100
102
103
106
104
108
99
104
102
98
106
100
108
96

FIG. 4

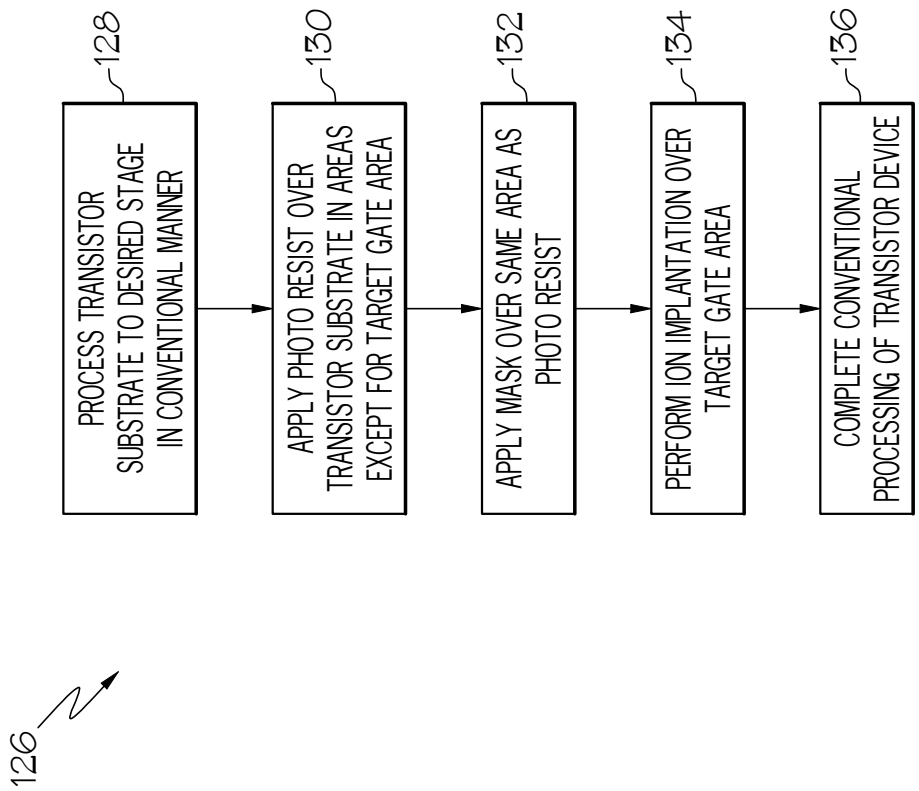

126
128
PROCESS TRANSISTOR SUBSTRATE TO DESIRED STAGE IN CONVENTIONAL MANNER
130
APPLY PHOTO RESIST OVER TRANSISTOR SUBSTRATE IN AREAS EXCEPT FOR TARGET GATE AREA
132
APPLY MASK OVER SAME AREA AS PHOTO RESIST
134
PERFORM ION IMPLANTATION OVER TARGET GATE AREA
136
COMPLETE CONVENTIONAL PROCESSING OF TRANSISTOR DEVICE

FIG. 6