WHAT IS CLAIMED IS:

1. A circuit comprising:

a silicon-controlled rectifier (SCR) having a first n-type layer with a cathode connection, a first p-type layer with a first control connection, a second n-type layer with a second control connection, and a second p-type layer with an anode connection, wherein the anode connection is coupled to a power rail, and the cathode connection is coupled to a ground rail; and

a tunable holding voltage control unit including a first NMOS having a first gate, a first drain, and a first source, the first drain being coupled to the first control connection, the first source being coupled to the ground rail, and the first gate being coupled to a program circuit, wherein during an ESD event, the first NMOS is turned off and a holding voltage of the SCR is low.

2. The circuit according to claim 1, wherein during normal operation, the first NMOS is turned on.

3. The circuit according to claim 1, wherein the tunable holding voltage control unit further includes a second NMOS having a second gate, a second drain, and a second source, the second drain being coupled to the first control connection, the second source being coupled to the ground rail, and the second gate being coupled to the program circuit, wherein during an ESD event, the first and second NMOS are turned off and the holding voltage of the SCR is low.

4. The circuit according to claim 3, wherein during normal operation, the first NMOS is turned on and the second NMOS is turned on when the holding voltage of the SCR with the first NMOS turned on is less than an operating voltage of the power rail.

5. The circuit according to claim 1, wherein the tunable holding voltage control unit includes n NMOS each having a gate, a drain, and a source, each drain being coupled to the first control connection, each source being coupled to the ground rail, and each gate being coupled to the program circuit, wherein during an ESD event, all n NMOS are turned off and the holding voltage of the SCR is low, wherein n ranges from 3 to 10.

6. The circuit according to claim 5, wherein during normal operation, the first NMOS is turned on and m of the n NMOS are turned on, wherein m NMOS being turned on results in the holding voltage of the SCR being greater than an operating voltage of the power rail.

7. The circuit according to claim 1, further comprising:

a trigger component with a control connection coupled with the second control connection.

8. The circuit according to claim 1, wherein the program circuit comprises:

a one-time program or multi-time program circuit with a first output control connection coupled with the first gate.

9. A method comprising:

providing a silicon-controlled rectifier (SCR) having a first n-type layer with a cathode connection, a first p-type layer with a first control connection, a second n-type layer with a second control connection, and a second p-type layer with an anode connection;

coupling the anode connection to a power rail;

coupling the cathode connection to a ground rail;

providing a tunable holding voltage control unit including a first NMOS having a first gate, a first drain, and a first source, wherein during an ESD event, the first NMOS is turned off and a holding voltage of the SCR is low;

coupling the first drain to the first control connection;

coupling the first source to the ground rail; and

coupling the first gate to a program circuit.

10. The method according to claim 9, wherein during normal operation, the first NMOS is turned on.

11. The method according to claim 9, wherein the tunable holding voltage control unit further includes a second NMOS having a second gate, a second drain, and a second source, wherein during an ESD event, the first and second NMOS are turned off and the holding voltage of the SCR is low, and wherein the method comprises:

coupling the second drain to the first control connection;

coupling the second source to the ground rail; and

coupling the second gate to the program circuit.

12. The method according to claim 11, wherein during normal operation, the first NMOS is turned on and the second NMOS is turned on when the holding voltage of the SCR with the first NMOS turned on is less than an operating voltage of the power rail.

13. The method according to claim 9, wherein the tunable holding voltage control unit includes n NMOS each having a gate, a drain, and a source, wherein during an ESD event, all n NMOS are turned off and the holding voltage of the SCR is low, wherein n ranges from 3 to 10, and wherein the method comprises:

coupling each drain to the first control connection;

coupling each source to the ground rail; and

coupling each gate to the program circuit.

14. The method according to claim 13, wherein during normal operation, the first NMOS is turned on and m of the n NMOS are turned on, wherein m NMOS results in the holding voltage of the SCR being greater than an operating voltage of the power rail.

15. The method according to claim 9, further comprising:

providing a trigger component with a control connection; and

coupling the control connection with the second control connection.

16. The method according to claim 9, further comprising:

providing a one-time program or multi-time program circuit with a first output control connection; and

coupling the first output control connection with the first gate.

17. A circuit comprising:

a silicon-controlled rectifier (SCR) having a first n-type layer with a cathode connection, a first p-type layer with a first control connection, a second n-type layer with a second control connection, and a second p-type layer with an anode connection, wherein the anode connection is coupled to a power rail, and the cathode connection is coupled to a ground rail;

a one-time or multi-time program circuit; and

a tunable holding voltage control unit including n NMOS each having a gate, a drain, and a source, each drain being coupled to the first control connection, each source being coupled to the ground rail, and each gate being coupled to the program circuit, wherein during an ESD event, the program circuit turns off all n NMOS and a holding voltage of the SCR is less than an operating voltage of the power rail, wherein n ranges from 2 to 10.

18. The circuit according to claim 17, wherein during normal operation, the program circuit turns on m of the n NMOS, wherein m NMOS raise the holding voltage of the SCR to a value greater than the operating voltage of the power rail.

19. The circuit according to claim 17, further comprising:

a trigger component with a control connection coupled with the second control connection.

20. The circuit according to claim 17, wherein the program circuit comprises a plurality of output control connections, each gate of the n NMOS being coupled to one of the plurality of output control connections.

WHAT IS CLAIMED IS:

1. A circuit comprising:

a silicon-controlled rectifier (SCR) having a first n-type layer with a cathode connection, a first p-type layer with a first control connection, a second n-type layer with a second control connection, and a second p-type layer with an anode connection, wherein the anode connection is coupled to a power rail, and the cathode connection is coupled to a ground rail; and

a tunable holding voltage control unit including a first NMOS having a first gate, a first drain, and a first source, the first drain being coupled to the first control connection, the first source being coupled to the ground rail, and the first gate being coupled to a program circuit, wherein during an ESD event, the first NMOS is turned off and a holding voltage of the SCR is low,

wherein the tunable holding voltage control unit further includes a second NMOS having a second gate, a second drain, and a second source, the second drain being coupled to the first control connection, the second source being coupled to the ground rail, and the second gate being coupled to the program circuit, and

wherein during an ESD event, the first and second NMOS are turned off and the holding voltage of the SCR is low.

2. The circuit according to claim 1, wherein during normal operation, the first NMOS is turned on.

3. The circuit according to claim 1, wherein during normal operation, the first NMOS is turned on and the second NMOS is turned on when the holding voltage of the SCR with the first NMOS turned on is less than an operating voltage of the power rail.

4. The circuit according to claim 1, wherein the tunable holding voltage control unit includes n NMOS each having a gate, a drain, and a source, each drain being coupled to the first control connection, each source being coupled to the ground rail, and each gate being coupled to the program circuit, wherein during an ESD event, all n NMOS are turned off and the holding voltage of the SCR is low, wherein n ranges from 3 to 10.

5. The circuit according to claim 4, wherein during normal operation, the first NMOS is turned on and m of the n NMOS are turned on, wherein m NMOS being turned on results in the holding voltage of the SCR being greater than an operating voltage of the power rail.

6. The circuit according to claim 1, further comprising:

a trigger component with a control connection coupled with the second control connection.

7. The circuit according to claim 1, wherein the program circuit comprises:

a one-time program or multi-time program circuit with a first output control connection coupled with the first gate.

8. A method comprising:

providing a silicon-controlled rectifier (SCR) having a first n-type layer with a cathode connection, a first p-type layer with a first control connection, a second n-type layer with a second control connection, and a second p-type layer with an anode connection;

coupling the anode connection to a power rail;

coupling the cathode connection to a ground rail;

providing a tunable holding voltage control unit including a first NMOS having a first gate, a first drain, and a first source and a second NMOS having a second gate, a second drain, and a second source, wherein during an ESD event, the first and second NMOS are turned off and a holding voltage of the SCR is low;

coupling the first drain to the first control connection;

coupling the first source to the ground rail;

coupling the first gate to a program circuit;

coupling the second drain to the first control connection;

coupling the second source to the ground rail; and

coupling the second gate to the program circuit.

9. The method according to claim 8, wherein during normal operation, the first NMOS is turned on.

10. The method according to claim 8, wherein during normal operation, the first NMOS is turned on and the second NMOS is turned on when the holding voltage of the SCR with the first NMOS turned on is less than an operating voltage of the power rail.

11. The method according to claim 8, wherein the tunable holding voltage control unit includes n NMOS each having a gate, a drain, and a source, wherein during an ESD event, all n NMOS are turned off and the holding voltage of the SCR is low, wherein n ranges from 3 to 10, and wherein the method comprises:

coupling each drain to the first control connection;

coupling each source to the ground rail; and

coupling each gate to the program circuit.

12. The method according to claim 11, wherein during normal operation, the first NMOS is turned on and m of the n NMOS are turned on, wherein m NMOS results in the holding voltage of the SCR being greater than an operating voltage of the power rail.

13. The method according to claim 8, further comprising:

providing a trigger component with a control connection; and

coupling the control connection with the second control connection.

14. The method according to claim 8, further comprising:

providing a one-time program or multi-time program circuit with a first output control connection; and

coupling the first output control connection with the first gate.

15. A circuit comprising:

a silicon-controlled rectifier (SCR) having a first n-type layer with a cathode connection, a first p-type layer with a first control connection, a second n-type layer with a second

control connection, and a second p-type layer with an anode connection, wherein the anode connection is coupled to a power rail, and the cathode connection is coupled to a ground rail;

a one-time or multi-time program circuit; and

a tunable holding voltage control unit including n NMOS each having a gate, a drain, and a source, each drain being coupled to the first control connection, each source being coupled to the ground rail, and each gate being coupled to the program circuit, wherein during an ESD event, the program circuit turns off all n NMOS and a holding voltage of the SCR is less than an operating voltage of the power rail, wherein n ranges from 2 to 10.

16. The circuit according to claim 15, wherein during normal operation, the program circuit turns on m of the n NMOS, wherein m NMOS raise the holding voltage of the SCR to a value greater than the operating voltage of the power rail.

17. The circuit according to claim 15, further comprising:

a trigger component with a control connection coupled with the second control connection.

18. The circuit according to claim 15, wherein the program circuit comprises a plurality of output control connections, each gate of the n NMOS being coupled to one of the plurality of output control connections.