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ABSTRACT

An intermetal dielectric structure for integrated circuits

is provided having a premetal dielectric and a metal line thereon, with a SRO liner on the premetal dielectric layer and the metal lines, a FGS dielectric layer over the SRO liner, a SRO film over the FGS dielectric layer, and a TEOS dielectric layer over the SRO film. Vias through the FGS dielectric layer are treated to have fluorine-free regions around the vias. The structure is not subject to fluorine attack on the metal lines or vias while having a stable FGS dielectric layer with less fluorine out-gassing and out-diffusion.

(FIG. 1)

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