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1 Semiconductor Device with Buried

Electrode

BACKGROUND OF THE INVENTION

5 Field of the Invention

This invention relates to a semiconductor integrated circuit device such as memory, photoelectric converting device, signal processing device, etc. to be mounted on various electronic instruments, particularly to a semiconductor device having a specific feature in its electrode structure and a method for preparing the same.

Related Background Art

To describe the prior art, as an example, the vertical PNP (hereinafter abbreviated as V-PNP) transistor which is used in recent years as the functional device for highly integrated semiconductor device may be mentioned. For example, one having the structure shown in Fig. 1 has been known. In Fig. 1, the symbol 1 is a P-type silicon substrate. On the P-type silicon substrate 1 is formed an N^+ buried layer 2, and on the N^+ buried layer 2 is formed a collector region 5 comprising a P^+ buried layer 3 and a P^- well layer 4. Within the P^- well layer 4 of the collector region 5 is formed an N^- well layer 6, and further within the P^- well layer 6 are formed a P^+ layer 7 and an N^+ layer 8 made apart from each

1 other. Within the N^- well layer 4 of the collector
region 5 is formed a P^+ layer 9 apart from the N^- well
layer 6. And, on the P^+ layer 7, the N^+ layer 8 within
the N^- well layer 6 and the P^+ layer 9 within the P^-
5 well layer 4 are respectively formed an emitter
electrode 10, a base electrode 11 and a collector
electrode 12.

Around the collector region 5 as mentioned
above, an N^- epitaxial layer 13 is formed.

10 In the V-PNP transistor with such structure,
when the transistor actuation enters saturation region
(stage), current may be sometimes leaked from the
collector region 5 through the N-epitaxial layer 13
into the P-type silicon substrate 1, thereby forming
15 a parasitic PNP transistor. For this reason, as shown
in Fig. 2, there has been also known a transistor which
has been made to have a constitution having a deep
 N^+ layer 14 in contact with the N^+ layer 2 and
surrounding the collector region 5 formed within the
20 N^- epitaxial layer 13, and further in which the emitter
grounding current amplification β of the parasitic PNP
transistor is reduced by biasing to the maximum
potential, whereby the leak current to the P-type
silicon substrate 1 can be reduced. The guard ring
25 electrode 15 of the transistor is taken out from the
 N^+ buried layer 2 through the N^+ layer 14.

However, in the transistor of the type shown

1 in Fig. 1 and Fig. 2, the current from the emitter
electrode 10 flows into the P^- well layer of the
collector region 5 and the P^+ buried layer 3,
wherefrom it is taken out through the P^+ layer 9 on
5 the transistor surface at the collector electrode 12,
and therefore the resistance of the P^- well layer 4
becomes larger, thus involving the drawback that the
collector series resistance becomes larger as a whole.
Further, when the collector series resistance becomes
10 larger, the emitter grounding current amplification β
of large current region becomes lower, while when
collector region 5 is taken larger, there will occur an
inconvenience that the device size becomes larger.

In the transistor shown in Fig. 2, because the
15 N^+ layer 14 is required to be provided within the N^-
(epitaxial) layer 13 around the collector region 5,
the margins of the collector region 5 and the device
separation region 16 are required to be taken
sufficiently large due to the influence of lateral
20 spreading of the diffusion layer, and therefore the
device size becomes large also in this case, and yet
the junction capacity with the N^+ layer 14 of the
collector region 5 will be increased.

The technical task as described above is
25 marked in V-PNP transistor, and also in other
functional devices, there is main electrode region
(buried collector, buried base, buried emitter,

1 buried source, buried drain, buried gate, etc.) within
semiconductor substrate, and it is applicable similarly
if a region for connecting electrically said electrode
region to the electrode wiring on the substrate surface
5 is required.

SUMMARY OF THE INVENTION

A primary object of the present invention is to
provide a semiconductor device more excellent than in
10 the prior art.

More specifically, the present invention has
been accomplished in order to solve the technical task
as described above, and its object is to provide a
semiconductor device capable of great current
15 actuation.

Another object of the present invention is to
provide a semiconductor device including a bipolar
transistor, having a collector region including a
first semiconductor region of the first
20 electroconduction type and a second semiconductor
region of the first electroconduction type having
higher resistance than said first semiconductor region,
a base region including a semiconductor region of the
second electroconduction type, and an emitter region
25 including a semiconductor region of the first
electroconduction type, said device comprising a
metal layer region for connecting said first

1 semiconductor region and the collector electrode on
said collector region provided within said second
semiconductor region layer of said collector region.

5 BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic sectional view showing an
example of the bipolar transistor of the prior art.

Fig. 2 is a schematic sectional view showing
another example of the bipolar transistor of the prior
10 art.

Fig. 3 is a schematic sectional view showing the
first embodiment of the present invention.

Figs. 4A to 4I are schematic sectional views
for illustration of the preparation method of the
15 semiconductor device according to the present invention.

Fig. 5 is a schematic sectional view showing
the second embodiment of the present invention.

Fig. 6 is a schematic sectional view showing
the third embodiment of the present invention.

20 Figs. 7A to 7E are schematic views for illustration
of the semiconductor device according to the third
embodiment of the present invention.

Fig. 8 is a schematic view for illustration
of the CVD apparatus to be used for preparation of
25 the semiconductor device according to the present
invention.

Figs. 9, 10 are schematic views showing one

1 example of the film forming apparatus to be used for
practicing the preferable film forming method of the
wiring layer in the semiconductor device according to
the present invention.

5 Fig. 11 is a schematic plan constitutional view
of the apparatus shown in Figs. 9 and 10.

Fig. 12 is a schematic constitutional view of
the movement order of the substrate in Fig. 11 added
with arrowheads.

10 Figs. 13A to 13D are schematic views for
illustration of the preferable film forming method
for formation of the wiring layer in the semiconductor
device according to the present invention.

15 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

In the following, preferred embodiments of the
present invention are described.

An electrode structure to be used in a
preferred embodiment of the present invention is an
20 electrode region comprising a metal region with an
aspect ratio buried within the semiconductor
substrate.

The electrode structure of the present
invention forms a part of the electrode wiring
25 internally of the semiconductor substrate in the
sense of series resistance reduction, and can be
utilized for all functional devices, namely functional

1 devices such as field effect transistor, bipolar
transistor, diffusion resistance, etc. Particularly,
great effects will be exhibited when it is utilized for
the collector electrode of a bipolar transistor, above
5 all V-PNP transistor.

(First embodiment)

Fig. 3 is a schematic sectional view showing a
V-PNP transistor as its example. In Fig. 3, the same
symbols are attached to the same constitutional
10 portions as in the V-PNP transistor of the prior art
shown in Figs. 9 and 10, and description thereof is
omitted.

In Fig. 3, the symbol 20 is a first electrode
region comprising a metal as the electroconductive
15 material. Here, $W < H$, with H/W being 1.0 or higher,
preferably 2.0 or higher, optimally 3.0 or higher,
whereby the area occupied by the collector electrode can
be made smaller. The first electrode region 20 connects
the P^+ buried layer 3 in the collector region 5 to the
20 collector electrode 12, and is formed here along the
direction crossed at right angle as the crosslinking
direction relative to the surface of the P-type silicon
substrate 1 within the P^- well layer 4 of the collector
region 5 between the P^+ buried layer 3 and the
25 collector electrode 12 and the interlayer insulation
film 18. The P^- well layer 4 has higher resistance
than the P^+ buried layer. In the present embodiment,

1 because the first wiring layer is in direct ohmic
contact with the P^+ buried layer 3, no impurity layer
corresponding to the P^+ layer 9 in the transistor of
the prior art shown in Figs.1 and 2 is formed.

5 As the electroconductive material for forming
such first electrode region 20, materials conventionally
employed for electrodes or wiring in electronic devices
or integrated circuit devices by use of semiconductors,
and among them pure aluminum or an aluminum composed
10 mainly of Al and containing silicon as a metal (Al-Si),
etc. may be preferably employed. Particularly, Al is
inexpensive, has high electroconductivity, and also
can form a dense oxidized film on the surface, thereby
having a number of advantages such that the inner
15 portion is chemically protected to be stabilized
and has good adhesion with Si, and therefore it can
be preferably used when connecting well the P^+ buried
layer 3 to, for example, a collector electrode 12
comprising Al.

20 Thus, when the metal buried electrode is
electrically connected to a predetermined portion only
at the bottom of the groove, the whole side wall
surface should be preferably covered with an insulation
film.

25 On the other hand, when the metal buried
electrode is insulated from a part of the side wall
or the bottom of the groove, only said portion is

1 covered with an insulation film.

Next, by referring to Fig. 4A to Fig. 4I, an example of the present invention is described.

1) First, for example, on the surface of a
5 P-type silicon substrate 1 having an impurity concentration of 10^{14} to $10^{15}/\text{cm}^3$, a thermally oxidized film 30 comprising SiO_2 for diffusion mask, etc. is formed with a thickness of, for example, 0.8 to 1.0 mm, and the by patterning of the thermally
10 oxidized film 30, openings 31 with predetermined sizes, shapes are formed. Next, with the thermally oxidized film 30 as the mask, an N-type impurity such as Sb (antimony) or As (arsenic) is introduced according to the ion injection method in the surface of the P-type
15 silicon substrate 1 through the openings 31 of the thermally oxidized film 30, heat treatment is carried out to activate the N-type impurity simultaneously with diffusion thereof internally of the P-type silicon substrate 1. Thus, for example, an N^+ buried
20 layer 2 with a sheet resistance 40 to $120 \Omega/\square$ is formed (Fig. 4A).

2) Next, after removal of the thermally oxidized film 30 as described above, a thermally oxidized film 32 comprising another SiO_2 , etc. is
25 formed with a thickness of, for example, 100 to 1000 Å. Resist patterning is effected on the thermally oxidized film 32. After incorporation of a P-type

1 impurity of B (boron) into the N^+ buried layer 2 and
the region surrounding outside of the N^+ buried layer
B through the openings of the resist, heat treatment
is applied after removal of the resist. By such heat
5 treatment, the impurity as described above is
activated simultaneously with diffusion internally of
the substrate 1. Thus, P^+ layers 33, 34 of, for
example, 200 to 1000 $\Omega/\square$ are formed (Fig. 4B).

3) Next, after removal of all the oxidized
10 films on the silicon substrate 1, an N-type epitaxial
layer 13 is grown. The N-type epitaxial layer 13
should desirably have its thickness of about 1 to
5 μm , and a specific resistance of about 1 to 20 Ω/cm .
In such epitaxial growth, the impurity is diffused
15 into the N-type epitaxial layer 13 from the P^+ layers
33, 34. Particularly, from the N^+ buried layer 2
(P^+ layer 33), the N-type and P-type impurities are
diffused into the N-type epitaxial layer 13. However,
since the P-type impurity with greater coefficient of
20 diffusion is diffused at higher diffusion speed, a P^+
buried layer 3 will be formed on the N^+ buried layer
2 (Fig. 4C).

4) Next, a thermally oxidized film is formed
on the surface of the N-type epitaxial layer as
25 described above, the thermally oxidized film is
subjected to patterning to form openings. After
introduction of a P-type impurity such as B into

1 the surface of the N-type epitaxial layer 13 according
to ion injection through the openings with the
thermally oxidized film as the mask, heat treatment
is effected to have the impurity diffused internally of
5 the N-type epitaxial layer 13. By such ion injection
method and heat treatment, a P⁻ well layer 4 is formed
on the P⁺ buried layer 3 (Fig. 4D). The well layer 4
should desirably have a sheet resistance of about 2
to 10 k Ω /□.

10 5) Next, after removal of the thermally
oxidized film from above the N-type epitaxial layer
13, a thermally oxidized film with a thickness of 100 to
1000 Å and a non-oxidizable film comprising Si₃N₄, etc.
with a thickness of 1000 to 2000 Å are successively
15 laminated. Next, on the laminated film, patterning
is applied to form openings for device separation
region as described below. And, according to the
selective oxidation by use of the laminated film as
the oxidation resistant mask, a field oxidized film
20 region 17 for device separation (thickness 0.8 to
1.0 μ m) and a device region for bipolar region are
formed, and then the laminate film as described above
is removed (Fig. 4E).

25 6) Next, a thermally oxidized film with a
thickness of 200 to 1000 Å is formed on the N⁺ type
epitaxial layer 13 in the device region, the thermally
oxidized film is applied with resist patterning to

1 form openings for base formation of the bipolar
transistor. Then, after introduction of an N-type
impurity through the openings, the thermally oxidized
film is removed and then heat treatment is effected.
5 By doing so, a N^- well layer (base) 6 is formed within
the P^- well layer 4. The formation conditions of
the base layer 6, which depend on the characteristics
of the bipolar transistor to be prepared, should
desirably be made to have a sheet resistance of about
10 0.6 to 3 $k\Omega/\square$. (Fig. 4F).

7) Next, on the surface of the device region,
a thermally oxidized film is formed, and the thermally
oxidized film is applied with resist patterning to
form openings at the positions corresponding to the
15 N^- well layer (base) 6 of the thermally oxidized
film, namely the emitter formation region of the
resist and the PN device separation region. Next,
after introduction of a P-type impurity such as B,
 BF_2 etc. through these openings, the thermally
20 oxidized film as the resist is removed.

Next, a thermally oxidized film is formed on
the surface of the N^- well layer (base) 6, the
thermally oxidized film is applied with resist
patterning to form openings for formation of the N^+
25 layer of the base contact. Next, after formation of
an N-type impurity such as As, etc. through the
openings according to the ion injection method,

1 a thermally oxidized film as the resist is formed.

Then, the P-type impurity is activated and diffused by application of heat treatment to form the P^+ layer 7 and the N^+ layer 8 separately from each other at the upper portion of the N^- well layer (base) 6 (Fig. 4G).

The ion injection conditions of the P-type impurity in this step and subsequent heat treatment conditions are determined depending on the characteristics of the bipolar transistor to be prepared.

8) Next, on the whole surface of the device region and the device separation, for example, BPSG (Boro-phospho silicate glass), etc. is deposited to a thickness of about 0.6 to 1.0 μm according to the CVD method, annealing is applied to form an interlayer insulation film 18.

9) Next, a thermally oxidized film is formed on the interlayer insulation film 18, and the thermally oxidized film is applied with resist patterning to form openings for contact hole. Subsequently, through the openings the interlayer insulation film 18 and the P^- well layer 4 are applied with etching in two steps to form collector contact holes reaching the surface of the P^+ buried layer 3, and then the thermally oxidized film as the resist is removed. Then, a first electrode region 20 comprising an Al film

1 or an Al-Si film is formed according to the Al-CVD
method (Fig. 4H).

10) Next, on the surface of the device region
is formed a thermally oxidized film, which thermally
5 oxidized film is applied with patterning to form
resist openings for formation of contact holes for
base and emitter. Next, through these openings, etching
is applied on the interlayer insulation film 18 to form
base contact holes and emitter contact holes,
10 respectively. Subsequently, within these base contact
holes and emitter contact holes, electrode layers 21
and 22 comprising an Al film or an Al-Si film are again
formed so as to be coplanar with the interlayer
insulation film 18 according to the Al-CVD method.

15 Next, an Al film or Al-Si film is formed with
a thickness of 0.5 to 1.0 μm on the whole surface of
the device region according of the non-selective CVD
method or sputtering method, and by application of
patterning to the Al film, etc., the respective
20 electrodes of emitter electrode 10, base electrode 11,
collector electrode 12 and the wirings accompanying
these are formed to prepare desired V-PNP (Fig. 4I).

As shown in Fig. 4H, the first electrode
region 20 is grown so as to be coplanar with the
25 interlayer insulation film 18 according to the Al-CVD
method, but it is also possible to stop once the
selective growth at the stage when the first wiring

1 layer 20 has been grown to coplanar with the P^+ well
layer 4, and effect selective growth by initiating
again the Al-CVD method after formation of the base
and emitter contact holes as described above, thereby
5 making the respective upper surface of the first
electrode region 20 and the electrode layers 21, 22
coplanar.

In a V-PNP transistor thus constituted, since
the first electrode region 20 is provided, the
10 collector series resistance of the P^- well layer 4
can be reduced to great extent, and therefore reduction
of the emitter grounding current amplitude β of the
large current region, namely the present transistor
can be ameliorated.

15 (Second Embodiment)

Fig. 5 is a schematic sectional view showing
another embodiment of the present invention. Also
in Fig. 5, the same constituent portions as those of
the V-PNP transistor of the prior art showing Figs.
20 1, 2 are attached with the same symbols, and
description there of is omitted.

The present invention can be suitably used
for the second wiring layer comprising an
electroconductive material shown by the symbol 24 in
25 Fig. 5. The second electrode region 24 connects the
guard ring electrode 15 on the interlayer insulation
film 17 to the N^+ buried layer 2, and is formed along

1 the direction crossing at right angle to the surface of
the P-type silicon substrate 1 so as to extend through
the N⁻ epitaxial layer 13 surrounding the collector
region 5 and the interlayer insulation film 17.

5 As the electroconductive material forming the
second electrode region 24, the same kind as that
forming the first electrode material region 20 as
described above can be used. And, when forming both
of the electrode regions 20, 24, for example, after
10 formation of necessary contact holes according to such
steps as resist patterning, etching, etc., the both
electrode regions 20, 24 can be formed at the same
time according to the Al-CVD method preferable for
formation of the electrode regions according to the
15 present invention.

In a V-PNP transistor thus constituted, since
the second electrode region 24 is provided, even a
parasitic PNP transistor may be constituted at the
saturation step as the transistor actuation, the
20 emitter grounding current amplification β of the
parasitic PNP transistor can be reduced, and also the
leak current to the P-type silicon substrate 1 reduced
by biasing to the maximum potential. And, in the
V-PNP transistor, as different from the structure of
25 the V-PNP transistor of the prior art shown in Fig.
1, the second electrode region 24 is provided
comprising Al, etc. instead of the deep N⁺ layer 14,

1 and therefore no diffusion of the dopant from the N^+
layer 14 is required to be considered. Hence, no
great margin of the collector region 5 and the device
separation region 16 is required to be taken, whereby
5 the device size can be made smaller and also the
junction capacity of the collector region 5 can be
made smaller.

As described above, for formation of the first
electrode region 20 or the second electrode region 24,
10 other methods, for example, the sputtering method, the
gas phase method such as the CVD method, etc. by use
of triethylaluminum can be used, provided that such
deep hole can be buried. However, particularly with
respect to the point that Al, films of good quality,
15 etc. can be formed in the case when the aspect ratio
(depth of hole/hole diameter) is relatively larger and
the hole diameter itself is smaller as the contact
hole for wiring layer as described above, the Al-CVD
method as described below is preferred. According to
20 the Al-CVD method, fine working can be suitably
effected not only for an aspect ratio of 1.0 or higher
as a matter of course, but also for 2.0 or higher, or
3.0 or higher.

Referring now to specific examples, the
25 present invention is described in detail.

[Experimental example 1]

In the following manner, a V-PVP transistor

1 with the constitution shown in Fig. 3 was prepared.

First, on the surface of a P-type silicon substrate having an impurity concentration of 10^{14} to $10^{15}/\text{cm}^3$ was formed a thermally oxidized film comprising
5 SiO_2 , etc. for diffusion mask with a thickness of 0.8 to 1.0 μm , and the thermally oxidized film was subjected to patterning to form openings with predetermined sizes, shapes on the thermally oxidized film. Subsequently, after introduction of an N-type
10 impurity such as Sb (antimony) or As (arsenic) into the P-type silicon substrate through the openings according to the ion injection method, heat treatment was effected to activate the N-type impurity simultaneously with diffusion internally of the
15 P-type silicon substrate. Thus, an N^+ buried layer of 40 to 120 $\Omega/\square$ was formed.

Next, after removal of the thermal fixed film as described, another thermal oxidized film comprising SiO_2 , etc. was formed with a thickness of about 100
20 to 10000 $\text{\AA}$. On the thermally fixed film was applied resist patterning, and after introduction of a P-type impurity of B (boron) in the N^+ buried layer and the region surrounding the outside of the N^+ buried layer through the openings of the resist, heat
25 treatment was applied after removal of the resist. By such heat treatment, the above-mentioned impurity was activated simultaneously with diffusion internally

1 of the silicon substrate. Thus, a P^+ layer of 200 to
1000 $\Omega/\square$ was formed.

As the next step, all of the oxidized films on
the silicon substrate were removed, and then an N-type
5 epitaxial layer was grown. The N-type epitaxial layer
had a thickness of about 1 to 5 μm and a specific
resistance of about 1 to 20 Ω/cm . By such epitaxial
grown, a P^+ -type buried layer was formed on the N^+
buried layer.

10 Next, on the surface of the N^- epitaxial layer,
a thermally oxidized film was formed, the thermally
oxidized film was subjected to patterning to form
openings, and after introduction of a P-type impurity
such as B, etc. into the N^- epitaxial layer surface
15 with the thermally oxidized film as the mask through
its openings according to the ion injection method,
heat treatment was effected to have the impurity
diffused internally of the N^- epitaxial layer. By
doing so, a P^- well layer was formed on the P^+ buried
20 layer. The P^- well layer had a sheet resistance of
2 to 10 $\text{k}\Omega/\square$.

Next, after removal of the thermally oxidized
film from above the N^- epitaxial layer, again a
thermally oxidized film with a thickness of 100 to
25 10000 $\text{\AA}$ and a non-oxidizable film comprising Si_3N_4 ,
etc. with a thickness of 1000 to 2000 $\text{\AA}$ were
successively laminated. Then, the laminated film was

1 applied with patterning to form openings for device
separation region as described below. And, by the
selective oxidation by use of the laminated film as
oxidation resistant mask, the field insulation film
5 region for device separation (thickness 0.8 to 1.0 μm)
and the device region for bipolar transistor were
formed, followed by removal of the laminated film.

Subsequently, on the surface of the N^-
epitaxial layer in the device region, a thermally
10 oxidized film with a thickness of 200 to 10000 $\text{\AA}$ was
again formed, which thermally oxidized film was applied
with resist patterning to form openings for base
formation of bipolar transistor. Then, after
introduction of an N-type impurity through the
15 openings according to the ion injection method, the
thermally oxidized film as the resist was removed,
following by heat treatment. By doing so, an N^- well
layer (base) was formed within the P^- well layer.
The base layer had a sheet resistance of about 0.6 to
20 3 $\text{k}\Omega/\square$.

Next, on the surface of the device region a
thermally oxidized film was formed, and the thermally
oxidized film was applied with resist patterning to
form openings at the positions corresponding to the N^-
25 well layer (base), namely the emitter formation region
and the PN device separation region. Then, after
introduction of a P-type impurity such as B, BF_2 , etc.

1 through these openings according to the ion injection
method, the thermally oxidized film as the resist was
removed.

Subsequently, a thermally oxidized film was
5 formed on the N^- well layer (base), and the thermally
oxidized film was applied with resist patterning to
form openings for formation of the N^+ layer for base
contact. Then, after introduction of an N-type
impurity such as As, etc., the thermally oxidized film
10 as the resist was removed.

Then, the P-type and N-type impurities were
activated, diffused by application of heat treatment
to form the P^+ layer and the N^+ layer separate from
each other on the upper part of the N^- well layer
15 (base).

As the next step, after growth of BPSG, etc.
on the whole surface of the device region and the
device region to a thickness of 0.6 to 1.0 μm
according to the CVD method, annealing was applied to
20 form an interlayer insulation film.

Next, a thermally oxidized film was formed on
the interlayer insulation film, and the thermally
oxidized film was applied with resist patterning to
form openings for collector contact hole. Subsequently,
25 after formation of the interlayer insulation film and
the P^- well layer through the openings, etching was
applied in two steps to form contact holes reaching

1 the P^+ buried layer surface, followed by removal of the
thermally oxidized film as the resist. Next, within
the collector contact holes, a first electrode region
comprising an Al film was formed by use of DMAH and
5 hydrogen while maintaining the substrate surface
temperature at 270°C. The first electrode region was
permitted to grow until its surface became coplanar
with the interlayer insulation film surface.

Next, a thermally oxidized film was formed on
10 the surface of the device region, and the thermally
oxidized film was applied with patterning to form
resist openings for formation of contact holes for
base and emitter. Subsequently, through these openings,
the interlayer insulation film was applied with etching
15 to form base contact holes and emitter contact holes,
respectively.

Then, within these base contact holes and
emitter contact holes, respective electrode regions
comprising Al film were formed according to the Al-CVD
20 method.

Next, according to the sputtering method, an
Al film was formed with a thickness of about 0.5 to
1.0 μm , and the Al film was applied with patterning to
form a desired V-PNP transistor having the respective
25 electrodes such as emitter electrode, base electrode,
collector electrode, etc. and the wirings accompanied
with these formed thereon.

1 In the V-PNP transistor thus prepared,
reduction of the emitter grounding current amplification
 β could be ameliorated.

[Second Experimental Example]

5 A V-PNP transistor with the constitution shown
in Fig. 4 was prepared. The preparation steps are
the same as those in the first Example as described
above up to the steps before formation of the first
electrode region according to the Al-CVD method.

10 In the present Example, the first electrode
region and the second electrode region were formed
at the same time according to the Al-CVD method.

 In the V-PNP transistor thus prepared reduction
of the emitter grounding current amplification β could
15 be ameliorated, and further the β of the parasitic
transistor could be reduced.

 As described above, according to the present
Example, the collector series resistance of the P^- well
layer of the collector region can be reduced to great
20 extent by the first electrode region for connecting
the surface electrode for collector and the P^+ buried
region of the collector region, whereby reduction of
the emitter grounding current amplification β of the
bipolar transistor can be ameliorated, and also the
25 frequency characteristic can be improved.

 Also, according to the present invention, in
addition to the first electrode region as described

1 above, by the second electrode region connecting the
electrode for guard ring on the N^- epitaxial layer and
the N^+ buried layer, the β of the parasitic transistor
can be reduced, and also the leak current to the
5 substrate can be reduced, even if the maximum
potential may be biases without enlargement of the
device size. Further, improvement of frequency
characteristic can be effected, because the junction
capacity of the collector region can be made smaller.

10 (Third Embodiment)

Next, the electrode structure according to
the present invention is described by referring to an
example in which it is applied to static induction
transistor (SIT).

15 Referring now to drawings, an example of the
present invention is described. In Fig. 6, 101 is a
semiconductor substrate such as silicon, 101' a source
region, 102 a gate diffusion region, 103 a drain
diffusion region, 104 an insulation region such as
20 silicon dioxide, 105 a metal wiring region formed
by the sputtering method, etc., 106 an electrode
region comprising aluminum or aluminum-silicon
deposited within the concavity 110 by the selective
aluminum CVD method.

25 Figs. 7A to 7E are preparation steps of the
SIT according to the present Example.

First, on the substrate 401' which becomes

1 the source region, a silicon dioxide film 404 is grown
to 4000 Å according to the thermal oxidation method on
the silicon substrate 401 provided with an epitaxial
layer with high resistance. Next, at predetermined
5 positions of the oxidized film 404, holes are opened
for the drain region of 1 μm square. Next, by way of
ion injection, arsenic is implanted at 1×10^{16} ions/cm²,
to form a drain diffusion layer 403 (Fig. 7A).

Next, according to the lithographic steps, for
10 example, a resist image with holes of about 0.8 μm in
width being opened is formed according to the
lithographic steps. With that resist as the mask, the
oxidized film 404 was subjected to hole opening by dry
etching by use of an etchant of the C₂F₆-CHF₃ system,
15 and then a concavity 410 with a depth of, for example,
about 1.0 μm is formed by dry etching of the CCl₂F₂-N₂
system on the substrate 401. Then, the resist used for
the mask was removed, and a silicon dioxide film with a
thickness of 1500 Å is permitted to grow on the side and
20 the bottom surfaces of the concavity 410. At this
time, also the exposed portion of the drain surface is
covered at the same time with silicon dioxide, and
then reactive ion etching with the C₂F₆-CHF₃ is effected
to have only the bottom surface of the concavity 410
25 exposed (Fig. 7B).

Next, by ion injection, boron trifluoride is
implanted at a density of 1×10^{15} ions/cm².

1 Subsequently, ion activation is effected in a nitrogen
atmosphere of about 1000°C, 10 minutes to form a gate
diffusion layer 402 (Fig. 7C).

Next, burying within the concavity of the
5 aluminum-silicon which is the specific feature of the
present invention is practiced. For the substrate with
the structure shown in Fig. 7C, the treatment for
burying the aluminum-silicon is described in detail by
referring to Fig. 8.

10 First, a substrate is arranged in the loadlock
chamber 511. Into the loadlock chamber 511 is
introduced hydrogen as described above to form a
hydrogen atmosphere. And, the reaction chamber
512 is evacuated internally to ca. 1×10^{-8} Torr by the
15 evacuation system 510.

However, an Al-Si film can be formed even if the
vacuum degree within the reaction chamber 512 may be
poorer than 1×10^{-8} Torr.

And, from the gasline not shown, dimethylaluminum
20 hydride (DMAH) and Si_2H_6 are fed. For the carrier gas
through the DMAH line, H_2 is employed.

The second gasline not shown is for H_2 as the
reaction gas, and H_2 is permitted to flow through the
second gasline, and the opening of the slow leak valve
25 not shown was controlled to adjust the pressure within
the reaction chamber 512 to a predetermined value.
A typical pressure in this case is made ca. 1.5 Torr.

1 Through the DMAH line, DMAH is introduced into the
reaction tube. The total pressure is ca. 1.5 Torr, and
the DMAH partial pressure is made ca. 1.5×10^{-4} Torr,
and the Si_2H_6 partial pressure 2×10^{-6} Torr. Then, the
5 lamp is lighted to heat directly the wafer. Thus, an
Al-Si is deposited.

As the starting gas containing Si as the
second starting gas during formation of the Al-Si film,
 Si_2H_6 , SiH_4 , Si_3H_8 , $\text{Si}(\text{CH}_3)_4$, SiCl_4 , SiH_2Cl_2 , SiH_3Cl can
10 be employed.

By addition of DMAH, H_2 and Si starting gas
such as Si_2H_6 , etc., an Al-Si containing
0.5 to 2.0% of Si can be deposited. The reaction tube
pressure may be 0.05 to 760 Torr, desirably 0.1 to 0.8
15 Torr, the substrate temperature 260°C to 440°C , the
DMAH partial pressure 1×10^{-5} -fold to 1.3×10^{-3} -fold
of the pressure within the reaction tube, the Si_2H_6
partial pressure in the range of 1×10^{-7} to 1×10^{-4} -
fold of the pressure within the reaction tube, whereby
20 an Al-Si can be thus deposited.

After elapse of a predetermined deposition time,
feeding of DMAH is once stopped. The predetermined
deposition time for the Al-Si film deposited in the
process refers to the time before the Al-Si buries the
25 concavity 410 therein, which is about 20 minutes. The
substrate of the substrate temperature by direct heating
at this time is made 270°C . During the steps up to this

1 step, an Al-Si film 406 is deposited selectively only at
the concavity portion 410 (see Fig. 7D).

Next, on the drain region 403, holes are opened
according to lithographic steps, and an aluminum-silicon
5 405 is deposited to 8000 Å on the whole substrate surface
by the DC sputtering method. Finally, dry etching
according to the Cl_2BCl_3 -He system is applied to work the
aluminum-silicon to a desired wiring shape (see Fig.
7E).

10 In the Example as described above, description is
made about the case of N channel SIT wherein the drain
electrode 103 is n-type and the gate electrode 102 is
the p-type N channel SIT, but P-channel wherein the drain
electrode 103 is p-type and the gate electrode 102 is
15 n-type can be also similarly formed.

As described above, by use of the selective
aluminum CVD method, a buried electrode region of the
improved type SIT with a width of the concavity of 0.8
µm or less can be formed with high reliability.

20 The film forming method preferable for the
present invention is to form a deposited film by the
surface reaction on an electron-donative substrate
by use of a gas of an alkylaluminum hydride and
hydrogen gas (hereinafter called the Al-VCD method).

25

1 Particularly, by use of monomethylaluminum
hydride (MMAH) as the starting gas or dimethylaluminum
hydride (DMAH) as the starting gas, and H_2 gas as the
reactive gas, and heating the substrate surface under
5 the mixture of these gases, an Al film of good quality
can be deposited. Here, during the selective
deposition of Al, it is preferable to maintain the
surface temperature at the decomposition temperature
of the alkylaluminum hydride or higher and less than
10 450°C, more preferably 260°C to 440°C.

As the method for heating the substrate to the
above-mentioned temperature range, there are direct
heating and indirect heating. Particularly, by
maintaining the substrate at the above-mentioned
15 temperature by direct heating, an Al film of good
quality can be formed at high deposition speed. For
example, when the substrate surface temperature during
Al film formation is made 260 °C to 440 °C which is
more preferable temperature range, a film of good
20 quality can be obtained at higher deposition speed of
300 Å to 5000 Å/min. which is higher than in the case
of resistance heating. As such direct heating method
(substrate itself is heated by direct transmission of
the energy from the heating means to the substrate),
25 for example, lamp heating by means of halogen lamp,
xenon lamp, etc. may be included. As the method for
indirect heating, there is resistance heating, by

1 which heating can be performed by use of a heat-
generating body, etc. provided at the substrate
supporting member for supporting the substrate to
form deposited film arranged in the space for
5 formation of the deposited film.

By applying the CVD method to the substrate
having the electron-donative surface portion and the
non-electron donative surface portion co-present
thereon, a single crystal of Al is formed under good
10 selectivity only on the electron-donative substrate
surface portion. The Al thus formed will have all of
excellent characteristics desirable for the electrode/
wiring material. That is, reduction of generation
probability of hillock, reduction of generation
15 probability of alloy spike will be accomplished.

This may be considered to be due to the fact
that substantially no or extremely small formation of
alloy spike, etc. on account of the eutectic reaction
with the subbing silicon, etc. is seen, because Al of
20 good quality can be formed on the surface comprising
a semiconductor or an electroconductive member as the
electron-donative surface, and also the Al is
excellent in crystallinity. And, when employed for
the electrode of a semiconductor device, an effect
25 surpassing the concept of the Al electrode which has
been contemplated in the prior art, and could not be
even expected in the prior art can be obtained.

1 Having described above about the fact that the
Al deposited on an electron-donative surface, for
example, within the opening with the semiconductor
substrate surface exposed becomes to have a single
5 crystalline structure, according to the Al-CVD method,
a metal film composed mainly of Al as described below
can be also selectively deposited, and its film
quantity also exhibits excellent characteristics.

For example, in addition to a gas of an
10 alkylaluminum hydride and hydrogen,

a gas containing Si atoms such as SiH_4 , Si_2H_6 ,
 Si_3H_8 , $\text{Si}(\text{CH}_3)_4$, SiCl_4 , SiH_2Cl_2 , SiHCl_3 , or the like,

a gas containing Ti atoms such as TiCl_4 , TiBr_4 ,
 $\text{Ti}(\text{CH}_3)_4$, etc.,

15 a gas containing Cu atoms such as copper
bisacetylacetonate $\text{Cu}(\text{C}_5\text{H}_7\text{O}_2)$, copper
bisdipivaloylmethanite $\text{Cu}(\text{C}_{11}\text{H}_{19}\text{O}_2)_2$, copper
bishexafluoroacetylacetonate $\text{Cu}(\text{C}_5\text{HF}_6\text{O}_2)_2$, etc.,

may be introduced in a preferable combination
20 to form a gas mixture atmosphere, thereby forming an
electrode by selective deposition of an electroconductive
material such as Al-Si, Al-Ti, Al-Cu, Al-Si-Ti, Al-Si-Cu,
etc.

The Al-CVD method as described above is a film
25 forming method excellent in selectivity, and also the
surface characteristic of the film formed has good
surface characteristic. Hence, by application of a

1 non-selective film forming method to the next
deposition step, Al or a metal film composed mainly
of Al can be also formed on the Al film selectively
deposited as described above and SiO_2 , etc. as the
5 insulating film, whereby a preferable metal film
having high useability for general purpose as the
wiring of semiconductor device can be obtained.

Specific examples of such metal film include
the following. There may be included combinations of
10 Al, Al-Si, Al-Ti, Al-Cu, Al-Si-Ti, Al-Si-Cu, etc.
deposited selectively with Al, Al-Si, Al-Ti, Al-Cu,
Al-Si-Ti, Al-Si-Cu, etc.

As the film forming method for non-selective
deposition, there are other CVD methods than the Al-
15 CVD method as described above, the sputtering method,
etc.

(Film forming Apparatus)

Next, a preferable film forming apparatus for
forming the electrode according to the present
20 invention is described.

Fig. 9 to Fig. 11 show schematically a
sequential metal film forming apparatus preferable
for applying the film forming method as described
above.

25 The sequential metal film forming apparatus,
as shown in Fig. 9, is constituted of loadlock chamber
311 connected mutually communicated under shielding

1 from outer air through the gate valves 310a to 310f,
a CVD reaction chamber 312 as the first film forming
chamber, an Rf etching chamber 313, a sputtering chamber
314 as the second film forming chamber and a loadlock
5 chamber 315, and the respective chambers are
constituted reducible in pressure by evacuation with
the evacuation systems 316a to 316e. Here, the above
loadlock chamber 311 is a chamber for replacing the
substrate atmosphere before deposition treatment with
10 H₂ atmosphere after evacuation in order to improve
the throughput characteristic. The next CVD reaction
chamber 312 is a chamber for selective deposition on
the substrate according to the Al-CVD method as
described above under normal pressure or reduced
15 pressure, in which a substrate holder 318 having a
heat-generating member 317 which can heat the
substrate to be formed to a range of 200 °C to 450 °C
is provided internally, and starting gases such as
alkylaluminum hydride bubbled and gasified in the
20 bubbler 319-1 are introduced into the chamber through
the starting gas introducing line 319 for CVD, and
also hydrogen gas as the reactive gas is introduced
through the gasline 319'. The next Rf etching
chamber 313 is a chamber for carrying out cleaning
25 of the substrate surface after selective deposition
(etching) under Ar atmosphere, and internally
thereof are provided at least a substrate holder 320

1 capable of heating the substrate to a range of 100 °C
to 250 °C and an electrode line for Rf etching 321,
and also an Ar gas feeding line 322 is connected. The
next sputtering chamber 314 is a chamber for depositing
5 non-selectively a metal film by sputtering under Ar
atmosphere on the substrate surface, and internally
thereof are provided a substrate holder 323 heated
within a range of 200 °C to 250 °C and a target
electrode 324 for mounting a sputter target material
10 324a, and also an Ar gas feeding line 325 is
connected. The final loadlock chamber 315 is a
control chamber before taking out the substrate after
completion of the metal film deposition into the outer
air, and constituted so that the atmosphere may be
15 replaced with N₂.

Fig. 10 shows another constitutional example
of a sequential metal film forming apparatus preferable
for applying the film forming method as described
above, and the same portions as described above in
20 Fig. 9 are made the same symbols. The difference of
the apparatus in Fig. 10 from that in Fig. 9 resides
in that a halogen lamp 330 is provided as the direct
heating means and the substrate surface can be
directly heated, and for that purpose, the substrate
25 holder 312 is provided with a nail 331 for holding
the substrate under suspended state.

By heating directly the substrate surface

1 with such constitution, the deposition speed can be
further improved as described above.

The sequential metal film forming apparatus
with the above constitution, as shown in Fig. 11, is
5 substantially equivalent to one with the structure
having the above loadlock chamber 311, the CVD
reaction chamber 312, the Rf etching chamber 313, the
sputtering chamber 314, the loadlock chamber 315
connected mutually to one another with the conveying
10 chamber 326 as the relay chamber. With this
constitution, the loadlock chamber 311 functions also
as the loadlock chamber 315. In the above conveying
chamber 326, as shown in the Figure, an arm 327 as
the conveying means reversibly rotatable in the AA
15 direction and stretchable in the BB direction is
provided, and with the arm 327, as shown in the
arrowhead in Fig. 12, the substrate can be moved
following the steps successively from the loadlock
chamber 311 to the CVD chamber 312, the Rf etching
20 chamber 313, the sputtering chamber 314, the loadlock
chamber 315 without exposure to outer air.

(Film Forming Procedure)

The film forming procedure for forming the
electrode and wiring according to the present
25 invention is described.

Fig. 13 is a schematic perspective view for
illustration of the film forming procedure for

1 formation of the electrode and wiring according to the
present invention.

First, the outline is described. A semiconductor
substrate having openings formed on an insulating film
5 is prepared, which substrate is arranged in a film
forming chamber, and its surface is maintained at, for
example, 260 °C to 450 °C to deposit selectively Al
at the portion where the semiconductor is exposed
according to the hot CVD method in a mixed atmosphere
10 of DMAH as the alkylaluminum hydride and hydrogen gas.
Of course, as described above, a metal film composed
mainly of Al such as Al-Si, etc. may be also deposited
selectively by introducing a gas containing Si atoms,
etc. Next, on the Al selectively deposited by the
15 sputtering method and the insulating film, Al or a
metal film composed mainly of Al is non-selectively
formed. Then, by patterning of the metal film non-
selectively deposited to a desired wiring shape,
electrodes and wirings can be formed.

20 Referring next to Fig. 10 and Fig. 13,
description is made in more detail. First, a
substrate is prepared. As the substrate, for
example, a single crystalline Si wafer having an
insulating film provided with openings with
25 respective apertures provided thereon is prepared.

Fig. 13A is a schematic view showing a
part of the substrate. Here, 401 is a single

1 crystalline silicon substrate as a conductive
substrate, 402 a thermally oxidized silicon film as
the insulating film (layer). 403 and 404 are openings
(exposed portions), having apertures different from
5 each other. 410 is the groove bottom with Si exposed.

The procedure for forming Al film which
becomes the electrode as the first wiring layer on
the substrate is as follows with Fig. 10.

First, the substrate as described above is
10 arranged in the loadlock chamber 311. Hydrogen is
introduced into the loadlock chamber 311 to make it
under hydrogen atmosphere. And, the reaction chamber
312 is internally evacuated to approximately 1×10^{-8}
Torr by the evacuation system 316b. However, Al
15 film can be formed even if the vacuum degree within
the reaction chamber 312 may be worse than 1×10^{-8}
Torr.

And, the gas of DMAH bubbled from the gasline
319 is fed. For the carrier gas for the DMAH line,
20 H_2 is employed.

The second gasline 319' is for H_2 as the
reaction gas, and by flowing H_2 through the second gas
line 319' and controlling the opening degree of the
slow leak valve not shown to adjust the pressure
25 within the reaction chamber 312 to a predetermined
value. A typical pressure in this case is preferably
about 1.5 Torr. Through the DMAH line, DMAH is

1 introduced into the reaction tube. The total
pressure is made about 1.5 Torr, and the DMAH pressure
5.0 x 10⁻³ Torr. Then, current is passed to the
halogen lamp 330 to heat directly the wafer. Thus,
5 Al is selectively deposited.

After elapse of a predetermined deposition
time, feeding of DMAH is once stopped. The
predetermined deposition time of the Al film deposited
in this process is the time until the thickness of
10 the Al film on the Si (single crystalline silicon
substrate 1) becomes equal to the film thickness of
the SiO₂ (thermally oxidized silicon film 2), and
can be determined previously by experimentation.

The temperature of the substrate surface by
15 direct heating at this time is made about 270 °C.
According to the steps up to this state, the Al
film 405 is selectively deposited within the openings
and the grooves as shown in Fig. 13B.

All of the steps as described above are
20 referred to as the first film forming step for
formation of electrode within contact hole.

After the above first film forming step, the
CVD reaction chamber 312 is evacuated until reaching
a vacuum degree of 5 x 10⁻³ Torr or lower by the
25 evacuation system 316b. At the same time, the Rf
etching chamber 313 is evacuated to 5 x 10⁻⁶ Torr
or lower. After confirmation that the both chambers

1 have reached the above vacuum degree, the gate valve
310c is opened, the substrate moved from the CVD
reaction chamber 312 to the Rf etching chamber 313 by
the conveying means, and the gate valve 310c closed.

5 The substrate is conveyed to the Rf etching chamber 313,
and the Rf etching chamber 313 is evacuated by means
of the evacuation system 316c until reaching a vacuum
degree of 10^{-6} Torr or lower. Then, argon is fed
through the argon feeding line 322 for Rf etching, and

10 the Rf etching chamber 313 maintained under an argon
atmosphere of 10^{-1} to 10^{-3} Torr. The substrate holder
320 of Rf etching is maintained at about 200°C, Rf
power of 100 W supplied to the electrode for Rf etching
321 for about 60 seconds, and discharging of argon is

15 caused to occur within the Rf etching chamber 313
for about 60 seconds. By doing so, the surface of
the substrate can be etched with argon ions to remove
unnecessary surface layer of the CVD deposited film.
The etching depth in this case is made about 100 Å

20 in terms of the oxide. Here, surface etching of the
CVD deposited film is effected in the Rf etching
chamber, but since the surface layer of the CVD
film of the substrate conveyed through vacuum contains
no oxygen, etc., no Rf etching may be effected. In

25 that case, the Rf etching chamber 313 function as
the temperature changing chamber for effecting
temperature change within a short time, when the

1 temperatures in the CVD reaction chamber 12 and the
sputtering chamber 314 are greatly different.

In the RF etching chamber 313, after completion
of Rf etching, flowing of argon is stopped, and the
5 argon within the Rf etching chamber 313 is evacuated.
After the Rf etching chamber 313 is evacuated to 5×10^{-6}
 10^{-6} Torr and the sputtering chamber 314 to 5×10^{-6}
Torr or lower, the gate valve 310d is opened. Then,
the substrate is moved from the Rf etching chamber 313
10 to the sputtering chamber 314 by means of a conveying
means, followed by closing of the gate valve 310d.

After the substrate is conveyed to the
sputtering chamber 314, the sputtering chamber 314 is
made under an argon atmosphere of 10^{-1} to 10^{-3} Torr
15 similarly as in the Rf etching chamber 313, and the
temperature of the substrate holder 323 for mounting
the substrate set to about 200 to 250°C. And
discharging of argon is effected at a DC power of
5 to 10 kw to cut a target material such as Al or
20 Al-Si (Si: 0.5%) and effect film formation of a metal
such as Al, Al-Si, etc. at a deposition speed of about
10000 Å/min. on the substrate. This step is a non-
selective deposition step. This is called the second
film forming step for formation of the wiring to be
25 connected to the electrode.

After formation of a metal film of about 5000 Å,
flowing of argon and application of DC power are stopped.

1 After evacuation of the loadlock chamber 311 to 5×10^{-3} Torr or lower, the gate valve 310e is opened and the substrate moved. After the gate valve 310e is closed, N_2 gas is permitted to flow into the loadlock
5 chamber 311 until reaching atmospheric pressure, the gate valve 310f opened and the substrate taken out of the apparatus.

According to the second Al film deposition step as described above, the Al film 406 can be formed
10 on the SiO_2 film 402 as shown in Fig. 13C.

And, by patterning the Al film 406 as shown in Fig. 13D, a wiring with a desired shape can be obtained.

(Experimental Examples)

15 In the following, how excellent is the above-described Al-CVD method is and how good of the quality the Al film deposited within the openings is are described based on the experimental results.

First, as the substrate, a plurality of N-type
20 single crystalline silicon wafers were prepared, which are thermally oxidized on the surface to form SiO_2 of 8000 Å, and have various openings with various apertures from $0.25 \mu m \times 0.25 \mu m$ square to $100 \mu m \times 100 \mu m$ square patterned to have the subbing Si single crystal
25 exposed (Sample 1-1).

These are subjected to formation of Al films according to the Al-CVD method under the conditions as

1 described below. Under the common conditions by use
of DMAH as the starting gas, and hydrogen as the
reaction gas, a total pressure of 1.5 Torr, a DMAH
partial pressure of 5.0×10^{-3} Torr, the power amount
5 passed through the halogen lamp is adjusted and the
substrate surface temperature set within the range
of 200°C to 490°C to form films.

The results are shown in Table 1.

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1 As can be seen from Table 1, at a substrate
surface temperature by direct heating of 260 °C or
higher, Al is deposited selectively at a high deposition
speed of 3000 to 5000 Å/min. within the openings.

5 When the characteristics of the Al film within
the openings at substrate surface temperature range
of 260 °C to 440 °C are examined, they are found to be
excellent such that no carbon is contained, with
resistivity being 2.8 to 3.4 μΩcm, reflectance 90 to
10 95%, hillock density of 1 μm or higher 0 to 10 and
substantially no spike generation (destruction probability
of 0.15 μm junction).

 In contrast, at substrate surface temperatures
of 200 °C to 250 °C, the film is found to be
15 considerably good as compared with the prior art
although the film quality is slightly worse as
compared with the case of 260 °C to 440 °C, but the
deposition speed is 1000 to 1500 Å/min., which can
never be said to be sufficiently high.

20 When the substrate surface temperature becomes
450 °C or higher, the characteristics of the Al film
with the openings are lowered with the reflectance
becoming 60% or less, hillock density of 1 μm or more
10 to 10⁴ cm⁻², alloy spike generation 0 to 30%.

25 Next, description is made about how suitably
the method as described above can be used openings
such as contact hole or thru-hole.

1 That is, it can be also preferably applied to
the contact hole/thru-hole structure comprising the
material as described below.

5 On the sample 1-1 as described above, an Al
film is formed on a substrate (sample) as described
below under the same conditions as when the Al film is
formed.

10 On a single crystalline silicon as the first
substrate surface material is formed a silicon oxide
film according to the CVD method as the second
substrate surface material, and patterning effected
according to the photolithographic steps to have the
single crystalline silicon surface partially exposed.

15 The film thickness of the thermally oxidized
 SiO_2 film has a film thickness of $8000\text{\AA}$, the exposed
portion of the single crystalline silicon a size of
 $0.25\text{ }\mu\text{m} \times 0.25\text{ }\mu\text{m}$ to $100\text{ }\mu\text{m} \times 100\text{ }\mu\text{m}$. Thus, sample
1-2 is prepared (hereinafter such samples are
represented as "CVD SiO_2 (hereinafter abbreviated as
20 SiO_2 /single crystalline silicon")

Sample 1-3 is boron doped oxide film formed
by normal pressure CVD (hereinafter abbreviated as
BSG)/single crystalline silicon,

25 sample 1-4 phosphorus doped oxide film formed
by normal pressure CVD (hereinafter abbreviated as
PSG)/single crystalline silicon,

sample 1-5 phosphorus and boron doped oxide

1 film formed by normal pressure CVD (hereinafter
abbreviated as BSPG)/single crystalline silicon,

sample 1-6 nitride film formed by plasma CVD
(hereinafter abbreviates as P-SiN)/single crystalline
5 silicon,

sample 1-7 hot nitride film (hereinafter
abbreviated as T-SiN)/single crystalline silicon,

sample 1-8 nitride film formed by low pressure
CVD (hereinafter abbreviated as LP-SiN)/single
10 crystalline silicon,

sample 1-9 nitride film formed by means of an
ECR apparatus (hereinafter abbreviated as ECR-SiN)/
single crystalline silicon.

Further, according to all combinations of the
15 first substrate surface materials (18 kinds) and the
second substrate surface materials (9 kinds), samples
1-11 to 1-179 (note: sample Nos. 1-10, 20, 30, 40, 50,
60, 70, 80, 90, 100, 110, 120, 130, 140, 150, 160,
170 are lacking) are prepared. As the first substrate
20 surface material, single crystalline silicon (single
crystalline Si), polycrystalline silicon
(polycrystalline Si), amorphous silicon (amorphous
Si), tungsten (W), molybdenum (Mo), tantalum (Ta),
tungsten silicide (WSi), titanium silicide (TiSi),
25 aluminum (Al), aluminum silicon (Al-Si), titanium
aluminum (Al-Ti), titanium nitride (Ti-N), copper (Cu),
aluminum silicon copper (Al-Si-Cu), aluminum palladium

1 (Al-Pd), titanium (Ti), molybdenum silicide (Mo-Si),
tantalum silicide (Ta-Si) are employed. As the second
substrate surface material, T-SiO₂, SiO₂, BSG, PSG, BPSG,
P-SiN, T-SiN, LP-SiN, ECR-SiN are employed. For all
5 of the samples as described above, good Al films
comparable with the sample 1-1 could be formed.

Next, on the substrate having Al deposited
selectively as described above, Al is deposited non-
selectively according to the sputtering method as
10 described above, followed by patterning.

As the result, the Al film formed according
to the sputtering method, and the Al film selectively
selected within the openings are found to be under
the contact state with both electrically and mechanically
15 high durability due to good surface characteristic of
the Al film.

20

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1 CLAIMS:

 1. A semiconductor device including a
bipolar transistor, having a collector region including
a first semiconductor region of the first
5 electroconduction type and a second semiconductor
region of the first electroconduction type having
higher resistance than said first semiconductor region,
a base region including a semiconductor region of the
second electroconduction type, and an emitter region
10 including a semiconductor region of the first
electroconduction type, said device comprising a metal
layer region for connecting said first semiconductor
region and the collector electrode on said collector
region provided within said second semiconductor
15 region layer of said collector region.

 2. A semiconductor device according to Claim
1, wherein said collector region is formed on a third
semiconductor region of the second electroconduction
20 type different from said first electroconduction
type, and surrounded with a fourth semiconductor
region of the second electroconduction type having
higher resistance than said third semiconductor region,
said fourth semiconductor region comprising a second
25 metal layer region for connecting the electrode on
said semiconductor region and said third semiconductor
region provided therein.





1 3. A semiconductor device according to Claim
1 or 2, wherein said metal layer region is integrally
formed with said collector electrode.

5 4. A semiconductor device according to Claim
2 or 3, wherein said second metal layer region is
formed integrally formed with said electrode.

10 5. A semiconductor device according to any
one of Claims 1 to 4, wherein said metal layer region
is formed of a single crystalline aluminum.

15 6. A semiconductor device according to any
one of Claims 1 to 5, wherein said second metal layer
region is formed of a single crystalline aluminum.

20 7. A semiconductor device having a
semiconductor electrode region comprising a semiconductor
of the first electroconduction type provided internally
of a semiconductor substrate, an electrode provided on
one surface of said semiconductor substrate, and a metal
electrode region provided internally of said
semiconductor substrate for connecting said semiconductor
electrode region and said electrode.

25

8. A semiconductor device according to Claim
7, wherein an insulation film is provided around said





1 metal electrode region.

9. A semiconductor device according to Claim
7 or 8, wherein said metal electrode region is a
5 collector electrode of a bipolar electrode.

10. A semiconductor device according to Claim
7 or 8, wherein said metal electrode region is a source
or drain electrode of the insulation gate type
10 transistor.

11. A semiconductor device according to Claim
7 or 8, wherein said metal region is a gate electrode
of electrostatic induction transistor.

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* C L M S *

ABSTRACT

1 SEMICONDUCTOR DEVICE WITH BURIED ELECTRODE

A semiconductor device including a bipolar transistor, has a collector region including a first semiconductor region of the first electroconduction type and a second semiconductor region of the first electroconduction type having higher resistance than the first semiconductor region, a base region including a semiconductor region of the second electroconduction type, and an emitter region including a semiconductor region of the first electroconduction type. The semiconductor device further comprises a metal layer region for connecting the first semiconductor region and the collector electrode on the collector region provided within the second semiconductor region layer of the collector region.

20

This Sheet Has Been Replaced



25



FIG. 1 PRIOR ART

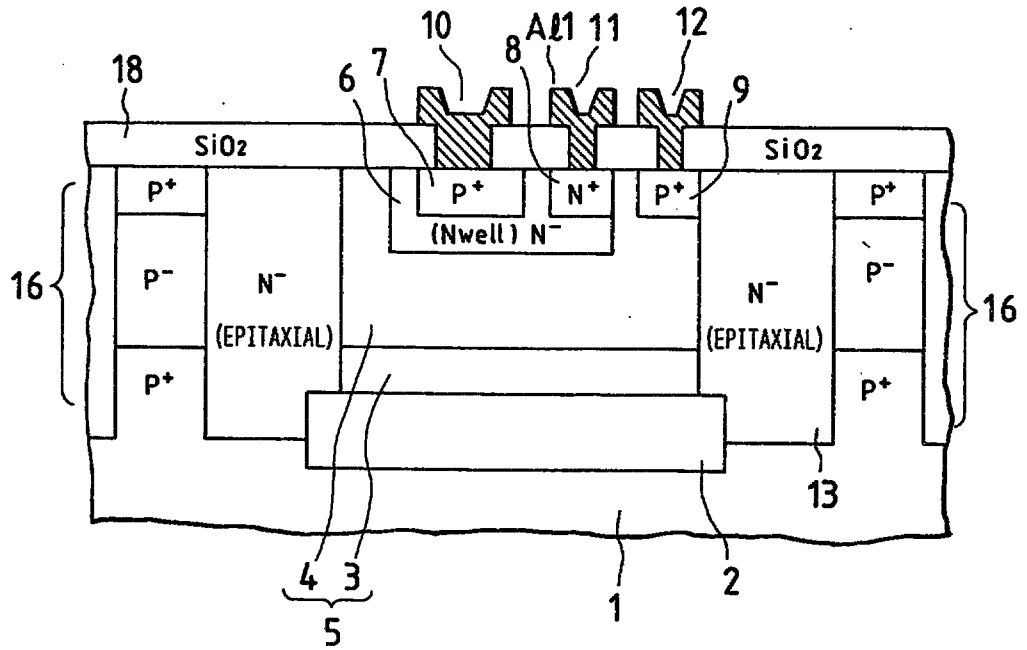


FIG. 2 PRIOR ART

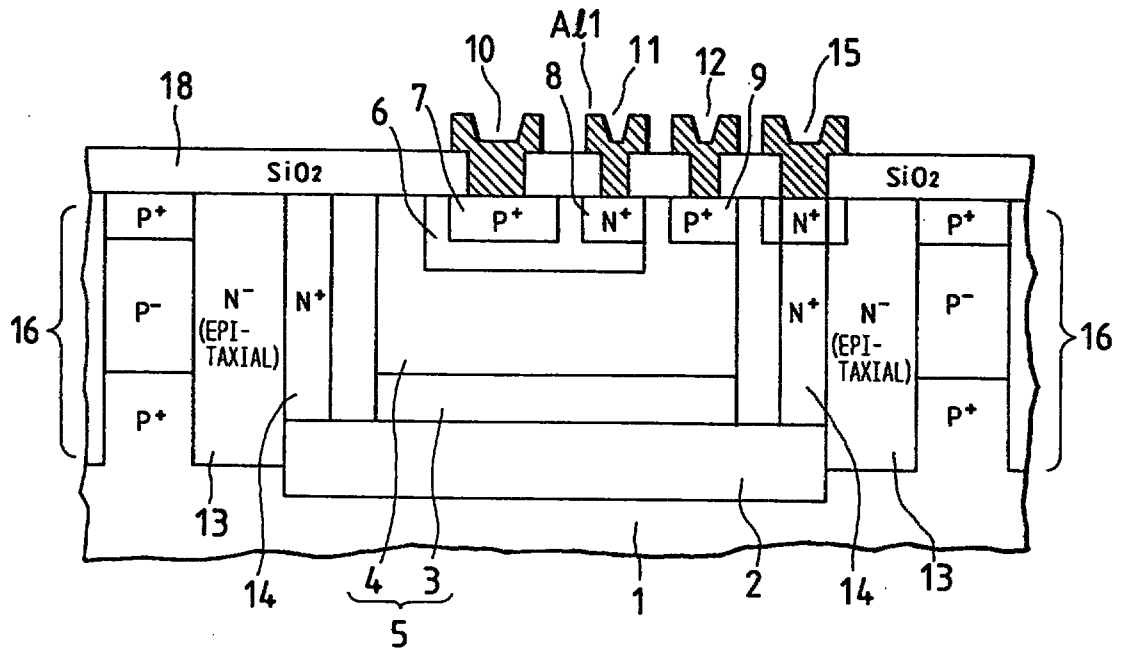




FIG. 3

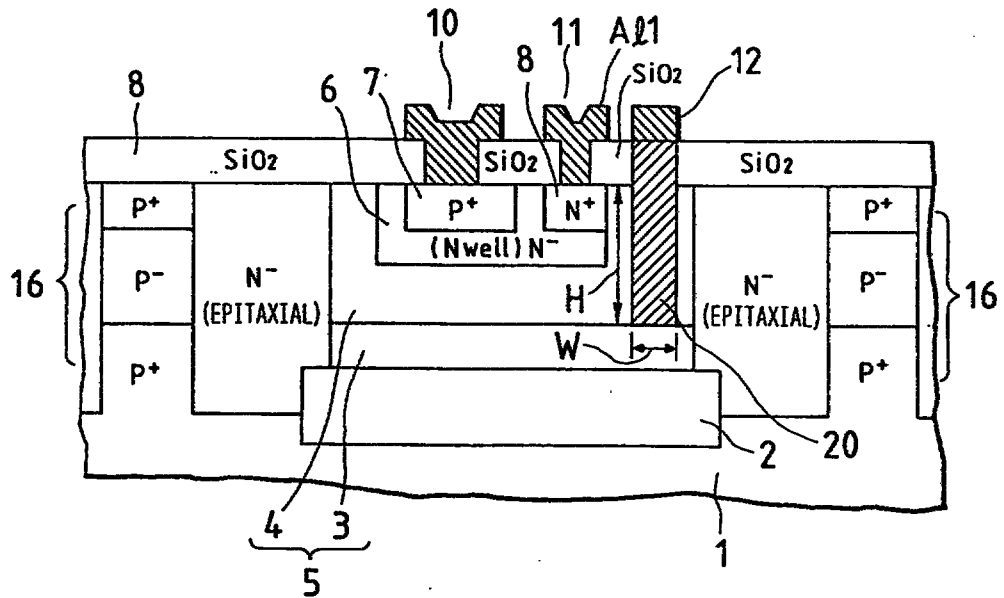


FIG. 5

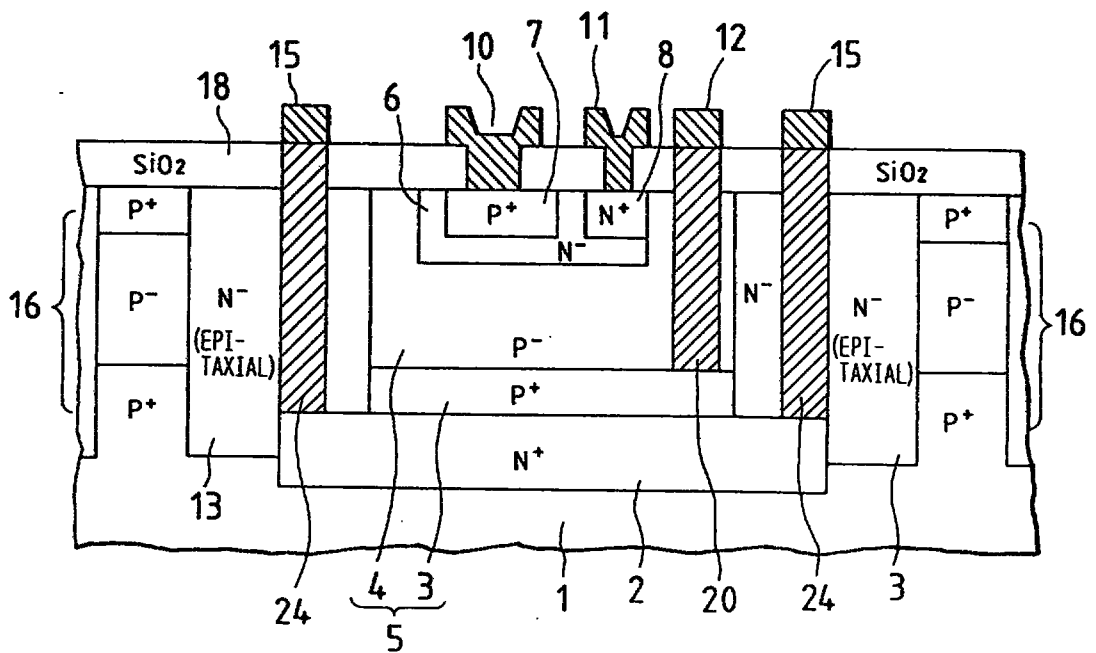




FIG. 4A

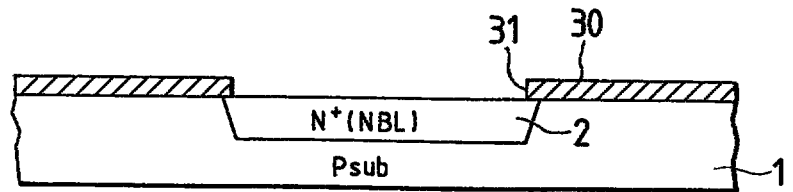


FIG. 4B

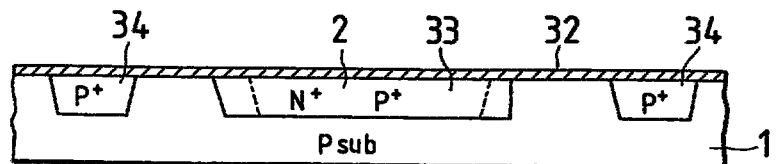


FIG. 4C

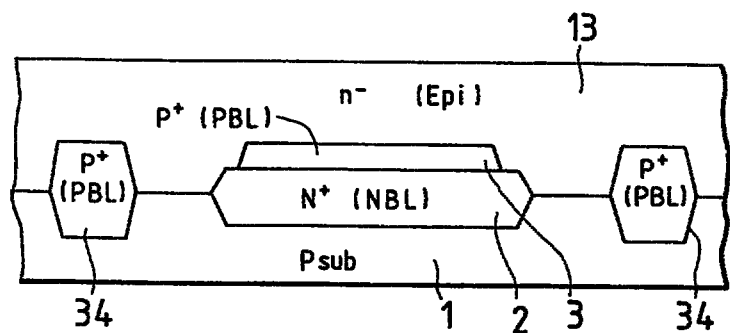


FIG. 4D

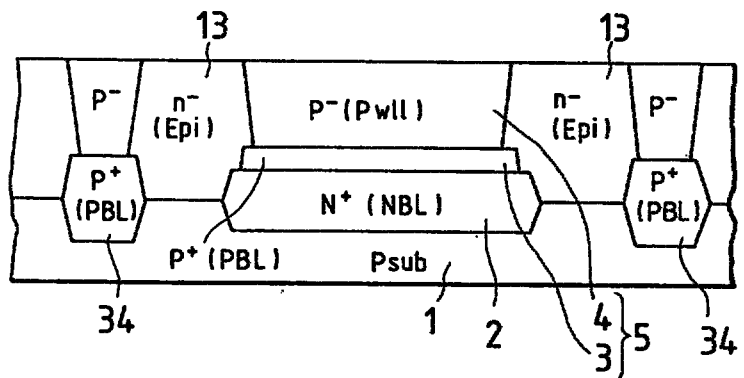


FIG. 4E

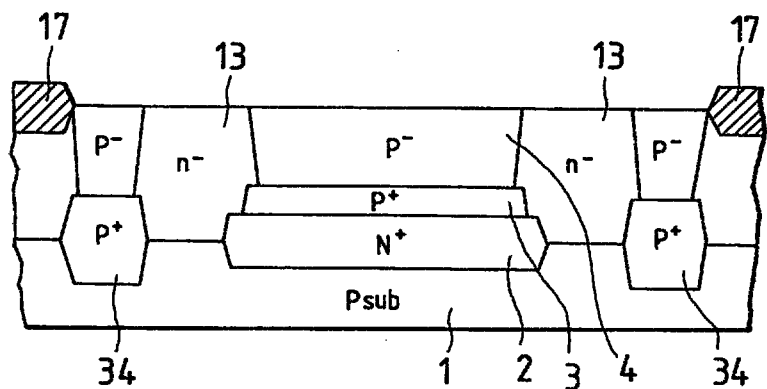




FIG. 4F

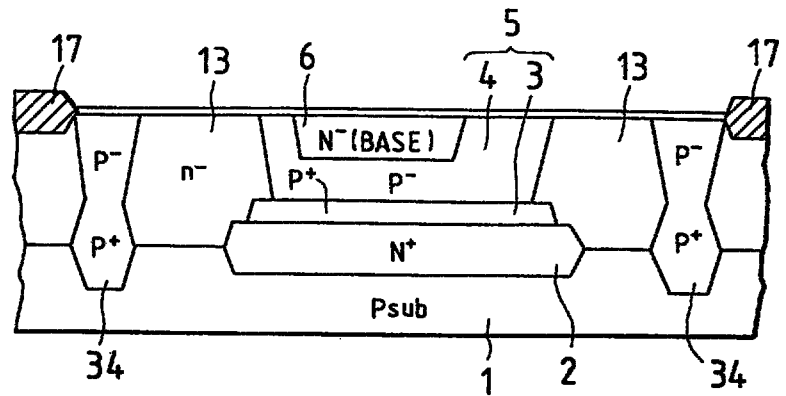


FIG. 4G

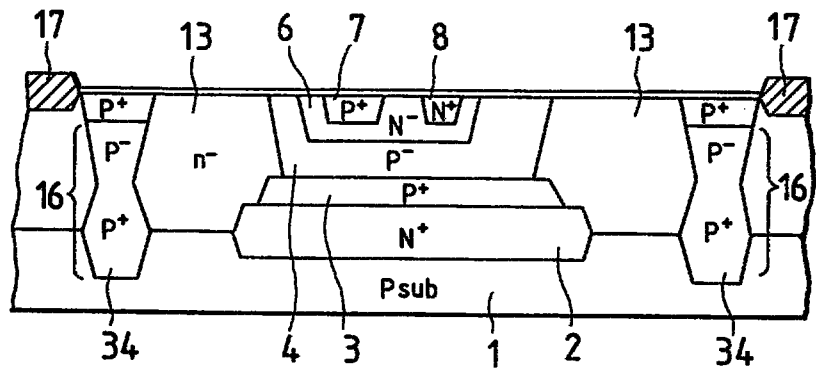


FIG. 4H

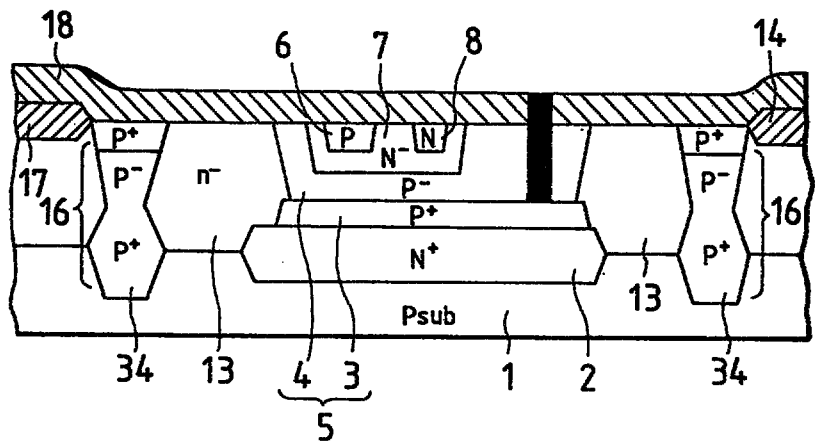


FIG. 4I

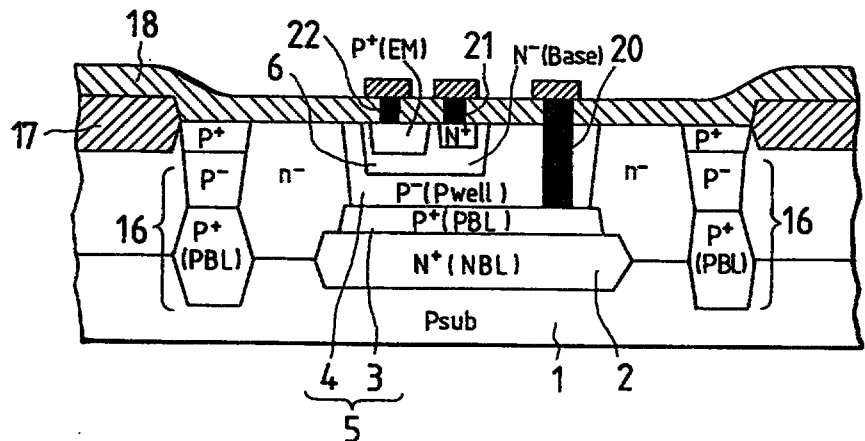




FIG. 6

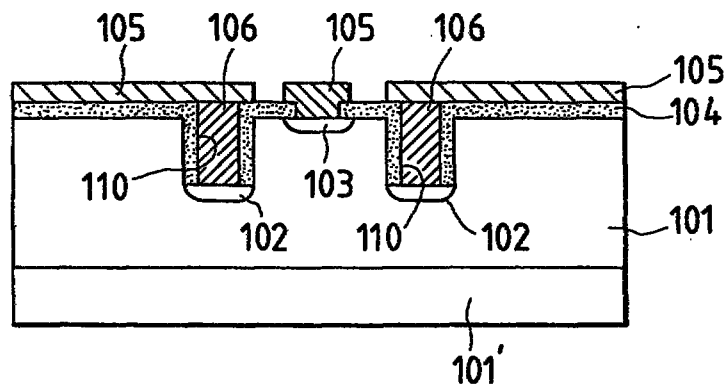


FIG. 8

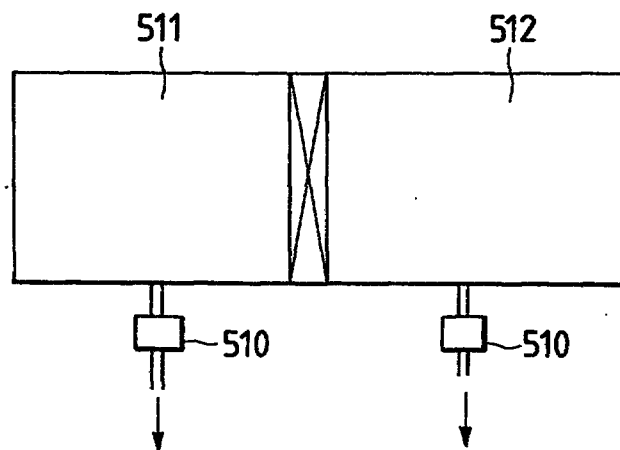




FIG. 7A

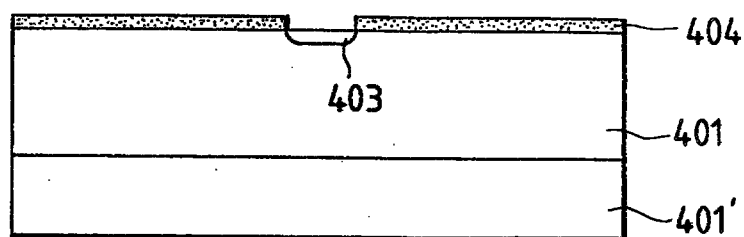


FIG. 7B

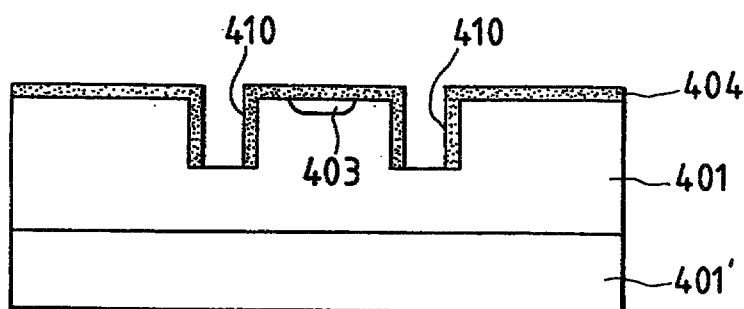


FIG. 7C

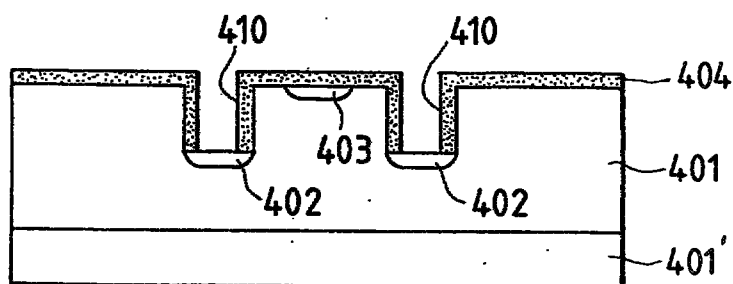


FIG. 7D

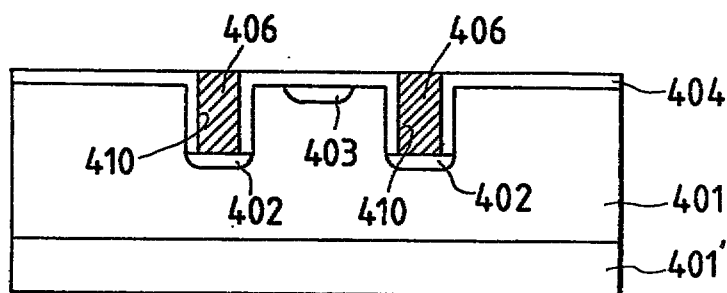
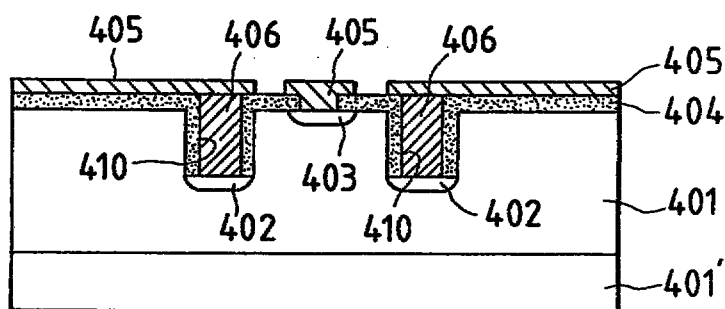


FIG. 7E



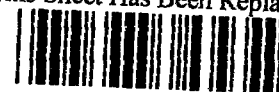


FIG. 9

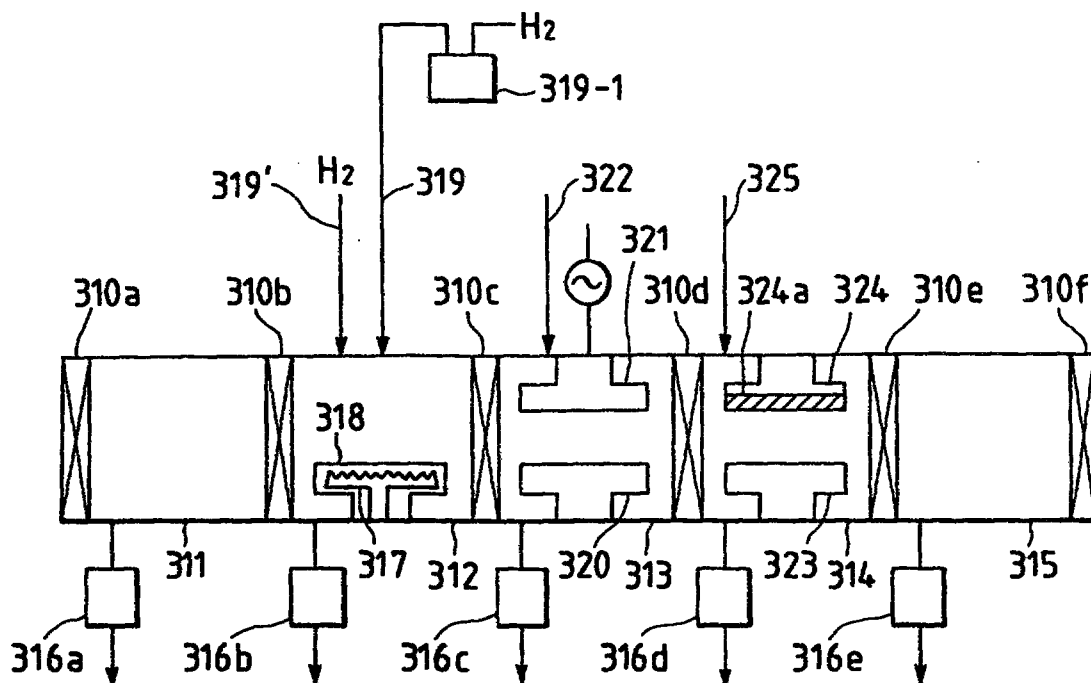


FIG. 10

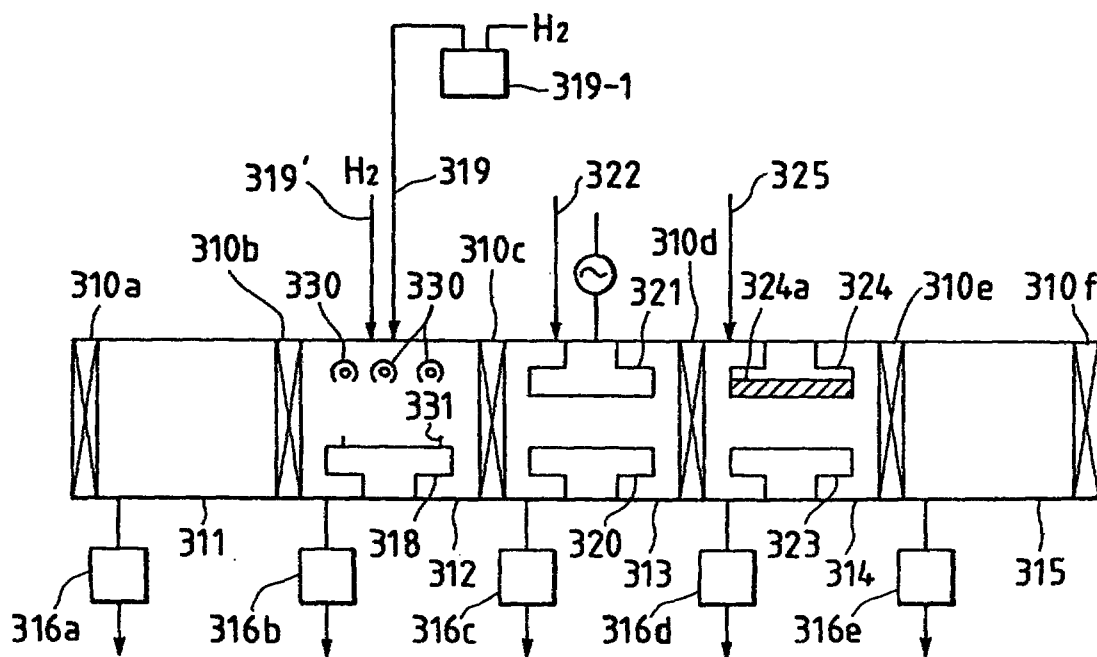




FIG. 11

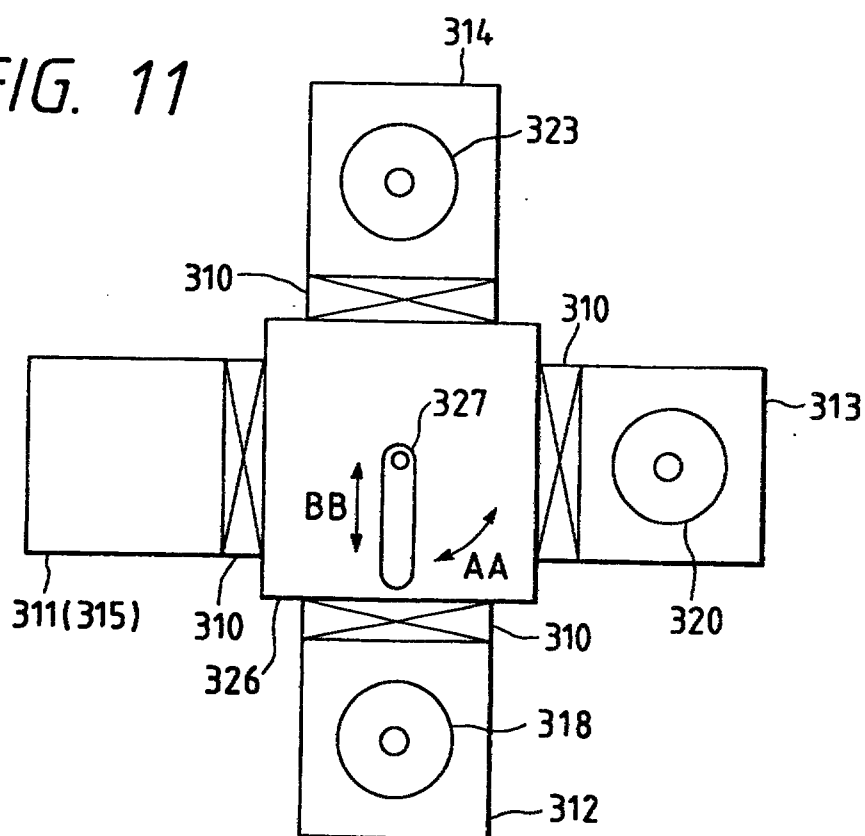
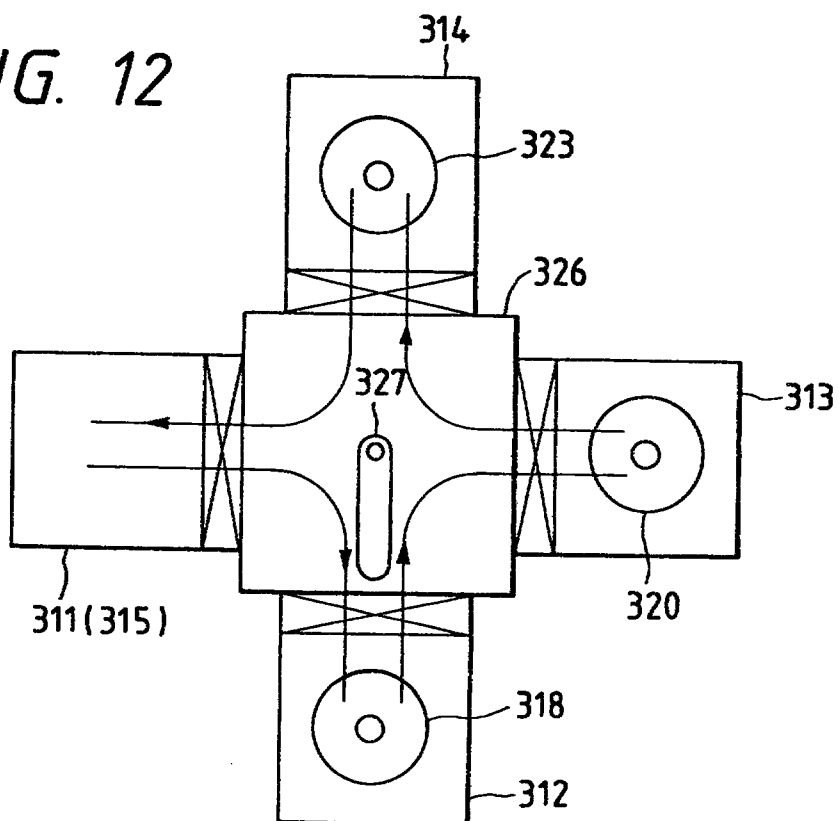


FIG. 12



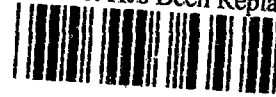


FIG. 13A

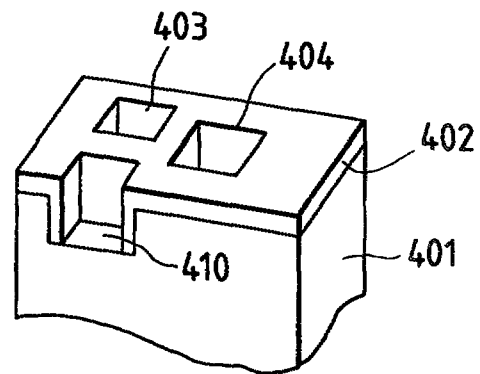


FIG. 13B

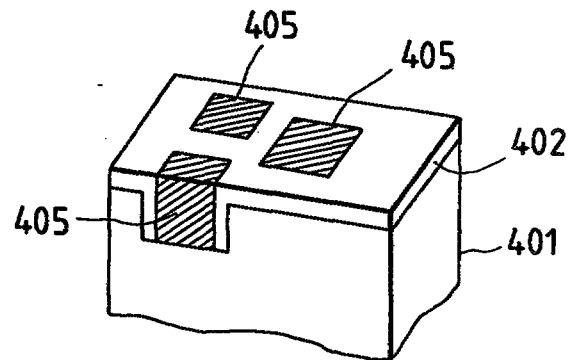


FIG. 13C

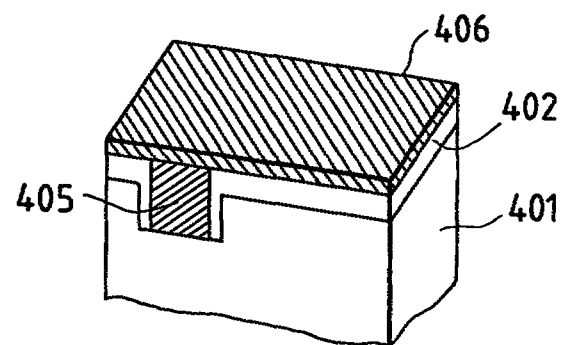
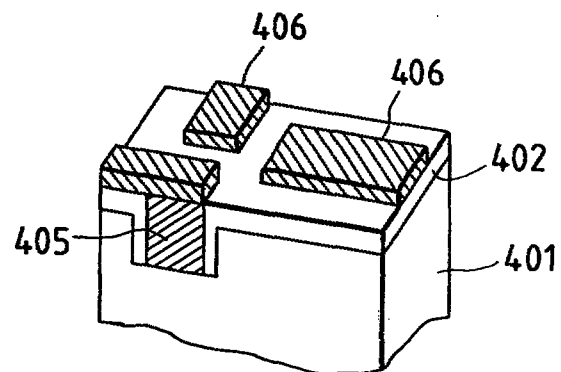


FIG. 13D



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SEMICONDUCTOR DEVICE WITH BURIED ELECTRODE1 ABSTRACT OF THE DISCLOSURE

A semiconductor device including a bipolar transistor, has a collector region including a first semiconductor region of the first electroconduction type and a second semiconductor region of the first electroconduction type having higher resistance than the first semiconductor region, a base region including a semiconductor region of the second electroconduction type, and an emitter region including a semiconductor region of the first electroconduction type. The semiconductor device further comprises a metal layer region for connecting the first semiconductor region and the collector electrode on the collector region provided within the second semiconductor region layer of the collector region.

FIGURE 3

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Date: 13 DEC 1996

FIG. 3

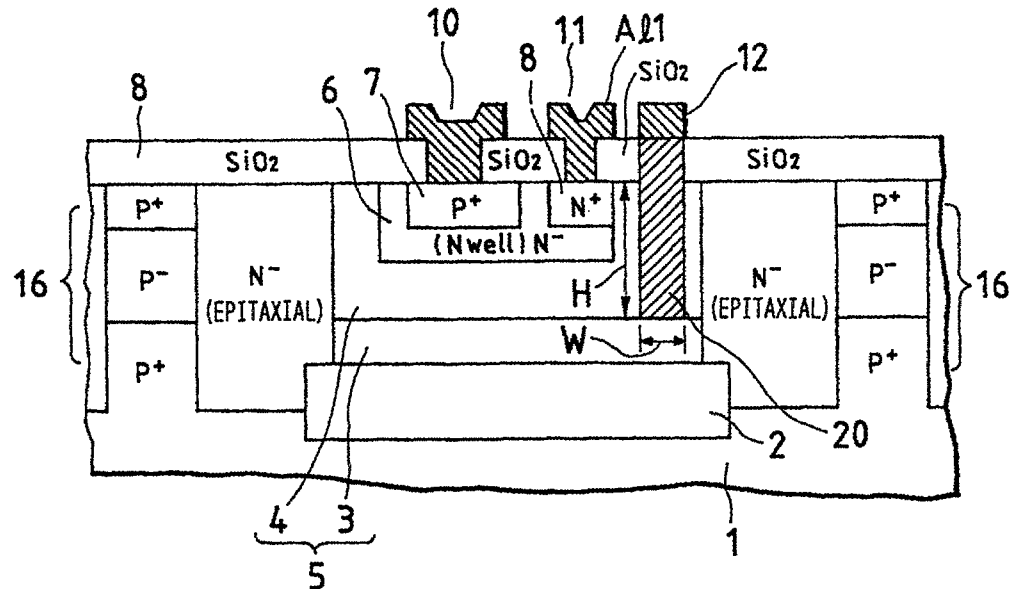
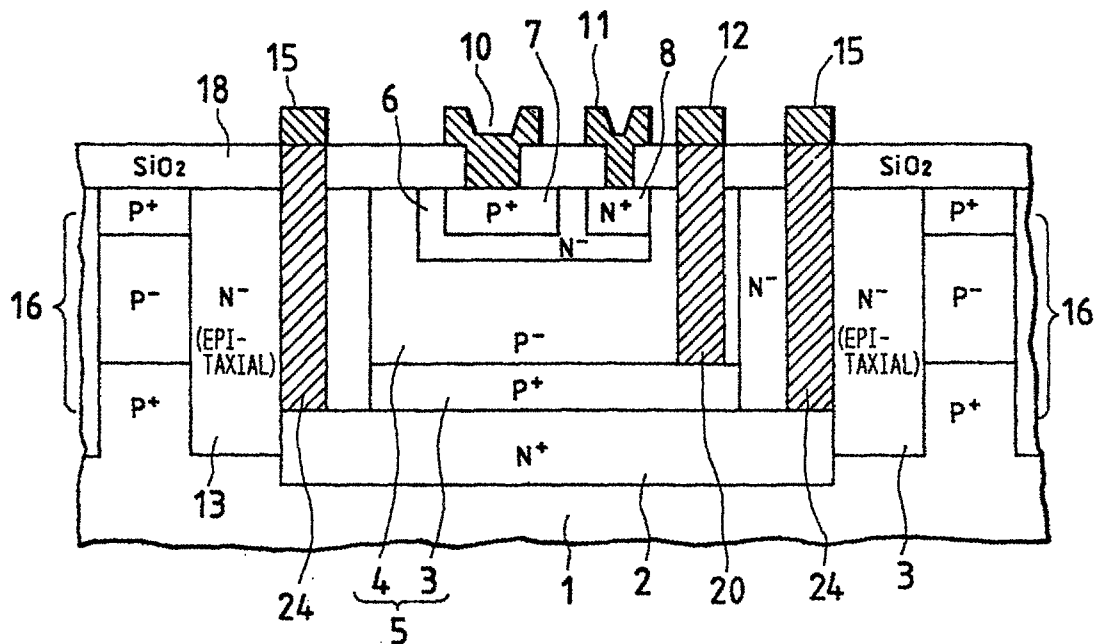


FIG. 5



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FIG. 4A

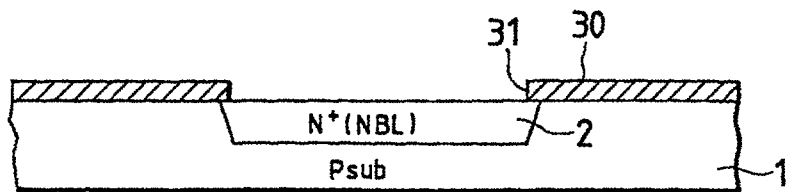


FIG. 4B

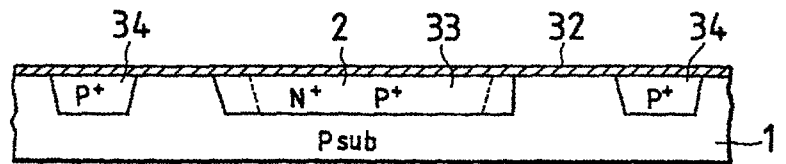


FIG. 4C

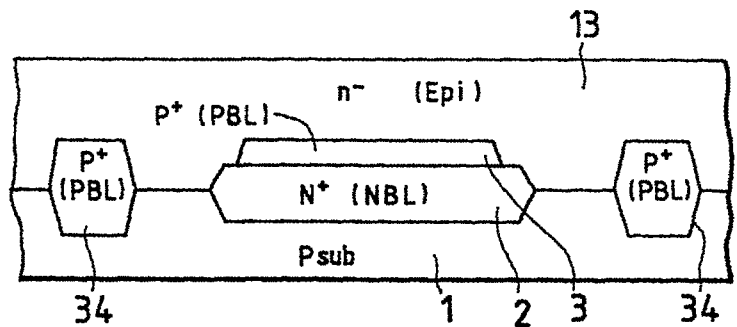


FIG. 4D

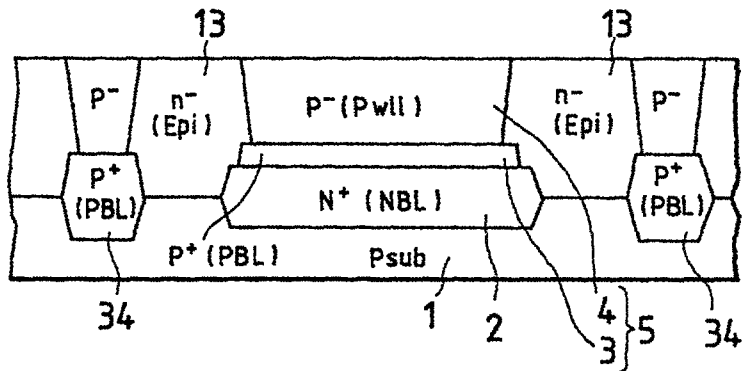


FIG. 4E

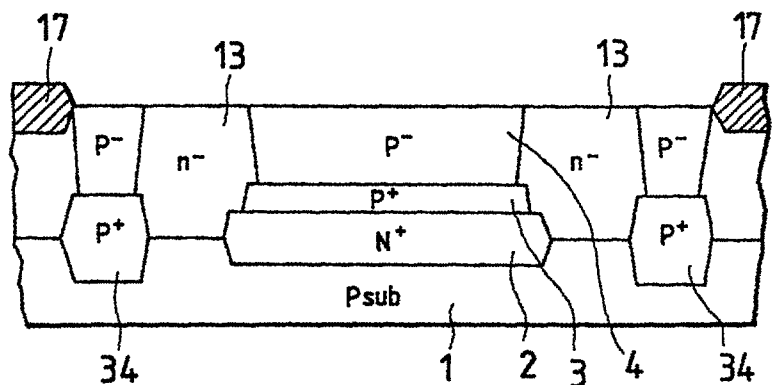


FIG. 4F

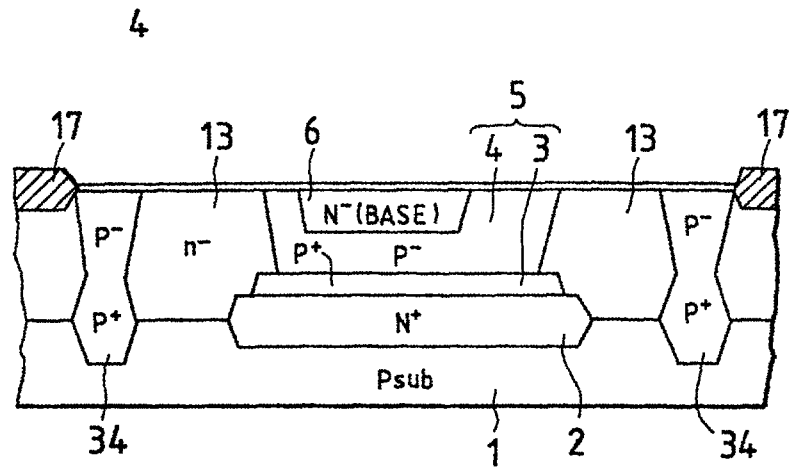


FIG. 4G

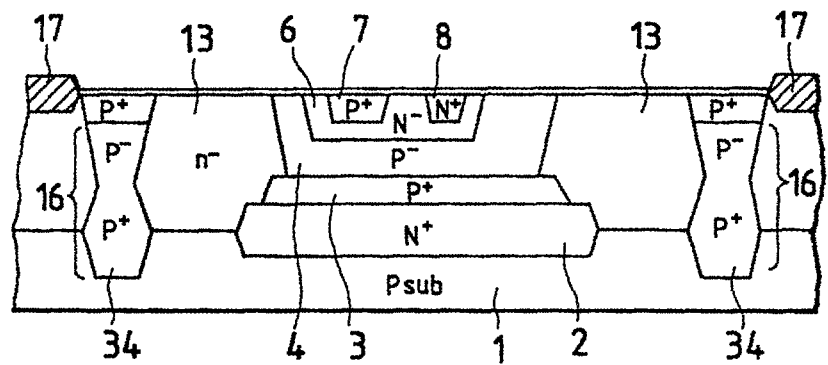


FIG. 4H

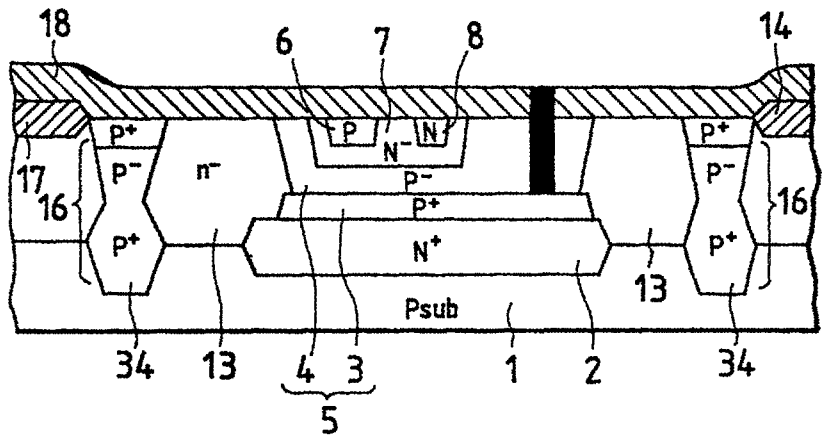
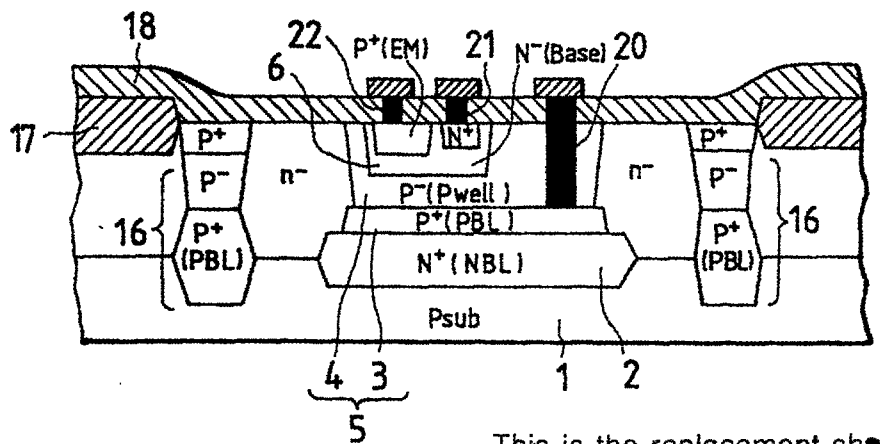
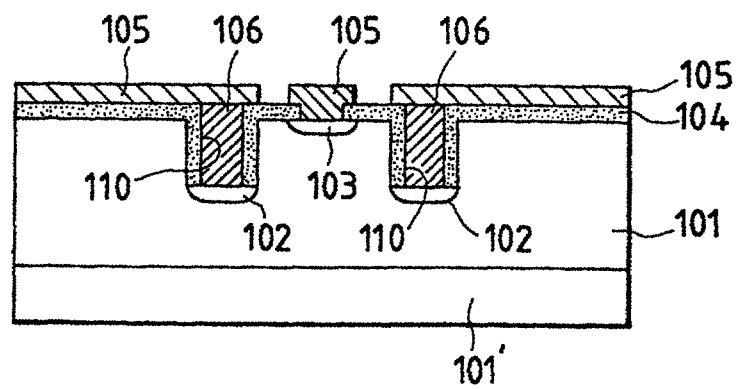
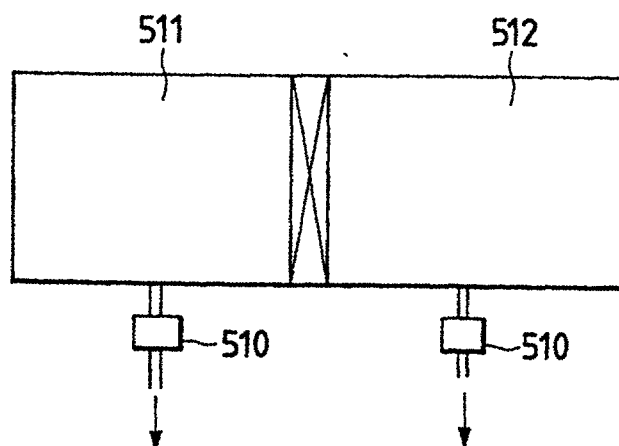


FIG. 4I



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FIG. 6*FIG. 8*

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Date: 13 DEC 1996

FIG. 7A

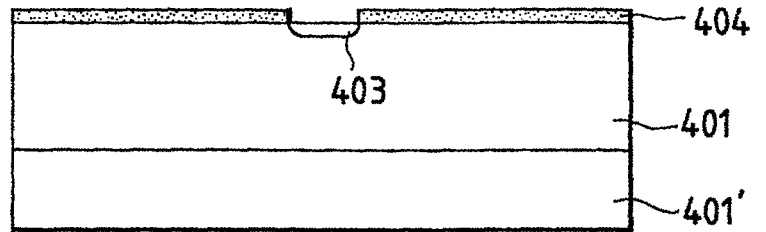


FIG. 7B

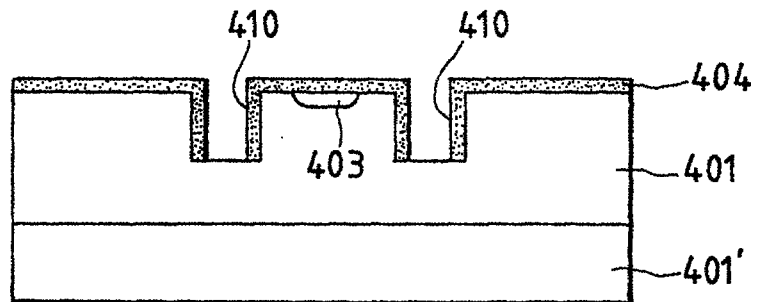


FIG. 7C

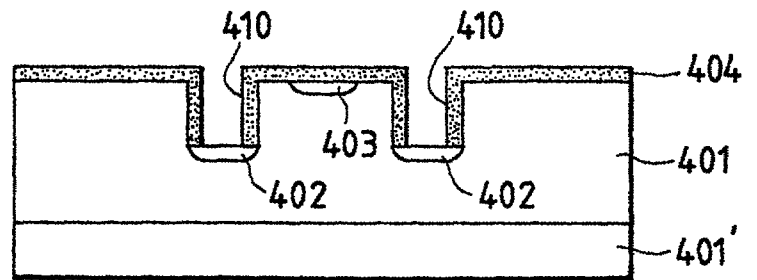


FIG. 7D

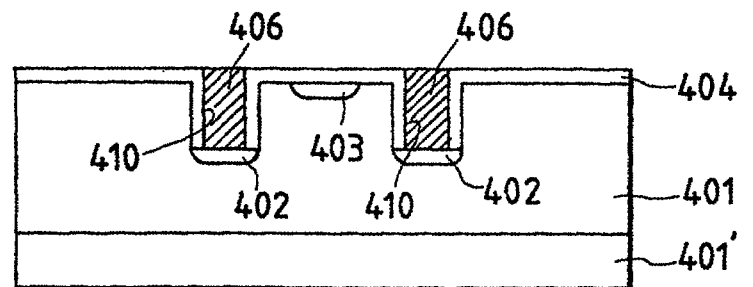
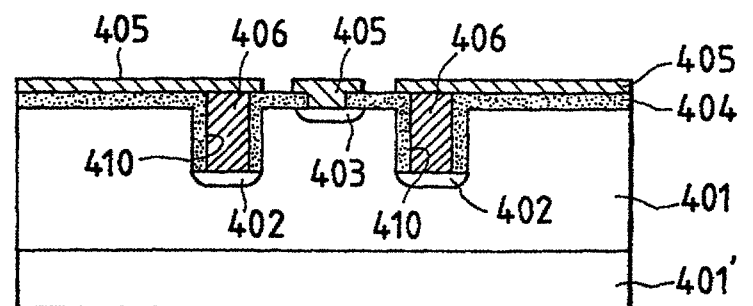


FIG. 7E



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Date: 13 DEC 1996

FIG. 9

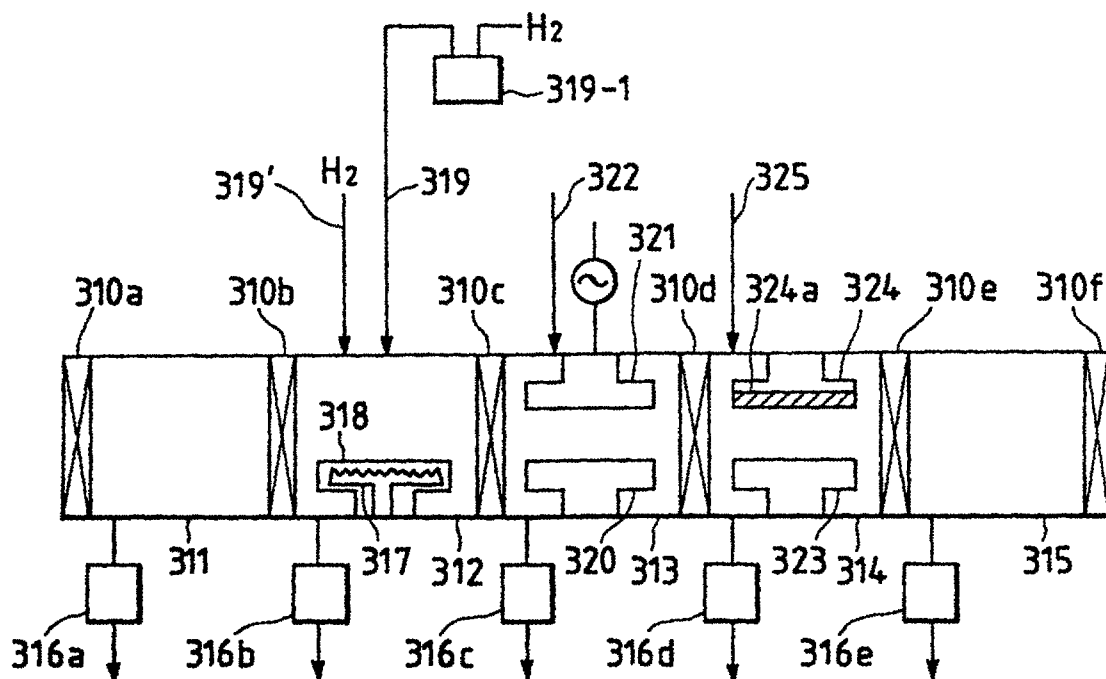
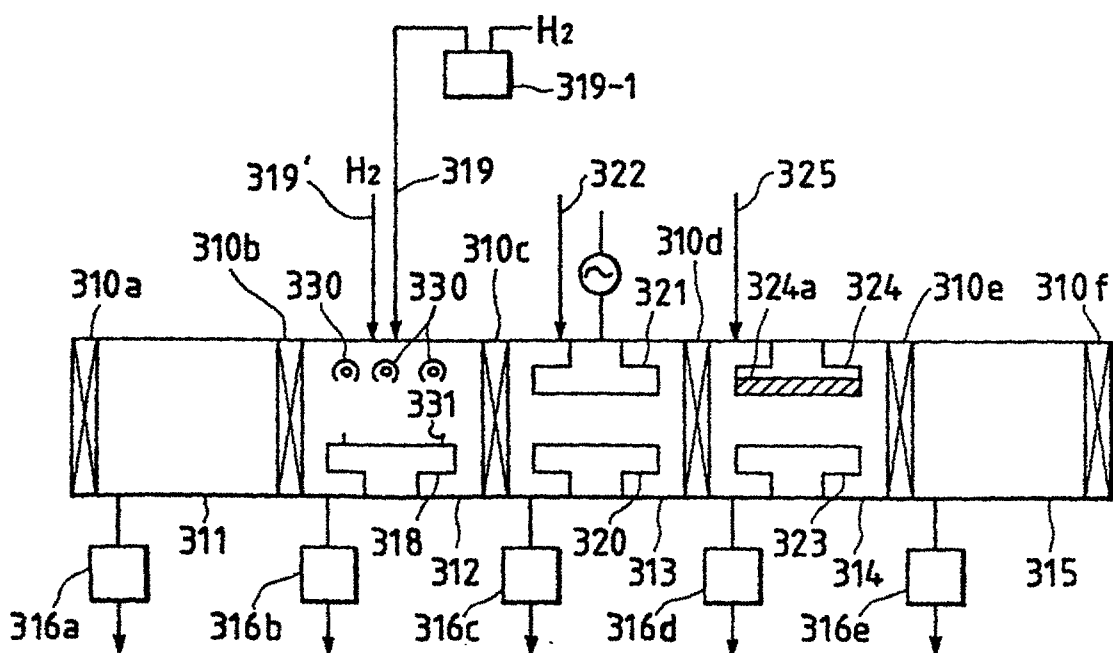


FIG. 10



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FIG. 11

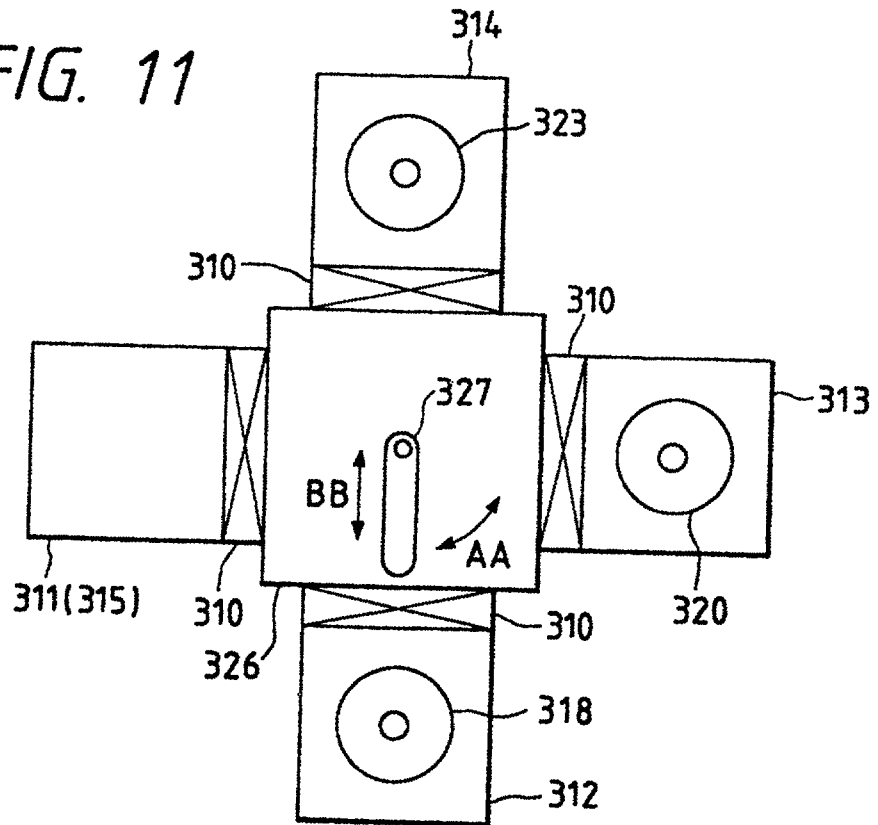


FIG. 12

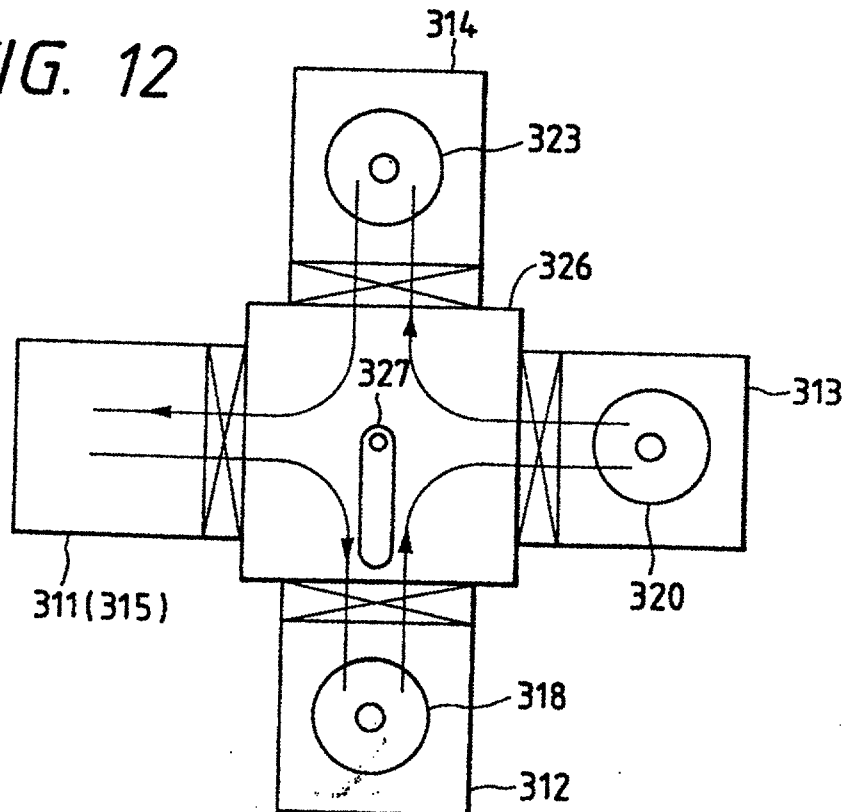


FIG. 13A

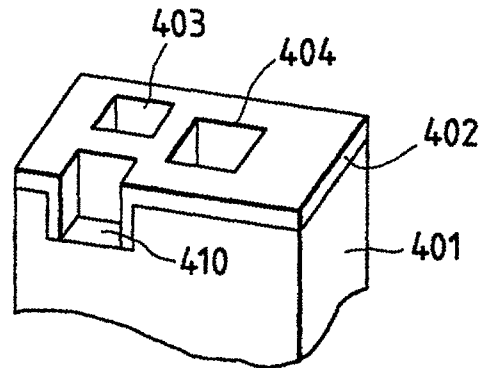


FIG. 13B

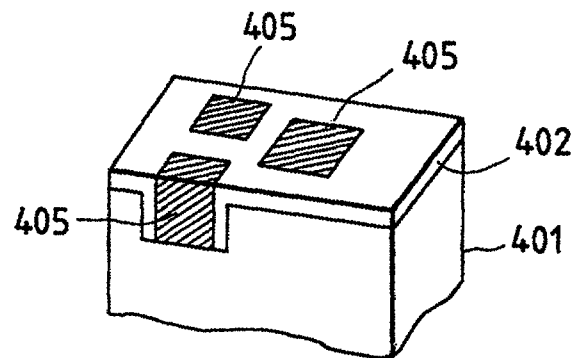


FIG. 13C

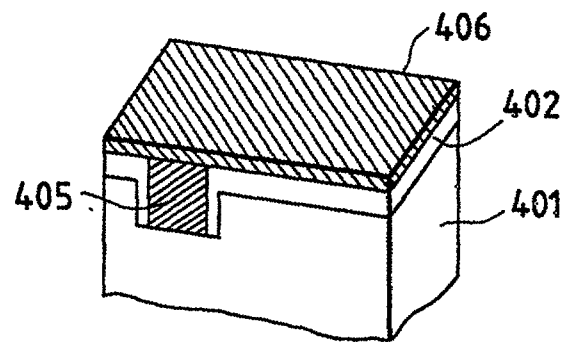
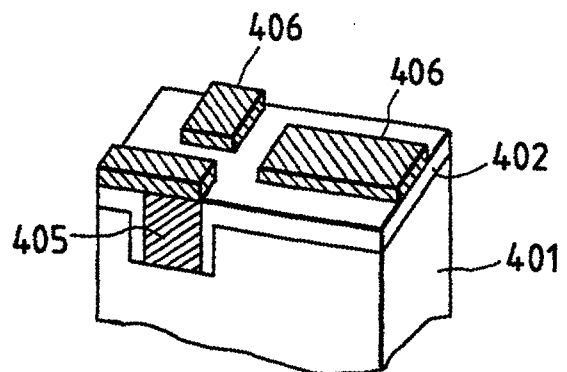


FIG. 13D



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Date: 13 DEC 1996

REPLACEMENT SHEET

We claim:

1. An electrostatic induction transistor comprising:
 - a first semiconductor region of a first conductivity type;
 - a second semiconductor region of said first conductivity type having higher resistance than said first semiconductor region and being disposed over said first semiconductor region;
 - an electrode disposed on a surface of said second semiconductor region; and
 - a metallic region disposed within said second semiconductor region so as to form a gate electrode by connecting a third semiconductor region of a second conductivity type buried in said second semiconductor region and said electrode through said second semiconductor region,wherein said metallic region is formed of single-crystalline aluminum.

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SEMICONDUCTOR DEVICE WITH BURIED ELECTRODE

REPLACEMENT SHEET

ABSTRACT OF THE DISCLOSURE

A semiconductor device including a bipolar transistor, has a collector region including a first semiconductor region of the first electroconduction type and a second semiconductor region of the first electroconduction type having higher resistance than the first semiconductor region, a base region including a semiconductor region of the second electroconduction type, and an emitter region including a semiconductor region of the first electroconduction type. The semiconductor device further comprises a metal layer region for connecting the first semiconductor region and the collector electrode on the collector region provided within the second semiconductor region layer of the collector region.

FIGURE 3

This is the replacement sheet

Date 27 SEP 1997