159159

G00002

Description

Electronic device as multichip module and method for producing it

The invention relates to an electronic device as multichip module, a leadframe arranged in the electronic device, and a panel having a plurality of leadframe positions, and also to a method for producing the electronic device.

An obstacle to the increasing miniaturization of integrated circuits is the required dimensions of passive components, such as coils and capacitors, since they take up a comparatively large semiconductor chip area. Moreover, design variants and degrees of freedom of design are considerably restricted by the requirement to arrange contact areas on the chips either in their edge regions or in a respective central region. When a plurality of semiconductor chips are combined to form a module assembly, the chip design is extremely complex on account of said requirement. If two semiconductor chips are intended to be wired together, then it ranges from difficult to impossible to coordinate their chip designs exactly with one another, especially if the semiconductor chips originate from different suppliers. Furthermore, it

is often necessary to provide a plurality of contact areas for the supply of semiconductor chips, which necessitates additional semiconductor chip area. These disadvantages are also not overcome by a method for producing a multichip module which is disclosed in the document US 5,556,812.

It is an object of the invention to provide an electronic device which permits more extensive miniaturization of the active top side of semiconductor chips. This object is achieved by means of the subject matter of the independent claims. Further advantageous embodiments of the invention emerge from the dependent claims.

This object is achieved by means of an electronic device having two or more semiconductor chips with contact areas on their active top sides. These semiconductor chips are integrated into a leadframe in such a way that a placement side of the leadframe and the active top sides of the semiconductor chips are flush and have a common fine wiring plane. This fine wiring plane has interconnects that are so fine that it is possible to reduce the area requirement of the contact areas on the active top side of the semiconductor chip. Furthermore, the common fine wiring plane enables area-intensive passive components

such as coils, capacitors, comb filters and other area-intensive components to be moved from the active top side of the semiconductor chip into the common fine wiring plane.

In the edge region of the leadframe, the fine wiring plane has contact pads which are connected via bonding connections to bonding areas of a rewiring substrate carrying the leadframe. For this purpose, the rewiring substrate has an edge region which is not covered by the leadframe. Bonding areas of the rewiring substrate are arranged on said edge region.

Since the contact areas of the semiconductor chips are connected to interconnects only in the fine wiring plane and have no areas for area-intensive bonding connections, these contact areas may be made significantly smaller than the contact pads on the leadframe and also smaller than the bonding areas on the rewiring substrate. Consequently, not only is it possible to reduce the size of the contact areas of the semiconductor chips, but they also no longer need be limited to the edge region and/or to a central bonding channel on the active top side of a semiconductor chip. Rather, it is now possible to accord the design development greater freedoms for an arrangement of contact

areas. Consequently, the entire surface of the semiconductor chip is available to the circuit design for an arbitrary arrangement of miniaturized contact areas.

Arranged on the rewiring substrate is a housing, into which are packaged the components on the rewiring substrate, such as bonding wires, leadframe with fine wiring plane and embedded semiconductor chips. The underside of the rewiring substrate simultaneously forms an outer side of the electronic device and has external contacts of the electronic device which are distributed on said underside.

The semiconductor chips may have different sizes with regard to their thickness and their active surfaces, and also different integrated circuits. The differences in thickness can be leveled out by the leadframe material, only the active top sides of the semiconductor chips having to be adapted in flush fashion to the top side of the leadframe in order to provide a prerequisite for a common fine wiring plane.

The common fine wiring plane may have electrical interconnects between contact areas of the two or more

semiconductor chips. The semiconductor chips can thus be wired together with one another via the fine wiring plane.

Furthermore, the common fine wiring plane may have electrical interconnects between contact areas of the semiconductor chips and contact pads in the edge region of the leadframe. In this case, it is not important that the contact areas of the semiconductor chips are arranged only in the edge region or in a central bonding region of the semiconductor chips, rather they can be distributed arbitrarily on the surface of the semiconductor chip and are nevertheless connected via the fine wiring plane to area-intensive bonding connections via the contact pads of the leadframe.

The fine wiring plane may have thin-film conductors, which are distinguished by their small thickness of a few hundred nanometers and their small width, which may likewise lie in the submicron range. It is thus possible to provide only contact areas of correspondingly miniaturized external dimensions on the semiconductor chips as well.

Furthermore, the fine wiring plane may be populated with passive discrete electronic components. Discrete

components of this type may have resistors, capacitors or coils, the electrodes of which may be connected via the fine wiring plane to electrodes of the components of the integrated circuit of the semiconductor chips. In particular, it is possible to apply coils to the placement side of the leadframe which not only cover the semiconductor chip but are larger than the active top side of the semiconductor chip. Coils of this type may advantageously be arranged approximately half on the semiconductor chip and approximately half on the leadframe.

Furthermore, the fine wiring plane may have thin-film components, in particular electrical resistors, comb filters, inductive components and/or capacitive components. Components of this type may be realized directly with the fine wiring in the fine wiring plane. For this purpose, electrical resistors have fine wiring interconnects arranged in meandering form, while inductive components have fine wiring interconnects arranged in spiral form or cochleate form. This has the advantage that it is possible to reduce the number of placement devices on the leadframe. Furthermore, it is possible to achieve larger resistances or larger inductances or capacitances

than are possible on the active top sides of the semiconductor chips.

The rewiring substrate not only carries the leadframe on its top side and the external contacts of the electronic device on its underside, but has besides the bonding areas rewiring lines and through contacts which connect bonding areas to external contact areas. External contacts of the electronic device may be arranged on the external contact areas.

Despite the leadframe, provision is made of an additional rewiring substrate for this electronic device in order that coarse wiring planes, that is to say rewiring lines with cross sections which correspond to the cross section of the bonding wires, are made available. The cross section of said lines differs from the fine wiring structure by about one order of magnitude.

The invention furthermore relates to a panel having a plurality of leadframe positions, each leadframe position having a leadframe for the electronic device. The leadframe positions in the panel are arranged in rows and columns, the panel corresponding in form and size to a semiconductor wafer. This has the advantage that fine

wiring structures as are possible in the production of semiconductor chips on semiconductor wafers can also be employed for the common fine wiring plane. In this case, on the panel, not just one leadframe but a plurality of leadframes are simultaneously provided with fine wiring structures. A panel of this type comprising leadframe positions can subsequently advantageously be separated into individual leadframes for electronic devices.

A method for producing an electronic device having a plurality of semiconductor chips which are embedded in a common leadframe works with two different panels. Firstly with a first panel, which has a plurality of leaframe positions, and with a second panel, which has a plurality of device positions and is arranged on a rewiring plate with a plurality of rewiring substrates.

First of all, in the context of the production of an electronic device, a first panel is produced with leadframe positions arranged in rows and columns. In this case, in each leadframe position of the first panel, two or more semiconductor chips are embedded in the material of the leadframe in such a way that the active top sides of the semiconductor chips become flush with one of the two top sides of the first panel. Afterward, on this

panel, a common fine wiring structure is applied to the active top sides of the semiconductor chips and to the top side - flush with said top sides - of the first panel in each leadframe position with corresponding contact pads in the edge regions of each leadframe position. This first panel is then separated into individual leadframes.

Temporally independently of the production of a first panel, a rewiring plate with device positions arranged in rows and columns is produced as baseplate of a second panel. In this case, bonding areas are arranged in edge regions of each device position, which are connected via rewiring lines and through contacts to external contact areas on the rewiring plate in each of the device positions. The leadframes separated from the first panel can then be applied to said rewiring plate in each of the device positions of the rewiring plate whilst leaving free the edge regions with bonding areas. Afterward, bonding connections are carried out between the contact pads of the leadframe and the bonding areas of the rewiring plate in each device position.

Finally, a second panel is produced by covering the device positions with a plastic housing composition. Before the panel is separated into individual electronic devices,

external contacts may be provided on contact areas of the underside of the rewiring plate. However, the application of external contacts may additionally be effected for each device individually after the panel has been separated into individual electronic devices.

This method has the advantage that the individual method steps for producing an electronic device can be effected simultaneously and in parallel for a plurality of devices through the production of a first and a second panel. Furthermore, the first panel may be embodied in wafer form, with the result that it is possible to carry out all the technologies for patterning a fine wiring structure by means of installations, apparatuses and methods which are known from silicon planar technology.

For the application of a common fine wiring structure, it is possible to use a photolithography method for the fine patterning of metal layers applied in closed fashion. Photolithography methods of this type have already been developed to such an extent that submicron structures are possible for the interconnects in the common fine wiring structure.

As an alternative, for the application of a fine wiring structure to the first panel or of a rewiring structure to the rewiring plate, a conductive paste may be printed on and subsequently sintered to form interconnects, contact pads, bonding areas and/or passive components. A method of this type has the advantage that an unpatterned application of closed metal layers is obviated, especially as the conductive paste can be printed on in its end structure onto the leadframe or onto the rewiring plate, respectively. If the material of the contact areas that are printed on or produced by photolithography cannot directly be connected to bonding wires, then the contact areas are coated with a bondable material. On a material of this type, the bonding connections may then be produced by means of thermocompression bonding of bonding wires on the contact pads.

The embedding of the leadframe with the bonding connections on the rewiring plate may also be effected before the division of the rewiring plate into individual electronic devices by means of a transfer molding method, thereby producing a second panel having device positions arranged in rows and columns, which are subsequently separated out from the panel.

To summarize, it should be emphasized that the present invention realizes a leadframe with integrated semiconductor chips which can be processed further by means of thin-film processes or processes comparable with those from wafer production in order to produce a fine wiring. This fine wiring enables very exact and small structures which permit connections between two chips on a confined area. The patterning makes it possible to produce installation locations and placement locations for passive components on the entire leadframe area. The fine wiring on the carrier makes it possible, finally, to route the power supply directly to the semiconductor chip. Furthermore, it is possible to reduce the housing thickness for the later components on the finished patterned and populated leadframe by means of a grinding-back process. Via the fine wiring on the leadframe with integrated semiconductor chips, the signals are passed to the outer edge to contact pads.

After the finished patterned and populated leadframe has been mounted onto a rewiring substrate, the contact connection can be effected by means of wire bonding technology. In this case, all the bonding wires are short and are situated at the edge of the leadframe. This edge position ensures that a housing can also have a high

number of connections. The use of the fine wiring plane ensures that the contact pads of the leadframe are distributed uniformly between four edge side regions. The use of a leadframe with integrated semiconductor chips produces, in principle, a new chip which can be optimized in respect of the requirements of a housing.

The invention will now be explained in more detail with reference to the enclosed figures.

Figure 1 shows a diagrammatic cross section through a leadframe position of a first panel.

Figure 2 shows a diagrammatic cross section as in figure 1 with a fine wiring structure in the leadframe position.

Figure 3 shows a diagrammatic cross section as in figure 2 with a discrete passive component on the fine wiring structure.

Figure 4 shows a plan view of a device position of a second panel prior to packaging in a plastic housing composition.

Figure 5 shows a cross section of an electronic device along the section line A-A of figure 4.

Figure 1 shows a diagrammatic cross section through a leadframe position 23 of a first panel. This first panel essentially has a plurality of leadframe positions arranged in rows and columns. This first panel essentially corresponds in form and size to a semiconductor wafer. However, the material of this wafer is not a semiconductor plate, but rather a plastic plate, in which case, in each of the leadframe positions 23, as shown in figure 1, semiconductor chips 2 are integrated in such a way that the active top sides 5 of the semiconductor chips 2 terminate flush with the placement side 8 of the leadframe 7. The thickness d of the semiconductor chips 2 lies in the range of between 50 µm and 750 µm and may vary from semiconductor chip to semiconductor chip in a respective leadframe position. The thickness D of the plastic material 24 is adapted to the thickness d of the thickest of the semiconductor chips 2 within a leadframe position, so that the passive rear side 31 of the semiconductor chip 2 is covered by plastic material.

In this embodiment of figure 1, after the semiconductor chips 2 had been introduced into the plastic material 24,

the first panel was subjected to a grinding-back process and ground down to the thickness D.

Contact areas 4 are arranged on the active top side 5 of the semiconductor chips 2, the extent of the contact areas 4 in this mode of representation being significantly larger than the true extent of contact areas 4 of this type. It is actually smaller than contact areas on semiconductor chips which have to receive bonding wires. Consequently, the dimensions of these contact areas 4 of the semiconductor chips 2 lie in a range which is smaller than the diameter of bonding wires.

In this embodiment, the contact area 33 is arranged in the edge region of the active top side of the semiconductor chip 2, and the contact area 34 lies at an arbitrary position between the edge region and the central region of the semiconductor chip 2. Such a freely selectable arrangement of the contact area 34, which depends only on the design of the integrated circuit on the active top side 5 of the semiconductor chip 2, can be selected arbitrarily by the layout designer in the case of the electronic device according to the invention.

The surface for realizing passive component structures and large-area contact pads for bonding connections is not limited to the surface region of the semiconductor chip 2 in this leadframe position, so that such area-intensive components of an electronic device are realized on a common fine wiring plane. Components with functions identical to those in figure 1 are identified by the same reference symbols in the following figures 2 to 5 and are not discussed separately.

Figure 2 shows a diagrammatic cross section as in figure 1 with a fine wiring structure 26 in the leadframe position 23. The fine wiring structure 26 is embodied using thin-film technology and therefore has a thickness δ of between 0.5 and 2.5 μm. The width b of the interconnects 20 and 21 is of the same order of magnitude as the thickness of the fine wiring structure 26. Consequently, contact areas 4 of the same minimal order of magnitude down to the submicron range as for the width b of the interconnects 20 and 21 are possible for the semiconductor chip 2.

Contact pads 11 for corresponding bonding connections are arranged on the edge region in each leadframe position 23. These area-intensive contact pads 11 thus only take up

areas which are available on the placement side 8 in each of the leadframe positions 23. While the interconnect 21 connects the contact area 33 of the semiconductor chip 2 to a contact pad 11 in the edge region 10 of the leadframe position, interconnects 20 which directly connect contact areas 4 of the semiconductor chip 2 to contact areas of adjacent semiconductor chips are also provided on the semiconductor chip 2.

Figure 3 shows a diagrammatic cross section as in figure 2 with a discrete passive component 22 on the fine wiring structure 26. In this embodiment, the discrete component 22 is a capacitor, especially as capacitors cannot be directly represented by means of interconnects 20 or 21 as passive components, such as, for example, resistors which are patterned by arrangement of finely patterned interconnects in meandering form or coils which are patterned by arrangement of the interconnects 20 and 21 in spiral form on the fine wiring plane. In order to electrically connect a discrete component 22 in the fine wiring plane 9 within a leadframe position 23, the interconnect 35 leading from the contact area 34 to the contact pad 11 is interrupted and is bridged by the passive component 22 at the interruption location. For this purpose, the electrodes 36 of the passive component

22 are connected to ends of the interconnect 35 at the interruption location.

After the conclusion of the population of the first panel in each of the leadframe positions of the fine wiring plane 9 with passive components 22, the first panel is separated into individual leadframes of each leadframe position 23 and practically represents an enlarged chip which can be applied to a rewiring substrate.

Figure 4 shows a plan view of a device position 30 of a second panel prior to packaging in a plastic housing composition. This device position 30 of the second panel has a rewiring substrate 12, which is part of a contiguous rewiring plate 27 with a plurality of device positions 30. The device positions are arranged in rows and columns in the rewiring plate. Said rewiring substrate 12 carries a leadframe 7 separated from the first panel, the size of the leadframe 7 being smaller than the rewiring substrate 12. Consequently, an edge region 14 having bonding areas 15 remains free on the rewiring substrate. The bonding areas 15 are connected via bonding wires 29 to contact pads 11 on the leadframe 7. Rewiring lines (not shown here) proceed from the bonding areas 7 and lead via

through contacts to the underside 19 of the rewiring substrate 12.

The leadframe 7 shown in figure 4 has two semiconductor chips 2 and 3 of different sizes. The contact areas 4 of these semiconductor chips 2 and 3 are partly arranged in edge regions and partly distributed on the top sides 5 and 6 of the semiconductor chips 2 and 3. The fine wiring structure 26 has interconnects 20 which directly connect contact areas 4 of the semiconductor chip 2 to contact areas 4 of the semiconductor chip 3. Other interconnects 21 of the fine wiring structure 26 connect contact areas 4 to contact pads 11 in the edge region 10 of the leadframe 7. Further interconnects 35 of the fine wiring structure 26 connect contact areas 4 to contact pads 11 via a passive component 22.

This plan view shows that all of the area-intensive components do not take up additional active chip surface, but rather are arranged on the placement side 8 of the leadframe 7. The section line A-A, along which the cross section of an electronic device as shown in figure 5 is taken, runs from left to right in figure 4 firstly through the material in the edge region 14 of the rewiring substrate 12 and in this case cuts through a bonding area

15 and a bonding wire 29 applied on a contact pad 11 of the leadframe 7 by means of a thermocompression pad. From there, the section line A-A continues via the interconnect 35 through the passive component 22 to a contact area 4 which is not arranged at the edge of the semiconductor chip 2.

The section line A-A then cuts through an interconnect 20 which leads from a contact area 4 of the semiconductor chip 2 to a contact area 4 of the semiconductor chip 3. Finally, the section line A-A cuts through a contact area 4 in the edge region of the semiconductor chip 2 of the connected interconnect 21 which leads to a contact pad 11 in the edge region 10 of the leadframe 7. On the right-hand side of the device position 30, the section line A-A again cuts through a bonding wire which leads to the bonding area 15 in the edge region 14 of the rewiring substrate 12.

Figure 5 shows a diagrammatic cross section of an electronic device 1 along the section line A-A of figure 4. Figure 5 shows, compared with figure 4, that the rewiring substrate 12 is covered with a plastic housing composition 28, in which the components carried by the rewiring plate 12 are embedded. Furthermore, figure 5

shows external contacts 18 arranged in a manner distributed uniformly on the underside 19 of the rewiring substrate 12. These external contacts 18 are electrically connected to the bonding areas 15 on the top side 13 of the rewiring substrate 12 via external contact areas, passage contacts and rewiring lines (not shown). Consequently, in this embodiment of the invention, the contact pads 11 in the edge region 10 of the leadframe 7 are electrically connected to the external contacts 18 distributed on the underside 19 and thus on the underside of the electronic device 1.

List of reference symbols

1	Electronic device
2	Semiconductor chip
3	Semiconductor chip
4	Contact areas
5	Active top side
6	Active top side
7	Leadframe
8	Placement side
9	Fine wiring plane
10	Edge region of the leadframe
11	Contact pads
12	Rewiring substrate
13	Top side of the rewiring substrate
14	Edge region of the top side of the rewiring substrate
15	Bonding areas
16	Bonding connections
17	Housing
18	External contacts
19	Underside of the rewiring substrate
20	Interconnect
21	Interconnect

22	Passive electronic component
23	Leadframe position of the first panel
24	Plastic material of the leadframe
25	Top side of the first panel
26	Fine wiring structure
27	Rewiring plate
28	Plastic housing composition
29	Bonding wires
30	Device position of a second panel
31	Passive rear side
32	Underside of the panel
33	Contact area in the edge region
34	Contact area on the active top side
35	Interconnects
36	Electrodes of the passive component
D	Thickness of the leadframe
d	Thickness of the semiconductor chip
δ	Thickness of the fine wiring structure

Patent Claims

1. An electronic device having the following features:

- two or more semiconductor chips (2, 3) with contact areas (4) on their active top sides (5, 6),

- a leadframe (7), the semiconductor chips (2, 3) being integrated into the leadframe (7) in such a way that a placement side (8) of the leadframe (7) and active top sides (5, 6) of the semiconductor chips (2, 3) are flush and have a common fine wiring plane (9), the fine wiring plane (9) having contact pads (11) in the edge region (10) of the leadframe (7),

- a rewiring substrate (12), the rewiring substrate (12) carrying the leadframe (7) on its top side (13), and said top side (13) having an edge region (14) which is not covered by the leadframe (7) and which has bonding areas (15),

- bonding connections (16) arranged between the contact pads (11) of the leadframe (7) and the bonding areas (15) of the rewiring substrate (12),

- a housing (19), into which the components on the rewiring substrate (12) are packaged,

- external contacts (18) of the electronic device (1), which are arranged in a manner distributed on the underside (19) of the rewiring substrate (12).

2. The electronic device as claimed in claim 1, characterized in that the semiconductor chips (2, 3) have different sizes with regard to thickness (d) and active surfaces (5, 6) and different integrated circuits.

3. The electronic device as claimed in claim 1 or claim 2, characterized in that the semiconductor chips (2, 3) have, outside a central bonding channel and outside contact areas on the edge side, additional contact areas (4) distributed arbitrarily on the active top side (5, 6).

4. The electronic device as claimed in one of the preceding claims, characterized in that the fine wiring plane (9) has electrical interconnects (21) between contact areas (4) of the two or more semiconductor chips (2, 3).

5. The electronic device as claimed in one of the preceding claims, characterized in that

the fine wiring plane (9) has electrical interconnects between contact areas (4) and contact pads (11).

6. The electronic device as claimed in one of the preceding claims,
characterized in that
the fine wiring plane (9) has thin-film interconnects.

7. The electronic device as claimed in one of the preceding claims,
characterized in that
the fine wiring plane (9) is populated with passive discrete electronic components (22).

8. The electronic device as claimed in one of the preceding claims,
characterized in that
the fine wiring plane (9) has thin-film components, in particular electrical resistors, comb filters, inductive components and/or capacitive components.

9. The electronic device as claimed in claim 8,
characterized in that
the electrical resistors have a meandering form.

10. The electronic device as claimed in claim 8 or claim 9,
characterized in that
the inductive components have a spiral form.

11. The electronic device as claimed in one of the preceding claims,
characterized in that
the rewiring substrate (12) has rewiring lines and passage contacts to external contact areas with external contacts (18) of the electronic device (1).

12. A leadframe for an electronic device (1) having a plurality of semiconductor chips (2, 3), the semiconductor chips (2, 3) being integrated into the leadframe (7) in such a way that a placement side (8) of the leadframe (7) and active top sides (5, 6) of the semiconductor chips (2, 3) are flush and have a common fine wiring plane (9), which has the features of one of claims 4 to 10.

13. A panel having a plurality of leadframe positions, each leadframe position having a leadframe (7) as claimed in claim 11.

14. The panel as claimed in claim 13,

characterized in that

the leadframe positions are arranged in rows and columns.

15. The panel as claimed in claim 13 or claim 14, characterized in that

the panel corresponds in form and size to a semiconductor wafer or to a printed circuit board.

16. A method for producing an electronic device (1) having a plurality of semiconductor chips (2, 3) which are embedded in a common leadframe (7), the method having the following method steps:

- production of a first panel with leadframe positions arranged in rows and columns, in each leadframe position two or more semiconductor chips (2, 3) being embedded in the material (24) of the leadframe (7), so that the active top sides (5, 6) of the semiconductor chips (2, 3) become flush with a top side of the first panel,
- application of a common fine wiring structure (26) to the active top sides (5, 6) of the semiconductor chips (2, 3) and to the top side (25) - flush with said top sides (5, 6) - of the first panel in each leadframe position with contact pads (11) in the edge regions (10) of each leadframe position,

- separation of the first panel into individual leadframes (7),

- production of a rewiring plate (27) with device positions arranged in rows and columns, with arrangement of bonding areas (15) in edge regions (14) of each device position and application of external contact areas distributed on the underside (19) of the rewiring plate (27) in each device position,

- application of a leadframe (7) separated from the first panel in each of the device positions of the rewiring plate (27) whilst leaving free the edge regions with bonding areas (15),

- production of bonding connections (16) between the contact pads (11) of each leadframe (7) and the bonding areas (15) of the rewiring plate (27) in each device position,

- production of a second panel by covering the device positions with a plastic housing composition,

- application of external contacts (18) on the external contact areas of the rewiring plate,

- separation of the second panel into individual electronic devices (1).

17. The method as claimed in claim 16,

characterized in that

for the application of a common fine wiring structure (9), use is made of a photolithography method for the fine patterning of metal layers applied in closed fashion.

18. The method as claimed in claim 16, characterized in that for the application of a rewiring structure to the rewiring plate (27) or of a fine wiring structure (9) to the first panel, a conductive paste is printed on and subsequently sintered to form interconnects (20, 21), contact pads (11), bonding areas (15) and/or passive components (22).

19. The method as claimed in one of claims 16 to 18, characterized in that the contact pads (11) are coated with a bondable material.

20. The method as claimed in one of claims 16 to 19, characterized in that the bonding connections (16) are bonded by means of thermocompression bonding of bonding wires (29) on the contact pads and on bonding areas (15) assigned thereto.

21. The method as claimed in one of claims 16 to 20, characterized in that

the plastic housing composition (28) is applied by means of a transfer molding method.