STANDARD CELL BACK BIAS ARCHITECTURE

ABSTRACT OF THE DISCLOSURE

An apparatus including, in one embodiment, a CMOS device cell including at least first and second CMOS transistors having first and second CMOS transistor doped regions in first and second doped wells, respectively, wherein each of the first and second CMOS transistor doped regions is configured to be biased with a corresponding one of a power supply potential and a ground potential. Such an embodiment also includes a tap cell having first and second tap cell doped regions in the first and second doped wells, respectively, wherein each of the first and second tap cell doped regions is configured to be biased with a different potential relative to the power supply and ground potential.

(FIG. 1)