

ABSTRACT

An error correction circuit includes an error correction code (ECC) memory and an ECC engine. The ECC memory stores an ECC, which is at least partially represented by a generation matrix. The ECC engine generates parity data based on main data using the ECC, and detects and/or corrects at least one error bit in the main data read from the memory cell array using the parity data. The main data includes a plurality of data bits divided into a plurality of sub data units. The ECC includes a plurality of column vectors divided into a plurality of code groups corresponding to the sub data units. The column vectors have elements configured to gather a mis-corrected bit and multiple error bits in one symbol and the mis-corrected bit is generated due to the multiple error bits in the main data.

FIG. 5