

## ABSTRACT

A semiconductor memory device includes a separation member defining active regions of a substrate. Gate lines intersect the active regions and are each buried in a trench formed in the substrate. Each of the gate lines includes a lower electrode structure and an upper electrode structure on the lower electrode structure. The upper electrode structure includes a source layer substantially covering a sidewall of the trench and including a work-function adjustment element. A conductive layer is on the source layer. A work-function adjustment layer is disposed between the source layer and the conductive layer. The work-function adjustment layer includes a material different from that of the source layer and is doped with the work-function adjustment element.

Fig. 2A