Description

This invention relates to Zener diodes.

Zener diodes having subsurface breakdown regions are known in the art for example from U.S. PATENT 4,136,349 (Tsang), U.S. Patent 4,079,402 (Dunkley et al.), U.S. Patent 4,398,142 (Beasom) and U.S. Patent 4,319,257 (Beasom), each of these patents being incorporated herein by reference. One reason for confining Zener breakdown to a subsurface region is to avoid drift in the Zener breakdown voltage with time. As is known in the art, a Zener diode exhibiting surface breakdown is subject to breakdown voltage drift because of the presence of a passivating or insulating silicon dioxide layer which typically lies adjacent the silicon surface where the breakdown takes place. This effect is discussed in greater detail in the above-mentioned patents. Accordingly, by causing Zener breakdown to occur at a subsurface region, breakdown voltage drift can be avoided.

It is also known in the art that the Zener breakdown voltage varies with temperature. Accordingly, it is known to couple a Zener diode to a temperature compensating device so that the voltage at the diode cathode relative to ground is relatively constant with respect to temperature. U.S. Patent 4,398,142 discusses a circuit including an NPN transistor connected to a Zener diode to maintain a constant voltage at the Zener cathode. U.S. Patent 4,319,257 illustrates another arrangement for coupling a Zener diode to an NPN transistor in order to compensate for Zener breakdown variation in response to temperature changes.

In accordance with the present invention, there is provided a circuit comprising a PNP transistor having a base, an emitter, and a collector, characterized by:

a Zener diode, the cathode of the Zener diode being formed within the emitter and, the emitter forming the anode of the Zener diode.

There is also provided in accordance with the invention a method of forming such a circuit comprising the steps of forming within a substrate of a first conductivity type a first region of a second conductivity type opposite to the first conductivity type, forming within the first region a second region of the first conductivity type, forming within the first region a third region, the third region being of the first conductivity type, said third region laterally surrounding said second region, said third region having a lower dopant concentration than said second region, characterized by the steps of:

forming within the third region a fourth region of the second conductivity type, a subsurface junction being formed between the fourth region and the second region, a junction also being formed between the third and fourth regions, Zener diode breakdown being confined to the junction between the second and fourth regions, and

coupling the substrate and the first region to a first node for receiving a reference voltage.

The invention moreover provides a semiconductor device having a major surface and comprising a first semiconductor region of a first conductivity type, the first semiconductor region serving as the collector of a transistor, a second semiconductor region having a second conductivity type opposite to the first conductivity type, the second semiconductor region serving as the base of the transistor, and a third semiconductor region of the first conductivity type formed within the second semiconductor region, the third semiconductor region serving as at least a portion of the emitter of the transistor, characterized in that the third semiconductor region also serves as the anode of a Zener diode, in that the semiconductor device comprises a fourth semiconductor region of the second conductivity type formed above the third semiconductor region, the fourth semiconductor region serving as the cathode of the Zener diode, and the junction between the third and fourth regions being below the major surface, and in that the semiconductor comprises a fifth semiconductor region of the first conductivity type and having a lower amount of dopant than the third region, the fifth region laterally surrounding the fourth region and serving as part of the emitter of the transistor, the breakdown voltage of the PN junction between the fifth and fourth regions being greater than the breakdown voltage of the PN junction between the third and fourth regions so that the diode exhibits subsurface breakdown. The inventive cathode of a Zener diode exhibiting subsurface breakdown is formed within the emitter of a vertical PNP bipolar transistor. The Zener diode exhibits subsurface breakdown and therefore avoids surface effects which cause Zener breakdown voltage drift over time. The vertical PNP transistor compensates for changes in Zener breakdown voltage caused by changes in temperature. Because the PNP transistor is formed directly underneath the Zener diode, the PNP transistor is at the same temperature as the Zener diode and therefore provides more accurate temperature compensation than if the PNP transistor were positioned further from the Zener diode. In addition, because the Zener cathode is formed directly in the emitter of the PNP transistor, there is no need to provide an emitter contact or an anode contact and therefore the transistor can be constructed with a smaller surface area than would be required if emitter and anode contacts were needed.

Because the cathode is formed directly in the emitter, there is no lateral current flowing through the PNP emitter and therefore no resistive voltage

drop caused by lateral current flow in the emitter of the PNP transistor.

The present invention is further described below, by way of examples with reference to the accompanying drawings, in which;

Figures 1-6 illustrate in cross-section the forming of a Zener diode and temperature compensating transistor in accordance with the present invention; and

Figure 7 is a schematic diagram of the structure of Figure 6.

A process for forming a Zener diode and temperature compensating PNP transistor in accordance with the present invention begins with the step of covering a semiconductor wafer 10 with a photoresist layer 12 (Figure 1). (Hereinafter, reference number 11 refers to the semiconductor substrate while reference number 10 refers to the wafer, i.e. substrate 11 and all layers formed directly or indirectly on the substrate.) In one embodiment, semiconductor wafer 10 is P type silicon having a [100] crystal orientation, and a conductivity of approximately 30 to 50 ohm-centimeters, but other semiconductor materials, crystal orientations, and conductivities can also be used. Referring to Figure 1, a window 14 is formed in photoresist layer 12 via conventional techniques to define the base of a subsequently formed PNP transistor. An N type base 16 is then formed in the area defined by window 14. In one embodiment, this is done by subjecting wafer 10 to an ion implantation process using N type ions such as phosphorus ions.

Referring to Figure 2, photoresist layer 12 is then removed and wafer 10 is covered with a photoresist layer 18. Photoresist layer 18 is then patterened, e.g. by selective exposure to light and removal of the exposed portions, thereby forming windows 20a, 20b and 20c. Windows 20a and 20c coincide with the area where electrical contacts to substrate 11 are to be formed, while window 20b defines a portion of a combination Zener diode anode and PNP transistor emitter. Wafer 10 is then subjected to an ion implantation process using P type ions such as boron ions, thereby forming P+ region 22. As is described below, P+ region 22 forms part of a combination emitter and anode for the subsequently formed PNP transistor and Zener diode respectively. During ion implantation, P+ regions 21a and 21b are also formed. This is done to facilitate the formation of subsequently formed electrical contacts to substrate 11 as described below.

Referring to Figure 3, photoresist layer 18 is removed and wafer 10 is covered with a photoresist layer 24. Photoresist layer 24 is patterned, e.g. by selective exposure to light and removal of the exposed portions, thereby forming window region 26. Window region 26 defines a subsequently formed P region 28 which is used to confine Zener breakdown to a subsurface portion of the Zener diode, as explained in greater detail below. Wafer 10 is then subjected to an ion implantation process during which P type ions, such as boron ions, are implanted into the portion of wafer 10 exposed by window 26, thereby forming P region 28. (Although illustrated as two regions, P region 28 is a single contiguous region laterally surrounding P region 22). Of importance, the concentration of dopants in P region 28 is less than the concentration of dopants in P region 22. As will hereinafter become apparent, this facilitates the confinement of Zener breakdown to a subsurface region in a subsequently formed Zener diode.

At this point in the process, wafer 10 includes P regions 22 and 28 (emitter of the PNP transistor), and N region 16 (the base of the PNP transistor) formed in P substrate 11 (the collector of the PNP transistor).

Referring to Figure 4, photoresist layer 24 is then removed and wafer 10 is covered with a photoresist layer 30. Photoresist layer 30 is then patterned by selective exposure to light and removal of the exposed portions, thereby resulting in the formation of windows 32a, 32b and 32c. Windows 32a and 32c coincide with subsequently formed electrical contacts to base region 16. An N type cathode 36 is formed in the area defined by window 32b. In one embodiment, this is done by subjecting wafer 10 to an N type ion implantation process using, for example, arsenic ions.

Of importance, because P region 22 has a higher dopant concentration than P region 28, the Zener breakdown voltage across PN junction 23 between regions 36 and 22 is lower than the Zener breakdown voltage across PN junction 29 between regions 36 and 28. When breakdown does occur, it occurs across the junction having the lower breakdown voltage, i.e. junction 23, which is formed entirely beneath the surface of wafer 10. In this way, a Zener diode has been formed exhibiting subsurface breakdown.

During formation of cathode 36, N+ regions 37a and 37b (defined by windows 32a and 32c, respectively) are also formed. This facilitates electrical contact to base region 16 of the PNP transistor.

Referring to Figure 5, photoresist layer 30 is then removed, and a layer of silicon dioxide 40 is then formed on wafer 10. In other embodiments, silicon dioxide layer 40 is grown during various drive-in diffusion steps associated with the various regions formed within wafer 10. A photoresist layer 42 is then formed on wafer 10 and patterned in a conventional manner leaving window regions 44a through 44e. As will subsequently become apparent, window regions 44a and 44e define an elec-

trical contact to P type substrate 11 (the collector of the PNP transistor), window regions 44b and 44d define an electrical contact to N type base region 16, and window region 44c defines an electrical contact to cathode 36. The portions of silicon dioxide layer 40 underlying window regions 44a through 44e are then removed using conventional etching techniques, e.g. placing wafer 10 in a buffered HF solution.

Thereafter, photoresist layer 42 is removed and wafer 10 is covered with a layer of conductive material 46 (Figure 6). In one embodiment, conductive material 46 is metal, such as aluminum or an alloy of aluminum, but other conductive materials such as polycrystalline silicon can also be used.

Conductive material 46 is patterned using conventional techniques, e.g. covering wafer 10 with photoresist (not shown), patterning the photoresist thereby exposing portions of the conductive material, removing the exposed portions of conductive material, and removing the remaning photoresist.

A schematic diagram of the resulting structure is provided in Figure 7. As can be seen in Figure 7, the junction between N+ cathode 36 and P+ anode 22 forms the PN junction of a Zener diode D. P+ region 22 and P region 28 form the emitter E of a PNP transistor Q. N region 16 forms the base B of transistor Q and substrate 11 forms the collector C of transistor Q. Base B and collector C are coupled to ground via resistors RB and RC, respectively, which model the lateral resistance of N region 16 and substrate 11, respectively.

Although Figures 1 - 6 illustrate a Zener diode and transistor in which P type substrate 11 serves as the collector, in other embodiments, a P well within an N type substrate or epitaxial layer serves as the PNP collector.

While the invention has been described in detail with respect to specific embodiments, those skilled in the art will recognize that changes can be made in form and detail without departing from the scope of the invention as defined by the following claims.

Claims

1. A circuit comprising a PNP transistor having a base (16), an emitter (22,28), and a collector (11), characterized by:

   a Zener diode, the cathode (36) of the Zener diode being formed within the emitter (22,28) and, the emitter (22) forming the anode of the Zener diode.

2. A circuit according to claim 1 characterized in that the transistor is a vertical transistor.

3. A circuit according to claim 1 or 2 characterized in that the collector (11) and base (16) of the transistor are coupled to ground.

4. A circuit according to claim 3, characterized in that the collector (11) and base (16) are resistively coupled to ground.

5. A circuit according to claim 1, 2, 3 or 4 characterized in that the collector (11) is a semiconductor wafer substrate.

6. A circuit according to any preceding claim characterized in that the Zener diode exhibits subsurface breakdown.

7. A semiconductor device having a major surface and comprising a first semiconductor region (11) of a first conductivity type, the first semiconductor region serving as the collector of a transistor, a second semiconductor region (16) having a second conductivity type opposite to the first conductivity type, the second semiconductor region serving as the base of the transistor, and a third semiconductor region (22) of the first conductivity type formed within the second semiconductor region, the third semiconductor region serving as at least a portion of the emitter (22) of the transistor, characterized in that the third semiconductor region also serves as the anode of a Zener diode, in that the semiconductor device comprises a fourth semiconductor region (36) of the second conductivity type formed above the third semiconductor region, the fourth semiconductor region serving as the cathode of the Zener diode, and the junction (23) between the third and fourth regions (22 & 36) being below the major surface, and in that the semiconductor comprises a fifth semiconductor region (28) of the first conductivity type and having a lower amount of dopant than the third region (22), the fifth region laterally surrounding the fourth region (36) and serving as part of the emitter of the transistor, the breakdown voltage of the PN junction (29) between the fifth and fourth regions (28 & 36) being greater than the breakdown voltage of the PN junction (23) between the third and fourth regions (22 & 36) so that the diode exhibits subsurface breakdown.

8. The device according to claim 7 characterized in that the second semiconductor region (16) is formed within the first semiconductor region (11).

9. A method of forming a circuit as claimed in claim 1 comprising the steps of forming within

trical contact to P type substrate 11 (the collector of the PNP transistor), window regions 44b and 44d define an electrical contact to N type base region 16, and window region 44c defines an electrical contact to cathode 36. The portions of silicon dioxide layer 40 underlying window regions 44a through 44e are then removed using conventional etching techniques, e.g. placing wafer 10 in a buffered HF solution.

Thereafter, photoresist layer 42 is removed and wafer 10 is covered with a layer of conductive material 46 (Figure 6). In one embodiment, conductive material 46 is metal, such as aluminum or an alloy of aluminum, but other conductive materials such as polycrystalline silicon can also be used.

Conductive material 46 is patterned using conventional techniques, e.g. covering wafer 10 with photoresist (not shown), patterning the photoresist thereby exposing portions of the conductive material, removing the exposed portions of conductive material, and removing the remaning photoresist.

A schematic diagram of the resulting structure is provided in Figure 7. As can be seen in Figure 7, the junction between N+ cathode 36 and P+ anode 22 forms the PN junction of a Zener diode D. P+ region 22 and P region 28 form the emitter E of a PNP transistor Q. N region 16 forms the base B of transistor Q and substrate 11 forms the collector C of transistor Q. Base B and collector C are coupled to ground via resistors RB and RC, respectively, which model the lateral resistance of N region 16 and substrate 11, respectively.

Although Figures 1 - 6 illustrate a Zener diode and transistor in which P type substrate 11 serves as the collector, in other embodiments, a P well within an N type substrate or epitaxial layer serves as the PNP collector.

While the invention has been described in detail with respect to specific embodiments, those skilled in the art will recognize that changes can be made in form and detail without departing from the scope of the invention as defined by the following claims.

Claims

1. A circuit comprising a PNP transistor having a base (16), an emitter (22,28), and a collector (11), characterized by:

   a Zener diode, the cathode (36) of the Zener diode being formed within the emitter (22,28) and, the emitter (22) forming the anode of the Zener diode.

2. A circuit according to claim 1 characterized in that the transistor is a vertical transistor.

3. A circuit according to claim 1 or 2 characterized in that the collector (11) and base (16) of the transistor are coupled to ground.

4. A circuit according to claim 3, characterized in that the collector (11) and base (16) are resistively coupled to ground.

5. A circuit according to claim 1, 2, 3 or 4 characterized in that the collector (11) is a semiconductor wafer substrate.

6. A circuit according to any preceding claim characterized in that the Zener diode exhibits subsurface breakdown.

7. A semiconductor device having a major surface and comprising a first semiconductor region (11) of a first conductivity type, the first semiconductor region serving as the collector of a transistor, a second semiconductor region (16) having a second conductivity type opposite to the first conductivity type, the second semiconductor region serving as the base of the transistor, and a third semiconductor region (22) of the first conductivity type formed within the second semiconductor region, the third semiconductor region serving as at least a portion of the emitter (22) of the transistor, characterized in that the third semiconductor region also serves as the anode of a Zener diode, in that the semiconductor device comprises a fourth semiconductor region (36) of the second conductivity type formed above the third semiconductor region, the fourth semiconductor region serving as the cathode of the Zener diode, and the junction (23) between the third and fourth regions (22 & 36) being below the major surface, and in that the semiconductor comprises a fifth semiconductor region (28) of the first conductivity type and having a lower amount of dopant than the third region (22), the fifth region laterally surrounding the fourth region (36) and serving as part of the emitter of the transistor, the breakdown voltage of the PN junction (29) between the fifth and fourth regions (28 & 36) being greater than the breakdown voltage of the PN junction (23) between the third and fourth regions (22 & 36) so that the diode exhibits subsurface breakdown.

8. The device according to claim 7 characterized in that the second semiconductor region (16) is formed within the first semiconductor region (11).

9. A method of forming a circuit as claimed in claim 1 comprising the steps of forming within

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a substrate (11) of a first conductivity type a first region (16)of a second conductivity type opposite to the first conductivity type, forming within the first region a second region (22) of the first conductivity type, forming within the first region a third region (28), the third region being of the first conductivity type, said third region laterally surrounding said second region (22), said third region having a lower dopant concentration than said second region, characterized by the steps of:

forming within the third region a fourth region (36) of the second conductivity type, a subsurface junction (23) being formed between the fourth region (36) and the second region (22), a junction (29) also being formed between the third and fourth regions (28 & 36), Zener diode breakdown being confined to the junction (23) between the second and fourth regions, and

coupling the substrate (11) and the first region (16) to a first node for receiving a reference voltage.

Patentansprüche

1. Schaltungsanordnung mit einem PNP-Transistor, der eine Basis (16), einen Emitter (22, 28) und einen Kollektor (11) aufweist, gekennzeichnet durch eine Z-Diode, wobei die Kathode (36) der Z-Diode im Emitter (22, 28) ausgebildet ist und der Emitter (22) die Anode der Z-Diode bildet.

2. Schaltungsanordnung nach Anspruch 1, dadurch gekennzeichnet, daß der Transistor ein Substrattransistor ist.

3. Schaltungsanordnung nach Anspruch 1 oder 2, dadurch gekennzeichnet, daS der Kollektor (11) und die Basis (16) des Transistors an Masse liegen.

4. Schaltungsanordnung nach Anspruch 3, dadurch gekennzeichnet, daß der Kollektor (11) und die Basis (16) über einen Widerstand an Masse liegen.

5. Schaltungsanordnung nach Anspruch 1, 2, 3 oder 4, dadurch gekennzeichnet, daß der Kollektor (11) ein Halbleitersubstrat ist.

6. Schaltungsanordnung nach einem vorhergehenden Anspruch, dadurch gekennzeichnet, daß die Z-Diode einen Durchbruch unter der Oberfläche zeigt.

7. Halbleiterbauelement mit einer Hauptfläche sowie mit einem ersten Halbleiterbereich (11) eines ersten Leitfähigkeitstyps, wobei der Halbleiterbereich als Kollektor eines Transistors dient, einem zweiten Halbleiterbereich (16) eines zweiten Leitfähigkeitstyps, der dem ersten Leitfähigkeitstyp entgegengesetzt ist, wobei der zweite Halbleiterbereich als Basis des Transistors dient, und einem dritten Halbleiterbereich (22) des ersten Leitfähigkeitstyps, der im zweiten Halbleiterbereich ausgebildet ist, wobei der dritte Halbleiterbereich wenigstens als ein Teil des Emitters (22) des Transistors dient, dadurch gekennzeichnet, daß der dritte Halbleiterbereich auch als Anode einer Z-Diode dient, daß das Halbleiterbauelement einen vierten Halbleiterbereich (36) des zweiten Leitfähigkeitstyps umfaßt, der über dem dritten Halbleiterbereich ausgebildet ist, wobei der vierte Halbleiterbereich als Kathode der Z-Diode dient und der Übergang (23) zwischen dem dritten und dem vierten Bereich (22, 36) unter der Hauptfläche liegt, und der Halbleiter einen fünften Halbleiterbereich (28) des ersten Leitfähigkeitstyps umfaßt, der eine niedrigere Dotierung als der dritte Bereich (22) hat, wobei der fünfte Bereich den vierten Bereich (36) seitlich umgibt und als Teil des Emitters des Transistors dient und die Durchbruchsspannung des PN-Übergangs (29) zwischen dem fünften und dem vierten Bereich (28, 36) größer als die Durchbruchsspannung des PN-Übergangs (23) zwischen dem dritten und dem vierten Bereich (22, 36) ist, so daß die Diode einen Durchbruch unter der Oberfläche zeigt.

8. Bauelement nach Anspruch 7, dadurch gekennzeichnet, daß der zweite Halbleiterbereich (16) im ersten Halbleiterbereich (11) ausgebildet ist.

9. Verfahren zum Herstellen einer Schaltungsanordnung nach Anspruch 1, welches die Schritte der Bildung in einem Substrat (11) eines ersten Leitfähigkeitstyps eines ersten Bereiches (16) eines zweiten Leitfähigkeitstyps, der dem ersten Leitfähigkeitstyp entgegengesetzt ist, der Bildung eines zweiten Bereiches (22) des ersten Leitfähigkeitstyps im ersten Bereich und der Bildung eines dritten Bereiches (28) im ersten Bereich umfaßt, wobei der dritte Bereich vom ersten Leitfähigkeitstyp ist, der dritte Bereich seitlich den zweiten Bereich (22) umgibt und der dritte Bereich eine niedrigere Dotierungskonzentration als der zweite Bereich hat, gekennzeichnet durch die Schritte: Bilden eines vierten Bereiches (36) des zweiten Leitfähigkeitstyps im dritten Bereich, wobei ein

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Übergang (23) unter der Oberfläche zwischen dem vierten Bereich (36) und dem zweiten Bereich (22) gebildet wird, ein Übergang (29) gleichfalls zwischen dem dritten und dem vierten Bereich (28, 36) gebildet wird und der Z-Diodendurchbruch auf den Übergang (23) zwischen dem zweiten und dem vierten Bereich beschränkt ist, und Verbinden des Substrates (11) und des ersten Bereiches (16) mit einem Knotenpunkt zur Aufnahme einer Bezugsspannung.

Revendications

1. Circuit comprenant un transistor PNP ayant une base (16), un émetteur (22,28) et un collecteur (11), caractérisé par :
   une diode Zener,la cathode (36) de la diode Zener étant formée à l'intérieur de l'émetteur (22, 28) et l'émetteur (22) formant l'anode de la diode Zener.

2. Circuit suivant la revendication 1, caractérisé en ce que le transistor est un transistor vertical.

3. Circuit suivant la revendication 1 ou 2, caractérisé en ce que le collecteur (11) et la base (16) du transistor sont reliés à la terre.

4. Circuit suivant la revendication 3, caractérisé en ce que le collecteur (11) et la base (16) sont reliés résistivement à la terre.

5. Circuit suivant la revendication 1,2,3 ou 4, caractérisé en ce que le collecteur (11) est un substrat constitué d'une tranche de semiconducteur.

6. Circuit suivant l'une quelconque des revendications précédentes, caractérisé en ce que la diode Zener présente une rupture au-dessous de la surface.

7. Dispositif semi-conducteur ayant une surface principale et comprenant une première région semi-conductrice (11) d'un premier type de conductivité, la première région semi-conductrice constituant le collecteur d'un transistor, une deuxième région semi-conductrice (16) d'un deuxième type de conductivité opposé au premier type de conductivité, la deuxième région semi-conductrice constituant la base du transistor, et une troisième région semiconductrice (22) du premier type de conductivité formée à l'intérieur de la deuxième région semi-conductrice, la troisième région semiconductrice constituant au moins une partie de l'émetteur (22) du transistor, caractérisé en ce que la troisième région semi-conductrice constitue également l'anode d'une diode Zener, en ce que le dispositif semi-conducteur comprend une quatrième région semi-conductrice (36) du deuxième type de conductivité formée au-dessus de la troisième région semiconductrice, la quatrième région semi-conductrice constituant la cathode de la diode Zener, et la jonction (23) entre les troisième et quatrième régions (22 et 36) étant au-dessous de la surface principale, et en ce que le semiconducteur comprend une cinquième région semi-conductrice (28) du premier type de conductivité et ayant une quantité de dopant plus faible que la troisième région (22), la cinquième région entourant latéralement la quatrième région (36) et constituant une partie de l'émetteur du transistor, la tension de rupture de la jonction PN (29) entre les cinquième et quatrième régions (28 et 36) étant plus élevée que la tension de rupture de la jonction PN (23) entre les troisième et quatrième régions (22 et 36) de sorte que la diode présente une rupture au-dessous de la surface.

8. Dispositif suivant la revendication 7, caractérisé en ce que la deuxième région semi-conductrice (16) est formée à l'intérieur de la première région semi-conductrice (11).

9. Procédé de fabrication d'un circuit suivant la revendication 1, comprenant les étapes de : formation, à l'intérieur d'un substrat (11) d'un premier type de conductivité, d'une première région (16) d'un deuxième type de conductivité opposé au premier type de conductivité ; formation, à l'intérieur de la première région, d'une deuxième région (22) du premier type de conductivité ; et formation, à l'intérieur de la première région, d'une troisième région (28), la troisième région étant du premier type de conductivité, ladite troisième région entourant latéralement ladite deuxième région (22), ladite troisième région ayant une concentration en dopant inférieure à celle de ladite deuxième région,
   caractérisé par les étapes de :
   formation, à l'intérieur de la troisième région, d'une quatrième région (36) du deuxième type de conductivité, une jonction au-dessous de la surface (23) étant formée entre la quatrième région (36) et la deuxième région (22), une jonction (29) étant également formée entre les troisième et quatrième régions (28 et 36), la rupture de la diode Zener étant limitée à la jonction (23) entre les deuxième et quatrième régions, et

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couplage du substrat (11) et de la première région (16) à un premier noeud pour recevoir une tension de référence.

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