SEMICONDUCTOR STORAGE DEVICE AND MANUFACTURING METHOD THEREOF

[Technical Field]

Embodiments of the present invention relate to a semiconductor storage device and a manufacturing method thereof.

[Background Art]

A three-dimensional stacked semiconductor memory, which is an example of a semiconductor storage device, includes a stacked body where a first electrode layer, which functions as a word line, is stacked. A semiconductor film, which functions as a channel, is formed in the stacked body. In addition, a second electrode layer, which functions as a bit line, is located on the stacked body and electrically connected to the semiconductor film.

[Citation List]

[Patent Literature]

[Patent Literature 1]

Japanese Patent publication No. 2019-4146

[Summary of Invention]

[Technical Problem]

In the above-described three-dimensional stacked semiconductor memory, an increase in the number of first electrode layers stacked for an improvement in degree of integration necessitates miniaturization of the second electrode layer. However, the miniaturization of the second electrode layer would lead to incidents such as an increase in electric resistance and a bad connection to the semiconductor film.

Embodiments of the present invention provide a semiconductor storage device and a method of manufacturing the same that are capable of addressing an increase in the number of electrode layers stacked.

[Solution to Problem]

A semiconductor storage device according to an embodiment includes: a first stacked body including a plurality of first electrode layers and a plurality of first insulating layers that are alternately stacked on a substrate in a first direction perpendicular to the substrate; a plurality of semiconductor films penetrating the first stacked body in the first direction; a second stacked body including a plurality of second electrode layers and a plurality of second insulating layers that are alternately stacked on the first stacked body in the first direction; and a plurality of contact plugs penetrating the second stacked body in the first direction and separately connected to the respective plurality of semiconductor films and the respective plurality of second electrode layers.

[Advantageous Effect of Invention]

According to an embodiment, it is possible to address an increase in the stacking number of electrode layers.

[Brief Description of Drawings]

Figure 1 is a perspective view illustrating a structure of a main part of a semiconductor storage device according to a first embodiment.

Figure 2A is a schematic plan view of the semiconductor storage device according to the first embodiment.

Figure 2B is a cross sectional view taken along a section line A1-A1 in Figure 2A.

Figure 3 is an enlarged cross sectional view of a part of a memory film and a semiconductor film.

Figure 4A is a plan view illustrating a formation process of a first stacked body, the memory film, and the semiconductor film.

Figure 4B is a cross sectional view taken along a section line A2-A2 in Figure 4A.

Figure 5A is a plan view illustrating a formation process of a second stacked body.

Figure 5B is a cross sectional view taken along a section line A3-A3 in Figure 5A.

Figure 6A is a plan view of a formation process of a mask.

Figure 6B is a cross sectional view taken along a section line A4-A4 in Figure 6A.

Figure 7A is a plan view illustrating a formation process of a first contact hole.

Figure 7B is a cross sectional view taken along a section line A5-A5 in Figure 7A.

Figure 8A is a plan view illustrating a formation process of a second contact hole.

Figure 8B is a cross sectional view taken along a section line A6-A6 in Figure 8A.

Figure 9A is a plan view illustrating a removal process of a sacrificial layer.

Figure 9B is a cross sectional view taken along a section line A7-A7 in Figure 9A.

Figure 10A is a plan view illustrating a formation process of an insulating film.

Figure 10B is a cross sectional view taken along a section line A8-A8 in Figure 10A.

Figure 11A is a plan view illustrating a formation process of a contact plug.

Figure 11B is a cross sectional view taken along a section line A9-A9 in Figure 11A.

Figure 12 is a perspective view illustrating a structure of a semiconductor storage device according to a comparative example.

Figure 13A is a plan view illustrating a formation process of a second stacked body according to a modification example.

Figure 13B is a cross sectional view taken along a section line B1-B1 in Figure 13A.

Figure 14A is a plan view illustrating a formation process of a mask according to the modification example.

Figure 14B is a cross sectional view taken along a section line B2-B2 in Figure 14A.

Figure 15A is a plan view illustrating a formation process of a first contact hole according to the modification example.

Figure 15B is a cross sectional view taken along a section line B3-B3 in Figure 15A.

Figure 16A is a plan view illustrating a formation process of a second contact hole according to the modification example.

Figure 16B is a cross sectional view taken along a section line B4-B4 in Figure 16A.

Figure 17A is a plan view illustrating a formation process of a metal film according to the modification example.

Figure 17B is a cross sectional view taken along a section line B5-B5 in Figure 17A.

Figure 18A is a plan view illustrating a removal process of the metal film according to the modification example.

Figure 18B is a cross sectional view taken along a section line B6-B6 in Figure 18A.

Figure 19A is a plan view illustrating a removal process of a sacrificial layer according to the modification example.

Figure 19B is a cross sectional view taken along a section line B7-B7 in Figure 19A.

Figure 20A is a plan view illustrating a formation process of an insulating film according to the modification example.

Figure 20B is a cross sectional view taken along a section line B8-B8 in Figure 20A.

Figure 21A is a plan view illustrating a formation process of an insulating film according to the modification example.

Figure 21B is a cross sectional view taken along a section line B9-B9 in Figure 21A.

Figure 22A is a plan view illustrating a formation process of a third hole according to the modification example.

Figure 22B is a cross sectional view taken along a section line B10-B10 in Figure 22A.

Figure 23A is a plan view illustrating a formation process of a metal film according to the modification example.

Figure 23B is a cross sectional view taken along a section line B11-B11 in Figure 23A.

Figure 24A is a plan view illustrating a lining process of a metal film according to the modification example.

Figure 24B is a cross sectional view taken along a section line B12-B12 in Figure 24A.

Figure 25 is a plan view illustrating another lining process of a metal film.

Figure 26 is a perspective view illustrating a structure of a main part of a semiconductor storage device according to a second embodiment.

[Description of Embodiments]

Embodiments of the present invention will be described below with reference to the drawings. The present embodiments by no means limit the present invention.

(First Embodiment)

Figure 1 is a schematic perspective view of a semiconductor storage device according to a first embodiment. Figure 2A is a schematic plan view of the semiconductor storage device according to the first embodiment. Figure 2B is a cross sectional view taken along a section line A1-A1 in Figure 2A. In the figures, a direction perpendicular to a substrate 100 is referred to as a Z-direction (a first direction). Meanwhile, two directions parallel to the substrate 100 and orthogonal to each other are referred to as an X-direction (a third direction) and a Y-direction (a second direction).

A semiconductor storage device 1 according to the present embodiment includes a first stacked body 10, a second stacked body 20, a plurality of memory films 30, a plurality of semiconductor films 40, and a plurality of contact plugs 50.

The first stacked body 10 is provided on the substrate 100. The substrate 100 is, for example, a silicon substrate. The first stacked body 10 includes first electrode layers 11 and first insulating layers 12 alternately stacked in the Z-direction. The first electrode layers 11, which contain, for example, tungsten (W), function as word lines. The first insulating layers 12 contain, for example, silicon oxide (SiO_2). In the present embodiment,

opposite ends of the first stacked body 10 in the Y-direction are provided with respective slit films 101 as illustrated in Figure 1. The slit films 101 cause the first stacked body 10 to be divided.

The second stacked body 20 is provided on the first stacked body 10. The second stacked body 20 includes second electrode layers 21 and second insulating layers 22 alternately stacked in the Z-direction. The second electrode layers 21, which contain, for example, tungsten, function as bit lines. The second insulating layers 22 contain, for example, silicon oxide. An upper surface of each of the second insulating layers 22 is covered with a protecting film 60. The protecting film 60 contains, for example, silicon oxide. It should be noted that illustration of the second insulating layers 22 and the protecting film 60 is omitted in Figure 1.

Figure 3 is an enlarged cross sectional view of a part of the memory films 30 and the semiconductor films 40. The memory films 30 and the semiconductor films 40 penetrate through the first stacked body 10 in the Z-direction. In addition, the memory films 30 each include a block insulating film 31, a charge accumulating film 32, and a tunnel insulating film 33.

The block insulating film 31, which contains, for example, silicon oxide, faces the first electrode layers 11 and the first insulating layers 12. The charge accumulating film 32, which contains, for example, silicon nitride (SiN), faces an inner circumferential surface of the block insulating film 31. The tunnel insulating film 33, which contains, for example, silicon oxynitride (SiON), faces an inner circumferential surface of the charge accumulating film 32.

The semiconductor films 40, which contain, for example, polysilicon, each face an inner circumferential surface of the tunnel insulating film 33. The semiconductor films 40 are each electrically connected to one of the plurality of second electrode layers 21 through the contact plug 50 as illustrated in Figure 2B.

In the present embodiment, the plurality of memory films 30 and the plurality of semiconductor films 40 are arranged along the Y-direction as illustrated in Figure 1. In addition, a plurality

of rows of the memory films 30 and the semiconductor films 40 are arranged in the X-direction.

The contact plugs 50 penetrate through the second stacked body 20 in the Z-direction as illustrated in Figure 2B. In addition, the contact plugs 50 each include a first columnar portion 50a and a second columnar portion 50b. The first columnar portion 50a and the second columnar portion 50b each contain, for example, a metal such as aluminum.

A lower end of the first columnar portion 50a is connected to the semiconductor film 40. An upper end of the first columnar portion 50a is connected to a lower end of the second columnar portion 50b. The second columnar portion 50b has a larger diameter than the first columnar portion 50a. The contact plugs 50 are each connected to one of the plurality of second electrode layers 21 at a boundary portion between the first columnar portion 50a and the second columnar portion 50b.

To separately connect the plurality of contact plugs 50 and the plurality of second electrode layers 21 as described above, side surfaces of the first columnar portions 50a and the second columnar portions 50b are each covered with an insulating film 51. By virtue of the insulating film 51, the contact plugs 50 are each insulated from the second electrode layers 21 except one to be connected.

In addition, in the present embodiment, as for a length in the Z-direction, the first columnar portion 50a of the contact plug 50 connected to lower one of the second electrode layers 21 is shorter than the second columnar portion 50b thereof. In contrast, the first columnar portion 50a of the contact plug 50 connected to upper one of the second electrode layers 21 is longer than the second columnar portion 50b thereof.

A manufacturing method of the above-described semiconductor storage device 1 according to the present embodiment will be described below.

First, the first stacked body 10, the memory films 30, and the semiconductor films 40 are formed on the substrate 100 as illustrated in Figure 4A and Figure 4B. The first stacked body 10

can be formed by, for example, chemical vapor deposition (CVD) or atomic layer deposition (ALD). The memory films 30 and the semiconductor films 40 can be formed in memory holes formed in the first stacked body 10.

Next, the second stacked body 20 is formed on the first stacked body 10 as illustrated in Figure 5A and Figure 5B. The second stacked body 20 can also be formed by CVD or ALD in the same manner as the first stacked body 10.

Next, a mask 70 is formed on the second stacked body 20 as illustrated in Figure 6A and Figure 6B. A plurality of hole portions 71 with respective different depths are formed in the mask 70 in order to form the second columnar portions 50b of the contact plug 50. The mask 70 is, for example, a resist. In addition, a pattern of the hole portions 71 can be formed by, for example, a nanoimplant technique. That is to say, the pattern of the hole portions 71 can be formed by transferring a projection/recess pattern of a template to the mask 70.

Next, etching is applied to the second stacked body 20 through the hole portions 71 by, for example, reactive ion etching (RIE) as illustrated in Figure 7A and Figure 7B. This causes a plurality of first contact holes 80 with respective different depths to be formed. The first contact holes 80 are each terminated at the second electrode layer 21 to be connected in accordance with the depth of corresponding one of the hole portions 71. The mask 70 is then removed.

Next, a sacrificial layer 90 is formed on a side surface of each of the first contact holes 80 and etching is applied to the second stacked body 20 by using the sacrificial layer 90 as a mask as illustrated in Figure 8A and Figure 8B. This causes second contact holes 81 having a smaller diameter than the first contact holes 80 to be formed. The sacrificial layer 90 contains, for example, silicon nitride. In addition, upper ends of the second contact holes 81 are in communication with the first contact holes 80, whereas lower ends thereof reach the semiconductor films 40.

Next, the sacrificial layer 90 is removed by, for example, wet etching as illustrated in Figure 9A and Figure 9B. This causes

the first contact holes 80 and the second contact holes 81 to be exposed.

Next, the insulating film 51 is formed on each of the side surfaces of the first contact holes 80 and side surfaces of the second contact holes 81 as illustrated in Figure 10A and Figure 10B.

Next, the contact plugs 50 are formed and, further, the protecting film 60 is formed on the second stacked body 20 as illustrated in Figure 11A and Figure 11B. The contact plugs 50 can be formed by, for example, embedding a metal material such as tungsten in the first contact holes 80 and the second contact holes 81 and applying chemical machining polishing (CMP) to a surface of a metal film.

At the end, the second stacked body 20 is lined in the X-direction, dividing the second electrode layers 21 as illustrated in Figure 2A and Figure 2B.

A semiconductor storage device according to a comparative example will be described below in comparison with the above-described semiconductor storage device 1 according to the present embodiment.

Figure 12 is a perspective view illustrating a structure of a semiconductor storage device 110 according to the comparative example. Components similar to those of the semiconductor storage device 1 as illustrated in Figure 1 are referred to with the same signs and detailed descriptions thereof will be omitted.

In the semiconductor storage device 110 according to the comparative example, the plurality of semiconductor films 40 belonging to the same rows in the Y-direction are connected to the respective second electrode layers 21 (bit lines) arranged in the X-direction. Accordingly, an increase in the stacking number of the first electrode layers 11 (word lines) necessitates miniaturization of the second electrode layers 21 in order to ensure X-direction intervals between the second electrode layers 21. In this case, a contact area between the second electrode layers 21 and the contact plugs 50 decreases, which increases an electric resistance. In addition, positions of the contact plugs 50

relative to the semiconductor films 40 have a limitation, which would cause an incident of the second electrode layers 21 and the semiconductor films 40 failing to be electrically connected to each other.

However, in the present embodiment, the second electrode layers 21 are stacked in the Z-direction as illustrated in Figure 1. This eliminates the necessity of miniaturization of the second electrode layers 21 even when the stacking number of the first electrode layers 11 is increased, so that contact areas between the second electrode layers 21 and the contact plugs 50 are sufficiently ensured. This makes it possible to reduce an increase in electric resistance. In addition, by virtue of positions of the contact plugs 50 relative to the semiconductor films 40 having no limitation, it is possible to sufficiently ensure an electrical connection between the second electrode layers 21 and the semiconductor films 40.

(Modification Example)

A method of manufacturing a semiconductor storage device according to a modification example will be described below with reference to Figure 13 to Figure 25. It should be noted that components similar to those of the above-described first embodiment are referred to with the same signs and detailed descriptions thereof will be omitted.

First, the first stacked body 10, the memory films 30, and the semiconductor films 40 are formed on the substrate 100 as in the first embodiment.

Next, a second stacked body 20a is formed on the first stacked body 10 as illustrated in Figure 13A and Figure 13B. The second stacked body 20a is different from the second stacked body 20 according to the first embodiment in that no uppermost second electrode layer 21 is formed.

Next, a mask 70a is formed on the second stacked body 20 as illustrated in Figure 14A and Figure 14B. A hole portion 71a and a hole portion 71b are formed in the mask 70a. An opening diameter of the hole portion 71b is larger than an opening diameter of the hole portion 71a. Meanwhile, depths of the hole

portion 71a and the hole portion 71b are equal to each other.

Next, as illustrated in Figure 15A and Figure 15B, etching is applied to the second stacked body 20 through the hole portion 71a and the hole portion 71b by, for example, RIE, thereby forming a plurality of first contact holes 82 with respective different opening diameters. The first contact holes 82 are terminated in the second insulating layer 22 formed on the lowermost second electrode layer 21.

Next, a sacrificial layer 91 is formed on a side surface of each of the first contact holes 82 and etching is applied to the second stacked body 20 by using the sacrificial layer 91 as a mask as illustrated in Figure 16A and Figure 16B. This causes second contact holes 83 having a smaller diameter than the first contact holes 82 to be formed. Upper ends of the second contact holes 83 are in communication with the first contact holes 82, whereas lower ends thereof reach the semiconductor films 40.

Next, a metal film 52 is formed as illustrated in Figure 17A and Figure 17B. At this time, the first contact hole 82 and the second contact hole 83 having small opening diameters are filled with the metal film 52. In contrast, in the first contact hole 82 and the second contact hole 83 having large opening diameters, the metal film 52 is formed on the sacrificial layer 91 or on the side surface of the second contact hole 83 with the inside of the contact holes not being fully filled.

Next, the metal film 52 is removed by, for example, wet etching as illustrated in Figure 18A and Figure 18B. At this time, in the first contact hole 82 and the second contact hole 83 having the small opening diameters, only an upper portion of the metal film 52 is etched. In contrast, in the first contact hole 82 and the second contact hole 83 having the large opening diameters, the metal film 52 is fully removed. Further, an etch-back region EB, in which the lowermost second electrode layer 21 is partially etched, is formed.

Next, the sacrificial layer 91 is removed as illustrated in Figure 19A and Figure 19B.

Next, the insulating film 51 is formed as illustrated in

Figure 20A and Figure 20B. The insulating film 51 is formed at an etching spot of the sacrificial layer 91, the etch-back region EB, etc.

Next, the contact plugs 50 are formed as illustrated in Figure 21A and Figure 21B. Here, the insulating film 51 is first removed by wet etching. However, in the first contact hole 82 and the second contact hole 83 having the small opening diameters, the insulating film 51 provided on the second electrode layer 21 immediately above the lowermost second electrode layer 21 is left. In addition, in the first contact hole 82 and the second contact hole 83 having the large opening diameter, the insulating film 51 formed in the etch-back region EB is also left. Subsequently, the same metal material as that of the metal film 52 is embedded in the first contact hole 82 and the second contact hole 83 and chemical machining polishing is applied to a surface of a metal film. The contact plugs 50 are thus completed.

Next, a third hole 84 is formed as illustrated in Figure 22A and Figure 22B. The third hole 84 is formed on the semiconductor film 40 that is not connected to any of the contact plugs 50. The third hole 84 is formed by etching the second stacked body 20a with a mask 70b having an opening portion 71c. A lower end of the third hole 84 reaches the semiconductor film 40.

Next, a metal film 53 is formed as illustrated in Figure 23A and Figure 23B. Here, an insulating film 54 containing silicon oxide is first formed on an upper surface of the second stacked body 20a and a side surface of the third hole 84. Subsequently, the metal film 53, which contains the same metal material as the second electrode layers 21, is formed on the insulating film 54. The metal film 53 formed on the upper surface of the second stacked body 20a corresponds to the uppermost second electrode layer 21. Meanwhile, the metal film 53 that fills the inside of the third hole 84 corresponds to the contact plug 50 connected to the uppermost second electrode layer 21.

Next, the metal film 53 formed on the upper surface of the second stacked body 20a is lined in the X-direction as illustrated in

Figure 24A and Figure 24B. The uppermost second electrode layer 21 is thus completed.

It should be noted that in the present modification example, the metal film 53 may be machined to cause the second electrode layers 21 to have connection regions 21a as illustrated in Figure 25. In this case, the connection regions 21a, which are to be connected to the contact plugs 50, have wider areas than other regions, which makes it possible to ensure a sufficient connection margin.

Even in the present modification example described above, the second electrode layers 21 can be stacked in the Z-direction. This eliminates the necessity of miniaturization of the second electrode layers 21 even when the stacking number of the first electrode layers 11 is increased as in the first embodiment. Hence, it is possible to reduce an increase in electric resistance and sufficiently ensure an electrical connection between the second electrode layers 21 and the semiconductor films 40.

(Second Embodiment)

Figure 26 is a schematic perspective view of a semiconductor storage device according to a second embodiment. In Figure 26, components similar to those of the semiconductor storage device 1 according to the first embodiment as illustrated in Figure 1 are referred to with the same signs and detailed descriptions thereof will be omitted.

In the above-described first embodiment, the second electrode layers 21 are provided for each row of the semiconductor films 40 arranged in the Y-direction. That is to say, a stacked block of the second electrode layers 21 is provided for each row of the semiconductor films 40.

In contrast, a semiconductor storage device 2 according to the present embodiment, a stacked block of the second electrode layers 21 is provided in common for a plurality of rows of the semiconductor films 40 adjacent in the X-direction as illustrated in Figure 26. At this time, the semiconductor films 40 are each electrically connected to one of the plurality of stacked second

electrode layers 21 as in the first embodiment. It should be noted that the semiconductor storage device 2 according to the present embodiment can be manufactured by a manufacturing method similar to those of the first embodiment and the modification example described above.

According to the above-described present embodiment, the second electrode layers 21 are stacked as in the first embodiment, which eliminates the necessity of miniaturization of the second electrode layers 21 even when the stacking number of the first electrode layers 11 is increased. Therefore, it is possible to reduce an increase in electric resistance and sufficiently ensure an electrical connection between the second electrode layers 21 and the semiconductor films 40.

Further, according to the present embodiment, an area of the second electrode layers 21 is increased as compared with in the first embodiment, which makes it possible to also reduce an electric resistance of the second electrode layers 21.

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel embodiments described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the embodiments described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

Claims

1. A semiconductor storage device comprising:

a first stacked body comprising a plurality of first electrode layers and a plurality of first insulating layers that are alternately stacked on a substrate in a first direction perpendicular to the substrate;

a plurality of semiconductor films penetrating the first stacked body in the first direction;

a second stacked body comprising a plurality of second electrode layers and a plurality of second insulating layers that are alternately stacked on the first stacked body in the first direction; and

a plurality of contact plugs penetrating the second stacked body in the first direction and separately connected to the respective plurality of semiconductor films and the respective plurality of second electrode layers.

2. The semiconductor storage device according to claim 1, wherein the plurality of contact plugs each comprise a first columnar portion and a second columnar portion having a larger diameter than the first columnar portion, the first columnar portion having a lower end connected to the semiconductor film, the first columnar portion having an upper end connected to a lower end of the second columnar portion, the second electrode layers each being connected to the contact plug at a boundary portion between the first columnar portion and the second columnar portion.

3. The semiconductor storage device according to claim 2, wherein a side surface of the first columnar portion and a side surface of the second columnar portion are each covered with an insulating film.

4. The semiconductor storage device according to claim 1, wherein a material of uppermost one of the second electrode

layers and a material of one of the contact plugs connected to the uppermost one of the second electrode layers are same as each other.

5. The semiconductor storage device according to any one of claims 1 to 3, wherein

the plurality of semiconductor films are arranged in a second direction orthogonal to the first direction, and

the plurality of second electrode layers are provided for a row of the semiconductor films.

6. The semiconductor storage device according to any one of claims 1 to 3, wherein

the plurality of semiconductor films are arranged in a second direction orthogonal to the first direction, and

the plurality of second electrode layers are provided in common for a plurality of rows of the semiconductor films adjacent to each other in a third direction orthogonal to the first direction and the second direction.

7. The semiconductor storage device according to any one of claims 1 to 5, further comprising a memory film provided between the plurality of first electrode layers and the plurality of semiconductor films.

8. The semiconductor storage device according to any one of claims 1 to 6, wherein the plurality of first electrode layers are each a word line and the plurality of second electrode layers are each a bit line.

9. A manufacturing method of a semiconductor storage device, the method comprising:

forming a first stacked body and a plurality of semiconductor films on a substrate, the first stacked body comprising a plurality of first electrode layers and a plurality of first insulating layers that are alternately stacked in a first

direction, the plurality of semiconductor films penetrating the first stacked body in the first direction;

forming a second stacked body on the first stacked body, the second stacked body comprising a plurality of second electrode layers and a plurality of second insulating layers that are alternately stacked in the first direction;

forming a plurality of contact holes penetrating the second stacked body in the first direction; and

forming, in the plurality of contact holes, a plurality of contact plugs separately connecting the plurality of semiconductor films and the plurality of second electrode layers.

10. The manufacturing method of a semiconductor storage device according to claim 9, wherein the forming the plurality of contact holes comprises forming a plurality of first contact holes with respective different depths, forming a sacrificial layer on a side surface of each of the first contact holes, and forming second contact holes that are in communication with the respective first contact holes by using the sacrificial layer as a mask.

11. The manufacturing method of a semiconductor storage device according to claim 9, wherein

the forming the plurality of contact holes comprises forming a plurality of first contact holes with respective different opening diameters, forming a sacrificial layer on a side surface of each of the first contact holes, and forming second contact holes that are in communication with the respective first contact holes by using the sacrificial layer as a mask, and

uppermost one of the second electrode layers and one of the contact plugs connected to the uppermost one of the second electrode layers are simultaneously formed.