

SWITCHED COMPARATOR CIRCUITS

The relatively recent development of CMOS switched-capacitor technology provides a way to incorporate on a single integrated circuit a high density of switching, resistive, capacitive and linear amplifier elements having a very low power consumption. Moreover, the development of techniques for fabricating capacitive and resistive elements to precise values (such as, for example, by fabricating precision MOS capacitive elements wherein the ratio of two MOS capacitors defines the value of the element) has permitted the development of circuits comprising components having excellent temperature and voltage stability coefficients as well as component values which may be accurately and precisely specified. Such technology has been particularly applied in monolithic signal filtering applications. See, e.g. Allstot et al, TECHNOLOGICAL DESIGN FOR MONOLITHIC MOS SWITCHED-CAPACITOR FILTERING SYSTEMS (Proceedings of the IEEE, Vol. 71, No. 8, August 1983).

In switching comparator designs, stability against oscillation is needed only when the operational amplifier is operating closed loop. When operating in open loop, the amplifier will not tend to oscillate and therefore its bandwidth need not be restricted. In the present specification there is described a switching comparator circuit with an operational amplifier which is compensated against oscillation only during the time which it is operating in closed loop. During open loop, compensation is switched out of the circuit, thereby permitting the operational amplifier to operate at maximum speed. The result is a highly accurate comparator due to the increased operating speed of the operational amplifier.

There is further described a CMOS limiter using a comparator, the limiter being responsive to an input signal with varying amplitude for producing

an output signal which changes between at least a first and a second level. The transition in the output signal occurs when the absolute value of the amplitude of the input signal exceeds a predetermined reference level.

Because of the advantages provided by switched capacitor CMOS techniques, the fixed reference level may be set very precisely. Only a single linear operational amplification stage (the comparator) is used, so that the limiter has very low power consumption. The input offset voltage of the comparator is nulled out, so that output error is reduced substantially. Finally, the entire limiter circuit may be fabricated on a single CMOS integrated circuit chip.

In the accompanying drawings, by way of example only:-

FIGURE 1 is a schematic diagram of a prior art switching comparator circuit;

FIGURE 2 is a schematic diagram of a switching comparator circuit for use in a limiter embodying the present invention;

FIGURE 3 is a detailed schematic diagram of the prior art operational amplifier shown in FIGURE 1 compensated against oscillation;

FIGURE 4 is a detailed schematic diagram of the operational amplifier shown in FIGURE 2,

FIGURE 5 is a schematic diagram of a comparator circuit using a digital logic array to process the comparator output signal;

FIGURE 6 is a schematic diagram of a limiter embodying the present invention;

FIGURES 7(a)-7(b) are graphical illustrations of the input and the output voltages of the limiter shown in FIGURE 6; and

FIGURE 8 is a timing diagram showing the relationship between various signals produced by the limiter shown in FIGURE 6.

The comparator in the present example of the invention provides high accuracy and fast response time in a CMOS comparator while keeping the number of components to a minimum and not requiring the component structure to be critically well balanced.

Often, the various schemes used to decrease circuit error work against one another. For instance, reduction of error introduced by DC offset voltage typically may only be obtained at the expense of increased response time, and decrease in response time may typically only be obtained at the expense of increased error due to DC offset. For instance, FIGURE 1 is a schematic diagram of a well-known switching comparator design (such as that disclosed by Miyakawa et al, U.S. Patent No. 4,068,138).

Operational amplifier 10 compares the voltage applied to its "-" terminal 12 with ground potential, and produces a positive output voltage V_{out} when the applied voltage is greater than 0. Two voltages to be compared to one another (V_{in} and V_{ref}) are summed together at summing node 20 before being applied to operational amplifier 10. V_{ref} is applied to a capacitor 14 during a time ϕ_2 via a reference switch 16 (which may be a CMOS transmission gate or an NMOS switch). Capacitor 14 stores the value of V_{ref} . During a subsequent interval ϕ_1 , V_{in} is applied to capacitor 14 via an input switch 18. V_{in} is summed with the stored V_{ref} at a summing node 20, the sum being applied to input 12 of operational amplifier 10. ϕ_1 and ϕ_2 are non-overlapping clock signals.

As is well known, a practical operational amplifier will not produce a zero output voltage when its two input terminals have the same voltage applied to them. The input offset voltage (V_{os}) of an operational amplifier is the DC input voltage

required to provide zero voltage at the output of the operational amplifier when the input bias current is also zero. The circuit shown in FIGURE 1 reduces or eliminates the effect of DC offset voltage by sampling the input offset voltage at the same time that V_{ref} is sampled. A third switch 22 is connected between the output and the input terminal 12 of the operational amplifier 10, and is turned on during time period ϕ_2 (i.e. the same time that V_{ref} is connected via switch 16 to capacitor 14). When the output of operational amplifier 10 is connected by switch 22 to its input, the amplifier will assume an equilibrium position (typically with V_{out} assuming the value of the mid-supply point). Input offset voltage is by definition that voltage which causes operational amplifier 10 to assume this equilibrium state. Thus, when switch 22 is closed, the input offset voltage V_{os} of operational amplifier 10 will appear at input terminal 12 of the operational amplifier.

Due to the effect of switches 16 and 22, the voltage V_c appearing across capacitor 14 during time period ϕ_2 is given by

$$V_c(\phi_2) = V_{ref} - V_{os} \quad (1)$$

During ϕ_1 , operational amplifier 10 is operated in an open loop mode and capacitor 14 is connected to V_{in} via switch 18. One may write a voltage equation around the loop during ϕ_1 as

$$-V_{in} + V_{ref} - V_{os} + V_x = 0 \quad (2)$$

(where V_x is the voltage across the input terminals of operational amplifier 10). This implies that

$$V_x = V_{in} - V_{ref} + V_{os} \quad (3)$$

If $V_{in} = V_{ref}$, then $V_x = V_{os}$. This corresponds to the comparison ("trip") point of operational amplifier 10. Since $V_x = V_{os}$, the output of operational amplifier 10 changes

state. Using the circuit shown in FIGURE 1, the effect of the operational amplifier input offset voltage is cancelled out and the comparator is accurate to within millivolts of V_{ref} .

A problem resulting from the use of the scheme shown in FIGURE 1 is that since the operational amplifier is in closed loop during ϕ_2 , it must be internally compensated to stabilize it against oscillation. FIGURE 3 shows a schematic diagram of such an internally compensated operational amplifier 10 suitable for use in the circuit shown in FIGURE 1. A circuit similar to the one shown in FIGURE 3 is disclosed by U.S. Patent No. 4,284,957 to Haque (issued August 18, 1981). One skilled in the art will readily recognize the circuit shown in FIGURE 3 as having a differential amplifier first stage followed by a push-pull output stage.

The gate 12 of FET 24 is the inverting input of operational amplifier 10, while the gate 13 of FET 26 is the non-inverting input of the operational amplifier. FETs 24 and 26 comprise a differential pair and are each provided with an active load (FETs 28 and 30, respectively). A current source (FET 32) supplies a current I_1 to a FET 34. I_1 is mirrored by FET 36 which supplies current to the differential pair (FETs 24 and 26). When the voltage applied to the gate 12 of FET 24 is equal to the voltage applied to gate 13 of FET 26, the current I_a flowing through FET 24 is equal to the current I_b flowing through FET 26. However, if the voltage applied to the gate of FET 24 is different from the voltage applied to the gate of FET 26, I_a will not equal I_b , and the voltage produced at the connection between the drain of active load (FET) 30 and drain of FET 26 will change. This voltage is applied to the gates of FETs 38 and 40, which comprise a push-pull second amplification stage. The output V_{out} of operational amplifier 10 is produced at the connection between the drain of FET 38 and the drain of FET 40.

A common way to stabilize the circuit shown in FIGURE 3 against oscillation is to use a compensation technique called "pole splitting", which creates an approximate single-pole frequency response for operational amplifier 10. One terminal of

a CMOS transmission gate 42 is connected to the junction of the drains of FETs 38 and 40 (i.e. to V_{out}). The other terminal of transmission gate 42 is connected to one terminal of a capacitor 44. The other terminal of capacitor 44 is connected to the tied-together gates of FETs 38 and 40. Capacitor 44 is used as a feedback elements in an inverting gain stage to realize a very large effective capacitance. A dominant low-frequency pole is created by using the "Miller effect".

As is well known, in order for amplifier 10 to exhibit good closed-loop stability, the only dominant pole should appear below the unity-gain frequency ω_u . If any nondominant singularities appear below ω_u , they should exist only as doublets (i.e. one left-half-plane pole and one left-half plane zero existing at very similar frequencies). If compensation capacitor 44 is made sufficiently large with respect to other capacitances existing in the circuit, the second and third poles of the transfer function of operational amplifier 10 are placed well beyond the nominal unity-gain frequency. Assuming that no other nondominant singularities are present, a unity-gain phase margin of at least 45° is obtained, resulting in an approximate single-pole frequency response with a unity-gain bandwidth of

$$\omega_u = G_{m1} / C_f \quad (4)$$

(where C_f is the capacitance of compensation capacitor 44 and G_{m1} is the gain of the differential amplifier stage composed of FETs 24, 26, 28 and 30). See Allstot and Black, Jr.,

"Technological Design Considerations for Monolithic MOS Switched-Capacitor Filtering Systems", Proceedings of the IEEE, Volume 71, No. 8 (August 1983).

Of course, transmission gate 42 is not strictly necessary. However, it is typically provided in conventional circuits in order to reduce the effect of signal feedthrough at high frequencies. When operational amplifier 10 is amplifying high-frequency signals, the signal appearing at the gates of FETs 38 and 40 will feed through capacitor 44 to the output V_{out} .

degrading the phase response of the operational amplifier. The ON resistance of transmission gate 42 need not be zero, however. If transmission gate 42 is made to have a non-zero ON resistance, a voltage which is identical to the feedthrough voltage appearing at V_{out} but opposite in polarity will appear across transmission gate 42. This opposite voltage cancels out the feedthrough voltage developed across compensation capacitor 44, resulting in better operational amplifier phase performance. Thus, in the prior art, transmission gate 42 is tied ON and its ON resistance is adjusted to reduce the effect of signal feedthrough. See, for example, Gray and Meyer, "MOS Operational Amplifier Design - A Tutorial Overview," IEEE Journal of Solid-State Circuits, Volume SC-17, No. 6, page 978 (December 1982); U.S. Patent No. 4,284,957 to Hague.

The Miller multiplication compensation scheme shown in FIGURE 3 is undesirable, however, because the speed of operational amplifier 10 is severely limited by the limited bandwidth necessary for circuit stability. For this reason, those skilled in the art typically resort to far more complex schemes to obtain stability if high speed operation is desired. Such schemes can be very difficult to implement and may involve fabricating individual FETs with close tolerances in order to match the operating parameters of one FET with those of another. Difficulties in fabrication can result in a large number of defective integrated circuits. Such techniques also are costly in power.

FIGURE 2 shows a schematic diagram of a
switching comparator 50.

The functions of switches 16, 18 and 22 and the function of capacitor 14 are the same as described previously in conjunction with FIGURE 1. Operational (differential) amplifier 10

changes bandwidth in response to a control signal ϕ_2 (which also controls whether the operational amplifier is being operated in closed or open loop). When the operational amplifier 52 is operated in closed loop during ϕ_2 (i.e. when closed loop

switch 22 is ON), operational amplifier 10 is internally compensated against oscillation. However, when operational amplifier 52 is operated in open loop (i.e. during ϕ_1), the internal compensation is disconnected to achieve much higher bandwidth and corresponding decreased response time.

FIGURE 4 shows a detailed schematic diagram of operational amplifier 52. The operation of elements of operational amplifier 52 like those shown in FIGURE 3 have similar functions as previously described in conjunction with FIGURE 3 and will not be further described here.

Transmission gate 42 is switched on and off by a control signal rather than being tied ON all the time. Since transmission gate 42 comprises an N switch and a P switch, an inverter 54 is used to invert the control signal so that both the N and the P switch sections of the transmission gate are turned ON simultaneously (of course, a simple N switch could be substituted for transmission gate 42 if desired). When operational amplifier 52 is operated in its closed loop mode (i.e. during ϕ_2), transmission gate 42 is turned ON (and thereby functions as a compensation switch). When operational amplifier 52 is operated in open loop (such as during ϕ_1), transmission gate 42 is turned OFF, thereby disconnecting compensation capacitor 44 from the drains of FETs 38 and 40. As a result, the bandwidth of operational amplifier 52 increases dramatically (since the dominant pole need not lie below the unity-gain frequency), and the speed of the operational amplifier increases correspondingly.

When transmission gate 42 is OFF, the gain-bandwidth product of operational amplifier 52 is increased by 10-50 times or more. The sensitivity of operational amplifier is increased (so that very small differences between signals applied to input terminals 12 and 13 of operational amplifier will produce large differences in the output V_{out} of the operational amplifier within a half clock cycle of the switching phases). The accuracy of the comparator circuit shown in FIGURE 2 is increased by the use of the operational amplifier

in that very small differences between V_{in} and V_{ref} will change the state of the comparator.

A simple dynamic compensation scheme is provided which greatly simplifies comparator design. Standard cells may be used to implement this comparator circuit, thereby reducing the cost and the time necessary for design and manufacturing of comparators. The resulting comparator requires very little supply current and operates at very high speed. The circuitry is compatible with double poly CMOS processes.

As will be recognized, the output of operational amplifier 52 is in an undefined state during ϕ_2 (i.e. when in closed loop). FIGURE 5 shows a presently preferred exemplary embodiment of a digital logic gate array 53 used to process the output of operational amplifier 52 in order to propagate only legitimate changes in state of the operational amplifier caused by the changes in V_{in} (i.e. to block changes in the output of operational amplifier 52 caused by connecting the output of the amplifier back to its input from passing to the output of the comparator). Inverters 54, 55, 64 and 74, NAND gates 56, 58 and 62 and flip-flop 60 serve to propagate the output of operational amplifier 52 through to the output V'_{out} of array 53 only when the output of the operational amplifier assumes a defined level (i.e. when ϕ_2 is low). In particular, these logic elements propagate a change in the output of operational amplifier 52 to V'_{out} as soon as a legitimate state change occurs (rather than one or more clock pulses later). In other words, changes in the output of operational amplifier 52 are asynchronously propagated to the output V'_{out} and simultaneously determine the state of flip-flop 60 so that during the next time that ϕ_1 goes low, V'_{out} will maintain its present output.

As mentioned previously, ϕ_1 and ϕ_2 must be non-overlapping clock signals. Inverters 66 and 68, flip-flop 70 and sampling controller 72 produce such non-overlapping clock signals. A system clock signal CLK is applied to the input of inverter 66. The output of inverter 66 is applied to the input of an inverter 68 and to the T input of a falling-edge sensitive T-type flip-flop 70. The output of inverter 68 is used to clock flip-flop 60, while the output of inverter 66 is used to control

the state transitions of flip-flop 70. As is well known, every time the signal applied to the T input of flip-flop 70 changes from a logic 1 to a logic 0, the Q output of the flip-flop is complemented. Flip-flop 60 thus divides the frequency of the system clock by 2. Sampling controller block 72 produces two non-overlapping clock signals ϕ_1 and ϕ_2 . ϕ_1 and ϕ_2 are non-overlapping clock signals in that they never assume logic level 1 simultaneously. In the preferred embodiment, ϕ_1 and ϕ_2 are the complements of one another. Sampling controller block 72 is of conventional design, and, in the preferred embodiment, comprises a combinational logic array which produces non-overlapping ϕ_1 and ϕ_2 each of which are at the same frequency as the signal produced at the Q output of flip-flop 70.

The CMOS limiter of Figure 6 provides voltage limiting, within a predetermined "window", of a varying input signal. FIGURES 7(a)-7(b) show the relationship between the input and output signals of such a limiter.

The output of the limiter changes state only when the input V_{in} satisfies the following:

$$|V_{in}| > V_{lim} \quad (5)$$

(where V_{lim} is a reference voltage of a predetermined level). In other words, the output signal V_{out} changes state whenever either $V_{in} > V_{lim}$ or $V_{in} < -V_{lim}$ (the present limiter may hence be described as an infinite gain limiter).

The output V_{out} of the limiter should not change state for $|V_{in}| \leq V_{lim}$, but rather should retain its latest value. Once V_{out} changes state for $V_{in} > V_{lim}$, V_{out} will not again change state until $V_{in} < -V_{lim}$. Likewise, once V_{out} changes state for $V_{in} < -V_{lim}$, V_{out} will not again change state until $V_{in} > V_{lim}$. V_{out} is graphically illustrated in FIGURE 7(b) for an arbitrary input signal V_{in} shown in FIGURE 7(a).

A schematic diagram of
a limiter 110

is shown in FIGURE 6. One preferred embodiment of limiter 110 is fabricated on a single integrated circuit chip using any conventional double poly CMOS technology. A reference source 112 and a clock generator 154 may be external to the monolithic limiter 110 for added flexibility in controlling the operating parameters of the limiter.

A reference source 112 (typically a variable, highly-stable reference voltage source) produces a predetermined reference signal V_{lim} , which determines the input voltage level at which transitions of the output voltage of the limiter occur. V_{lim} is selectively applied to a summing node A by a MOSFET switching element 114 when a signal ϕ_2 is high (i.e. logic level 1).

V_{in} (the input signal to be limited) is sampled by a MOSFET switching element 116 and a capacitor 118. Switching element 116 applies V_{in} to capacitor 118 when signal ϕ_2 is high. V_{in} is also sampled and inverted by MOSFET switching elements 120, 122 and 124 and a capacitor 126. When the signal ϕ_2 is high, V_{in} is applied to a first connection 128 of capacitor 126 through MOSFET switching element 120, while a second connection 130 of the capacitor is connected to ground potential through MOSFET switching element 122. When a signal ϕ_1 is high, first connection 128 of capacitor 126 is grounded to ground potential, and the inverted sampled V_{in} may be obtained from second connection 130 of the capacitor. ϕ_1 and ϕ_2 are non-overlapping (i.e. they are never high simultaneously).

The values of capacitors 118 and 126 should be chosen to be small enough to permit charging during the interval when the control signals are high, yet large enough to minimize the effect of clock feedthrough offsets (i.e. voltage offsets produced by storage of clock signals in the capacitance between capacitor 118 and switching elements 116 and 132 and between capacitor 126 and its associated switching elements) and charge injection due to the MOSFET transmission gates. Capacitors 118 and 126 have equal capacitance in the preferred embodiment to balance the effect of errors which may be introduced.

A first switching network comprising MOSFET switching element 132 and a MOSFET switching element 134 selectively apply one of the sampled signal level of V_{in} (stored on capacitor 118) and the sampled inverted signal level of V_{in} (stored on capacitor 126) to summing node A. Switching element 132 applies sampled V_{in} to summing node A when a signal ϕ_3 is high, while switching element 134 applies inverted sampled V_{in} to summing node A when a signal ϕ_4 is high. Summing node A comprises a simple hard-wired connection of switching elements 114, 132 and 134 and a capacitor 138. The relationship between ϕ_1 , ϕ_2 , ϕ_3 and ϕ_4 will be explained in greater detail shortly.

A comparator network including an active CMOS comparator 136 and capacitor 138 are connected to summing node A. The "-" input 140 of comparator 136 is connected to summing node A via capacitor 138, while the "+" input of the comparator is connected to ground potential. Comparator 136 is a conventional CMOS comparator which produces an output signal V_{comp} which is low (i.e. assumes logic level "0") when the signal applied to input 140 is greater than the signal applied to input 142, and is high (i.e. assumes logic level "1") when the signal applied to input 140 is less than the signal applied to input 142. Thus, V_{comp} will be low if V_a (the voltage level at node A) exceeds V_c (the voltage across capacitor 138). V_{comp} will be high when $V_c > V_a$.

V_{comp} is applied to the input of a conventional digital logic inverter 144. The output of inverter 144 is applied to one of the two inputs of a NAND gate 146. The output of NAND gate 146 is applied to one of the inputs of a two-input NAND gate 148. The output of NAND gate 148 is applied to the D input of a D-type conventional flip-flop 150, the Q output of which is applied to an input of a two-input NAND gate 152. The output of NAND gate 152 is applied to the other input of NAND gate 148.

A clock generator 154 produces a periodic clock signal ϕ_0 . In the preferred embodiment, clock generator 154 is a conventional free-running square wave oscillator operating at a fixed frequency. The frequency of clock generator 154 is chosen

to be high enough to minimize the effect of leakage of capacitors 118, 126 and 138 on circuit performance as well as to handle the input frequency range of V_{in} . The output of clock generator 154 is applied to the input of an inverter 156. The output of inverter 156 is applied to the input of an inverter 158 and to the T input of a falling-edge sensitive T-type flip-flop 160. The output of inverter 158 is used to clock flip-flop 150, while the output of inverter 156 is used to control the state transitions of flip-flop 160. As is well known, every time the signal applied to the T input of flip-flop 160 changes from a logic 1 to a logic 0, the Q output of the flip-flop is complemented. Flip-flop 160 thus functions to divide the frequency of ϕ_0 by two. As will be explained, flip-flop 150 maintains the present output of NAND gate 148 during periods in which the output of comparator 136 (V_{comp}) is undefined whenever ϕ_2 is high.

The Q output of flip-flop 160 is applied to a sampling controller block 162 which produces two non-overlapping clock signals ϕ_1 and ϕ_2 (discussed earlier). ϕ_1 and ϕ_2 are non-overlapping clock signals in that they never assume logic level 1 simultaneously. In the preferred embodiment, ϕ_1 and ϕ_2 are the complements of one another. Sampling controller block 162 is of conventional design, and, in the preferred embodiment, comprises a combinational logic array which produces non-overlapping ϕ_1 and ϕ_2 each of which are at the same frequency as the signal produced at the Q output of flip-flop 160. ϕ_1 is applied to the other input of NAND gate 146 directly and through the other input of NAND gate 152 through an inverter 163.

The output of NAND gate 148, in addition to being applied to the D input of flip-flop 150, is also applied to an input of a two-input AND gate 164. The other input of AND gate 164 is connected to ϕ_2 , while the output of the AND gate is connected to the T input of a positive edge triggered T flip-flop 166. AND gate 164 gates the output of NAND gate 148 with ϕ_2 to reduce the possibility of "glitches" or other transients causing

flip-flop 166 to change state. The Q output of flip-flop 166 is connected to an input of a two-input NOR gate 168, while the $\bar{Q}$ output of the flip-flop is connected to an input of a two-input NOR gate 170. The other input of each of NOR gates 168 and 170 are connected in common and to the input of an inverter 172. The input of inverter 172 is connected to ϕ_1 .

The Q output of flip-flop 166 is also connected to the input of an inverter 174, the output of which is the output signal of limiter circuit 110 (V_{out}).

The operation of the presently preferred exemplary embodiment shown in FIGURE 6 may be better understood by observing the timing diagram shown in FIGURE 8. V_{in} is sampled during the interval when ϕ_2 is high, and is stored on capacitors 118 and 126. Depending upon the level of output of T-flip-flop 166, either the (non-inverted) signal stored on capacitor 118 or the (inverted) signal stored on capacitor 126 is selected and connected to summing node A. Hysteresis is provided by controlling when the various MOSFET switching elements are switched in relation to one another.

V_{lim} is summed with the signal selected by one of the MOSFET switching elements 132 and 134 at summing node A. When ϕ_2 is high (and thus, ϕ_1 is low), V_{lim} is applied to and stored by capacitor 138. Simultaneously, V_{in} is applied to capacitors 118 and 126 when ϕ_2 is high. As is shown in FIGURE 8, ϕ_3 and ϕ_4 may be high only when ϕ_2 is low, so that V_{in} is never applied directly to summing node A, nor is V_{lim} ever directly applied to capacitors 118 and 126.

It will be understood that when ϕ_2 is high, the output V_{comp} of comparator 136 goes to an unknown (undefined) level. NAND gates 146, 152 and 148, inverters 144 and 163 and flip-flop 150 serve to propagate V_{comp} through to the input of NAND gate 164 only when V_{comp} assumes a defined level (i.e. when ϕ_2 is low).

When ϕ_1 is high, switching elements 114, 116, 120 and 122, act as open circuits, and switching element 124 acts as a closed circuit. Thus, one of the signal levels stored on capacitor 118

and capacitor 126 (the latter available from connection 130 of capacitor 126) is applied to summing node A when one of ϕ_3 or ϕ_4 is high. During this time, connection 128 of capacitor 126 is connected to ground by switching element 124. Also during this time, V_{lim} (stored on capacitor 138) is subtracted from the selected one of the voltages stored on capacitors 118 and 126.

ϕ_3 is high only when ϕ_1 is high and V_{out} is low. When ϕ_3 is high, $V_{in} - V_{lim}$ is applied to input 140 of comparator 136, causing V_{comp} to be low only when $V_{in} < V_{lim}$. Likewise, ϕ_4 is high only when V_{out} is high and ϕ_1 is high. When ϕ_4 is high, $-V_{in} - V_{lim}$ is applied to input 140 of comparator 136, so that V_{comp} will be low only if $V_{in} < -V_{lim}$ (i.e. V_{in} is inverted and compared with positive V_{lim}). V_{out} changes state only when V_{comp} is low and a leading edge of ϕ_2 occurs.

Because flip-flop 166 is triggered by the positive edge of the output NAND gate 164, flip-flop 166 will change state the next time ϕ_2 is high and the output of NAND gate 148 is high. When flip-flop 166 changes state, the opposite one of ϕ_3 and ϕ_4 than the one high in the previous state is made high (as gated by ϕ_1). In this way, the signal level stored on a different one of capacitors 118 and 126 is applied to summing node A. A search for the next "window excursion" is thus carried out.

As is well known, mismatches in the input circuit of comparator 136 may result in a non-zero input offset voltage. Input offset voltage (V_{off}) is the voltage which must be applied to lead 140 of comparator 136 to cause the comparator to sense that equal signal levels applied to leads 140 and 142 are exactly equal. As is well known, V_{off} has, in general, an unknown value which fluctuates with several factors (such as temperature, power supply voltage, etc.). To compensate for this non-zero input offset voltage, a MOSFET switching element 172 is connected between the output of comparator 136 and the input 140 of the comparator. Switching element 172 is triggered by ϕ_2 . Thus, V_c (the voltage across capacitor 138) is in fact $V_{lim} -$

V_{off} (where V_{off} is the non-zero input offset voltage of comparator 136). Comparator 136 is compensated for a non-zero V_{off} , resulting in more accurate operation.

The limiter circuit 110 shown in FIGURE 6 may be fabricated on a single integrated circuit chip. In the preferred embodiment, switched capacitor techniques are used to implement the switching elements (114, 116, 120, 122, 124, 132, 134 and 172) and capacitors (118, 126 and 138).

Although only one exemplary embodiment has been described in detail above, those skilled in the art will appreciate that many variations and modifications may be made in this exemplary embodiment without departing from the novel and advantage features of this invention. For instance, although switching elements 114, 116, 120, 122, 124, 132, 134 and 172 are shown as simple N-MOSFETs, they can each comprise a transmission gate having both an n-channel and a p-channel switch in order to increase the dynamic range (signal handling capability) of limiter 110 (of course, the p-channel switches would be controlled by the inverse of the corresponding n-channel switch control signals). Likewise, while the circuitry used in the preferred embodiment for producing ϕ_1 , ϕ_2 , ϕ_3 and ϕ_4 is implemented by CMOS digital logic elements, it would be understood that many other implementations (such as a transmission gate and capacitor or a microprocessor implementation) are possible. Moreover, capacitor 138 could be used to store the level of $V_{in} - V_{off}$ (or $-V_{in} - V_{off}$) rather than V_{lim} (provided that the arrangement of the various switching elements was changed to accommodate such a configuration). Also, V_{lim} could be made variable and applied at different levels depending upon the current limiter output, thus increasing the amount of hysteresis control. In addition to double poly, poly-to-diffusion or metal-to-diffusion capacitors could be used with care taken as to the extra stray capacitance associated with such structures. Accordingly, these and other modifications are intended to be within the scope of the following claims.



CLAIMS

1. An electrical signal limiter with hysteresis, said limiter comprising:

a voltage comparator having first and second inputs and an output, said comparator having two different output states depending upon which of its inputs is at the higher relative voltage and having said first input connected to a reference voltage point;

a first switched capacitor means for storing a sample of a limiting voltage V_{lim} ;

a second switched capacitor means for storing a sample of an input voltage V_{in} ;

a third switched capacitor means for storing an inverted sample of the input voltage, that is $-V_{in}$ and

sampling control means connected to said output of the voltage comparator and to said first, second and third switched capacitor means for alternatively connecting either said first and second or said first and third switched capacitor means in circuit with the second input of the voltage comparator as required to cause a change of state in the comparator output when $|V_{in}| > V_{lim}$.

2. An electrical signal limiter with hysteresis as in claim 1 wherein said first switched capacitor means includes offset switch means connected between the comparator output and its second input for sensing and also simultaneously storing any offset voltage V_{off} associated with the comparator's operation in the first switched capacitor means.



3. A limiter as in claim 2 wherein:

said second switched capacitor means includes first input signal level storing means for storing the level of said sampled input voltage V_{in} ; and

said third switched capacitor means includes second input signal level storing means for storing the negative of the level of said sampled input voltage $-V_{in}$.

4. A CMOS limiter as in claim 3 wherein:

said second switched capacitor means further includes first input switching means for periodically applying said input voltage to said first input signal level storing means; and

said third switched capacitor means further includes second input switching means for periodically applying said input signal to said second input signal level storing means.

5. A CMOS limiter as in claim 4 wherein:

said second input signal level storing means comprises a MOS precision capacitive element having first and second plates; and

said third switched capacitor means further comprises:

first inverter switching means for periodically connecting the first plate of said capacitive element to ground potential, said first plate also coupled to said second input switching means, said first input switching means connecting said first plate to said input voltage and said first inverter switching means connecting said first plate to ground potential in alternating sequence in response to signals produced by said sampling control means; and

second inverter switching means for periodically connecting the second plate of said capacitive element to ground potential, said second plate also connected to said first switching means, said first switching means connecting said second plate to said first input of said comparator and said second inverter switching means connecting said second plate to ground potential in alternating sequence in response to said signal produced by said sampling control means.



6. A limiter as in claim 5 wherein said first and second input switching means apply said input signal to said first and second input signal level storing means, respectively, during the same periodic time interval.

7. A limiter as in claim 4 wherein said first and second input switching means apply said input signal to said first and second input signal level storing means, respectively, during the same periodic time interval.

8. A limiter as in claim 4 wherein said sampling control means includes:

selection control means, responsive to said output of said voltage comparator, for producing first and second control signals, the production of said first control signal and the production of said second control signal being mutually exclusive;

first selection switching means, responsive to said first control signal, for applying the signal stored by said first input signal level storing means in circuit with the second input of the voltage comparator; and

second selection switching means, responsive to said second control signal, for applying the signal stored by said second input signal level storing means in circuit with the second input of the voltage comparator.



9. A limiter as in claim 8 wherein;

said sampling control means further includes means for producing a sampling control signal, said sampling control signal specifying the periodic time intervals during which said first and second input switching means apply said input signal to said first and second input signal level storing means, respectively; and

said selection control means includes means responsive to said sampling control signal for gating said first and said second control signals with the inverse of said sampling control signal to prevent said sampling control signal and one of said first and second control signals from being produced simultaneously.

10. A limiter as in claim 9 wherein said sampling control means further comprises:

clock generator means for producing a periodic clock signal; and

sequential logic means, responsive to said clock signal and to the signal produced by said comparator, for producing said output signal and said first and second control signals.

11. A limiter as in claim 1 further including summing means, connecting said first, second and third switched capacitor means together, for summing one of said stored voltages V_{in} and $-V_{in}$ with said stored limiting voltage V_{lim} .

12. A limiter as in claim 1 wherein said offset switch means connects the output and the second input of said voltage comparator together during an interval when said limiting voltage is sampled by said first switched capacitor means.

13. A limiter as in claim 1 wherein said first input of the voltage comparator is connected to ground potential.



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14. A CMOS limiter, responsive to an input signal of varying amplitude, for producing an output signal which changes between at least first and second levels when the absolute value of the amplitude of said
5 input signal exceeds a predetermined reference level, said limiter comprising: sampling means for sampling said input signal; sampling and inverting means for sampling and inverting said input signal; first switching means, responsive to said output signal,
10 for selecting said sampled input signal when said output signal is produced at said first level and for selecting said inverted sampled input signal when said output signal is produced at said second level; summing means for summing said selected signal
15 and said predetermined reference level together to produce a summed signal having a polarity; and comparing means, connected to receive said summed signal, for changing the level of said output signal in response to said polarity of said summed signal.

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15. A CMOS limiter as in claim 14 wherein said limiter further comprises:

reference signal level storing means for storing the level of said predetermined reference
25 level;

second switching means for periodically applying said predetermined reference level to said reference signal level storing means; and

summing node means, connecting said first
30 switching means and said second switching means to said reference signal level storing means, for producing a signal level proportional to the difference between said selected signal and said stored predetermined reference level.



16. A CMOS limiter as in claim 15 wherein said first and said second switching means alternately apply said selected signal and said predetermined reference level, respectively, to said summing node means.

17. A CMOS limiter as in claim 16 wherein:

said first switching means includes means for producing a sampling control signal, said sampling control signal specifying the periodic time intervals during which said first and second input switching means apply said input signal to said first and second input signal level storing means, respectively.

18. A CMOS limiter as in claim 17 wherein said comparing means further includes an operational amplifier, responsive to said difference signal, for producing a signal when said difference signal exceeds a second predetermined reference level.

19. A CMOS limiter as in claim 18 wherein said summing node means includes means for subtracting a signal proportional to the input offset voltage of said operational amplifier from said selected signal.

20. A CMOS limiter as in claim 18 wherein said second predetermined reference level is ground potential.

21. A CMOS limiter as in claim 18 wherein said comparing means further comprises:

a clock generator means for producing a periodic clock signal; and

sequential logic means, responsive to said clock signal and to the signal produced by said operational amplifier, for producing said output signal and for controlling said first switching means to select one of said sampled input signal and said inverted sampled input signal.



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22 . A CMOS signal limiter with hysteresis comprising:

an operational amplifier (136) having one grounded input, one signal input and one output;

a first capacitor (138) connected at one end to said one signal input, a first controllable switch (172) connected across said output and signal input of the operational amplifier having an offset voltage V_{off} and a second controllable switch (114) connected between the other end of said first capacitor at a summing node and a limiting reference voltage V_{lim} , said first and second controllable switches (172, 114) being simultaneously operable to store a reference voltage $V_{lim} - V_{off}$ across said first capacitor;

a second capacitor (118) having one end grounded, and its other end controllably connected to said summing node through a third controllable switch (132) operable to temporarily connect said first and second capacitors in series with the signal input of said operational amplifier;

a third capacitor (126) having one end controllably grounded through a fourth controllable switch (122) and its other end controllably grounded through a fifth controllable switch (124), its said one end also being controllably connected to said summing node through a sixth controllable switch (134);

said other end of the second capacitor and said one end of the third capacitor being controllably connected to an input signal voltage through a seventh controllable switch (116, 120); and

control means connected to the output of said operational amplifier and to each of said controllable switches for causing said first, second, fourth and seventh controllable switches to operate simultaneously and in synchronous non-overlapping timed relationship with the alternate operations of either the third or the fifth and sixth controllable switches.



23. A CMOS limiter as in claim 22 wherein said seventh controllable switch comprises a first input controllable switch (116) and a second input controllable switch (120), a first end of said first and second input controllable switches commonly connected to said input signal voltage, the other end of said first input controllable switch connected to said other end of said second capacitor, the other end of said second input controllable switch connected to said other end of said third capacitor, said first and second input controllable switches operating simultaneously with said first, second and fourth controllable switches.

24. A CMOS limiter as in claim 22 wherein said control means comprises:

- clock generator means for producing a periodic clock signal;
- sampling controller means, responsive to said clock signal, for producing a first and a second non-overlapping control signal, said first control signal operating said first, second, fourth and seventh controllable switches and said second control signal operating said fifth controllable switch;

- first gating means, responsive to said output of said operational amplifier and to said first control signal, for producing a signal which changes with a change in said output of said operational amplifier only when said second control signal is not present and otherwise corresponds to the output of said operational amplifier during the last interval when said first control signal was present;

- a flip-flop (166) the input of which is connected to said signal produced by said first gating means, the flip-flop changing state when the signal produced by said first gating means changes, said flip-flop having first and second complementary outputs; and

- second gating means for gating each of said first and second outputs of said flip-flop with said first control signal, said gated first output operating said third controllable switch, said gated second output operating said sixth controllable switch.



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25. A signal processor comprising:

a signal comparator having first and second inputs and an output, said comparator having two different output states depending upon which of its inputs is at the higher relative voltage, said first input adapted to be connected to a reference signal point;

a first storing means for storing a sample of a limiting signal V_{lim} ;

a second storage means for storing a sample of input signal V_{in} ;

a third storage means for storing an inverted sample of the input signal, that is $-V_{in}$; and

sampling control means coupled to said output of the signal comparator and to said first, second and third storage means for alternately connecting either said first and second or said first and third storage means in circuit with the second input of the signal comparator as required to cause the signal comparator output to assume a first output state when V_{in} and V_{lim} are of a first combination of polarities and to assume a second state when V_{in} and V_{lim} are of a second combination of polarities.

26. A signal processor programmed to respond to an input signal of varying amplitude, for producing an output signal which changes between at least first and second levels when the absolute value of an amplitude of said input signal exceeds a predetermined reference level, said processor comprising;

sampling means for sampling said input signal;

sampling and inverting means for sampling and inverting said input signal;

first switching means, responsive to said output signal, for selecting said sampled input signal when



said output signal is produced at said first level and for selecting said inverted sampled input signal when said output signal is produced at said second level;

5 summing means for summing said selected signal and said predetermined reference level to produce a summed signal having a polarity, and

 comparing means, connected to receive said summed signal, for changing the level of said output
10 signal in response to said polarity of said summed signal.

27. A method for producing an output signal, in response to an input signal of varying amplitude,
15 which output signal changes between at least first and second levels when the absolute value of the amplitude of said input signal exceeds a predetermined reference level, comprising the steps of: producing an output signal at one of said first and second levels;
20 sampling said input signal; sampling and inverting said input signal; selecting said sampled input signal when said output signal is produced at said first level; selecting said inverted sampled input signal when said output signal is produced at said
25 second level; summing said selected signal and said predetermined reference level together to produce a summed signal having a polarity; and changing the level of said output signal in response to said polarity of said summed signal.

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28. A method of processing signals comprising the steps of: applying a reference signal to a first input of a signal comparator having first and second inputs and an output, said comparator having two differ-
35 ent output states depending upon which of its inputs



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is at the higher relative voltage; storing a sample of a limiting signal V_{lim} ; storing a sample of an input signal V_{in} ; storing an inverted sample of the input signal, that is $-V_{in}$; and alternating

5 connecting either (a) said stored sample of said limiting signal V_{lim} and said stored sample of said input signal V_{in} or (b) said stored sample of said limiting signal V_{lim} and said stored inverted sample of said input signal $-V_{in}$ in circuit with said second

10 input of said signal comparator as required to cause the signal comparator output to assume a first output state when V_{in} and V_{lim} are of a first combination of polarities and to assume a second output state when V_{in} and V_{lim} are of a second combination of

15 polarities.
