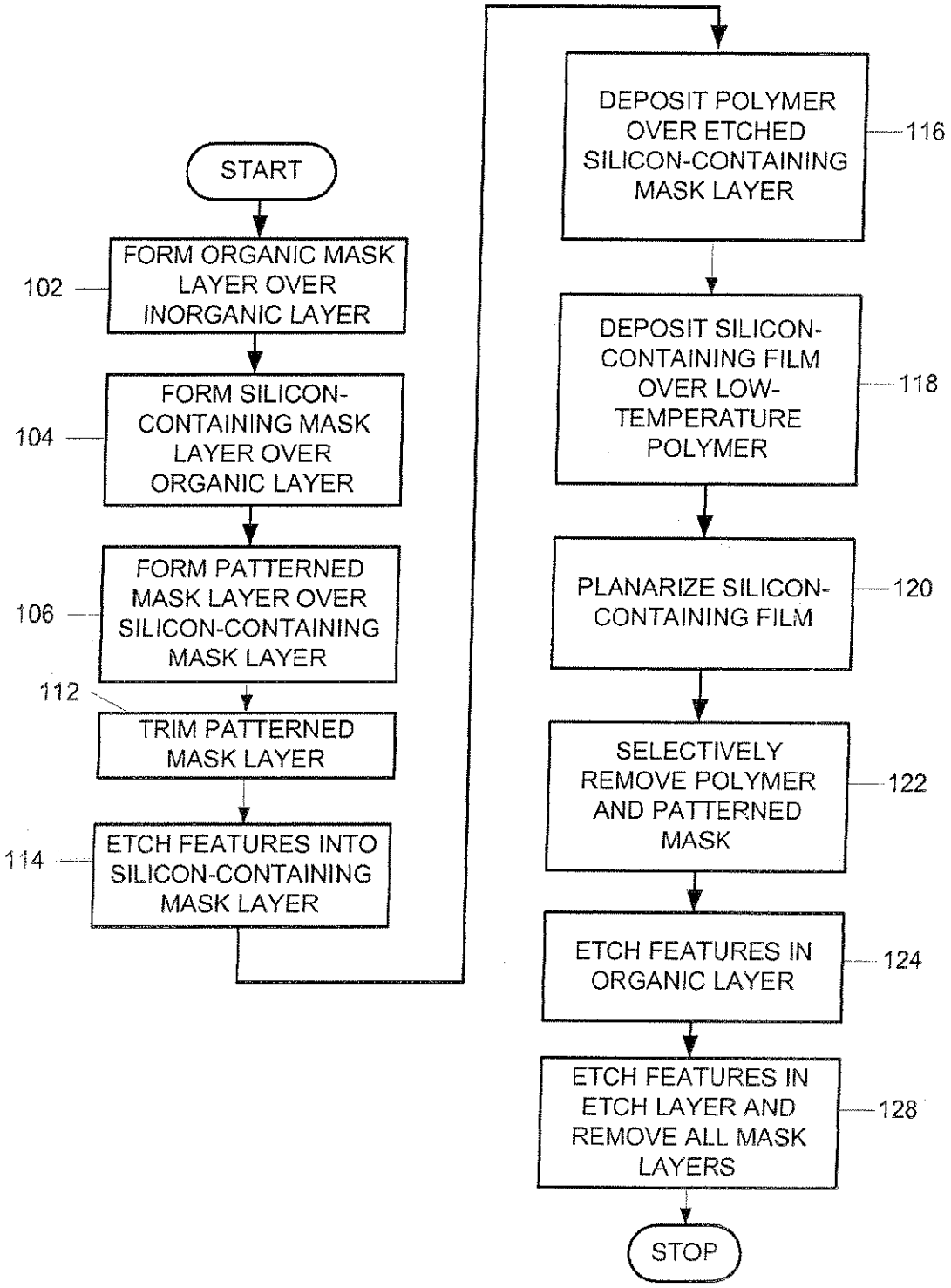

START
FORM ORGANIC MASK LAYER OVER INORGANIC LAYER
102
FORM SILICON-CONTAINING MASK LAYER OVER ORGANIC LAYER
104
FORM PATTERNED MASK LAYER OVER SILICON-CONTAINING MASK LAYER
106
112
TRIM PATTERNED MASK LAYER
ETCH FEATURES INTO SILICON-CONTAINING MASK LAYER
114
DEPOSIT POLYMER OVER ETCHED SILICON-CONTAINING MASK LAYER
116
DEPOSIT SILICON-CONTAINING FILM OVER LOW-TEMPERATURE POLYMER
118
PLANARIZE SILICON-CONTAINING FILM
120
SELECTIVELY REMOVE POLYMER AND PATTERNED MASK
122
ETCH FEATURES IN ORGANIC LAYER
124
ETCH FEATURES IN ETCH LAYER AND REMOVE ALL MASK LAYERS
128
STOP

FIG. 1

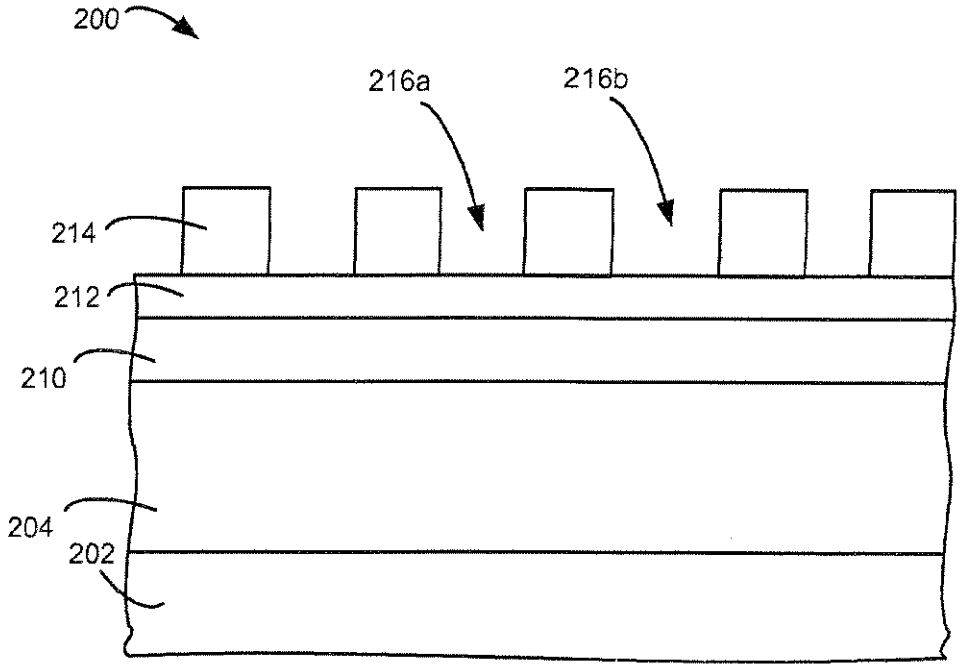

200
216a
216b
214
212
210
204
202

FIG. 2A

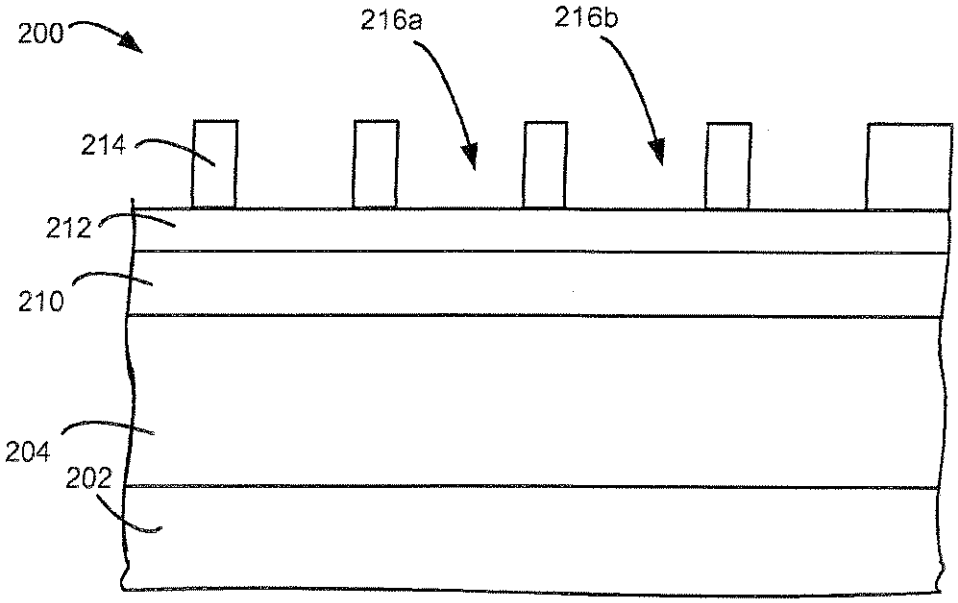

200
216a
216b
214
212
210
204
202

FIG. 2B

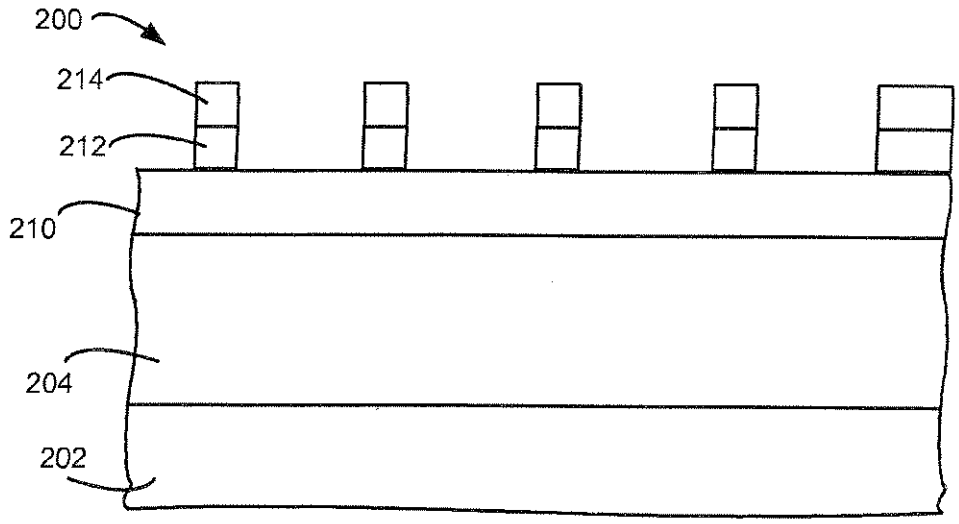

200
214
212
210
204
202

FIG. 2C

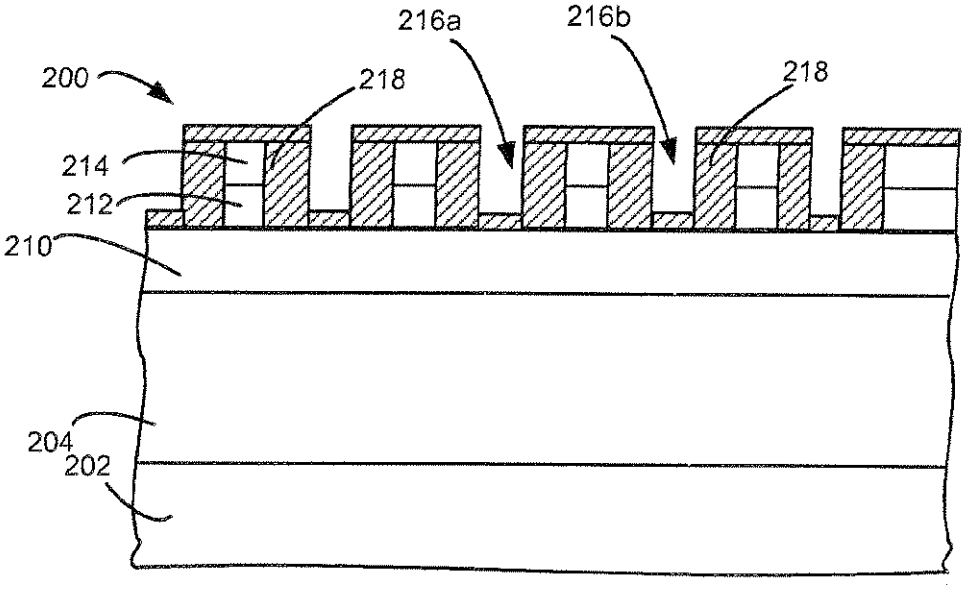

216a
216b
200
218
218
214
212
210
204
202

FIG. 2D

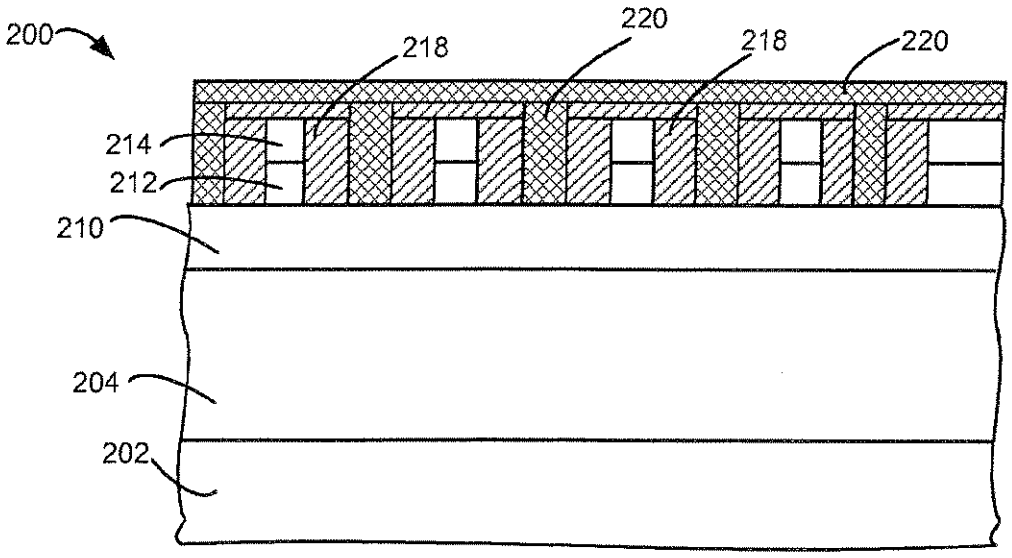

200
218
220
218
220
214
212
210
204
202

FIG. 2E

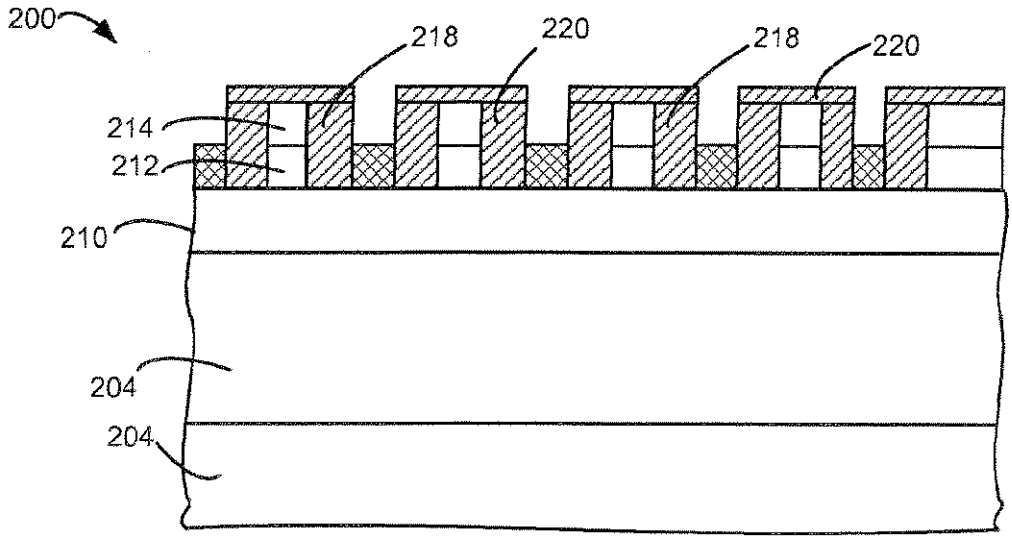

200
218
220
218
220
214
212
210
204
204

FIG. 2F

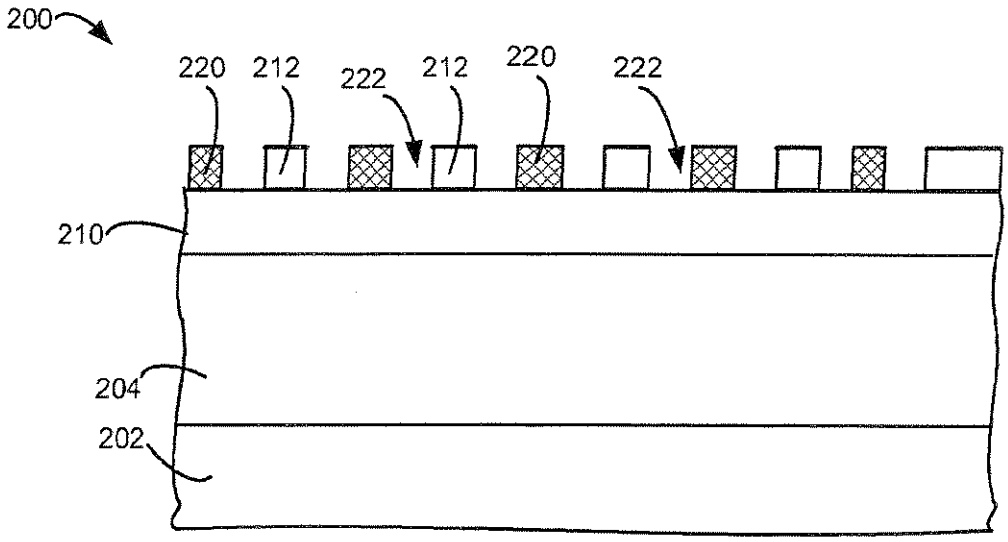

200
220
212
222
212
220
222
210
204
202

FIG. 2G

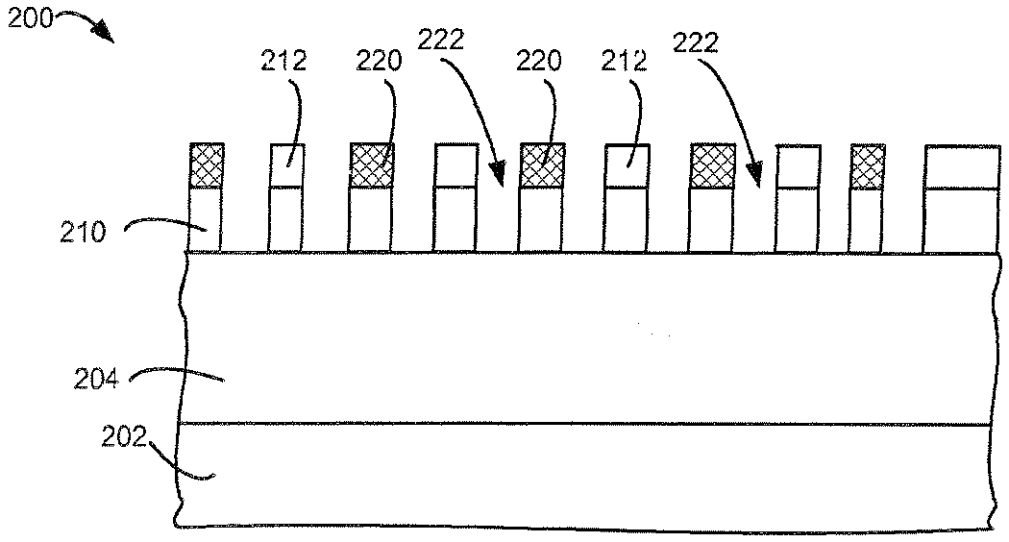

200
212
220
222
220
212
222
210
204
202

FIG. 2H

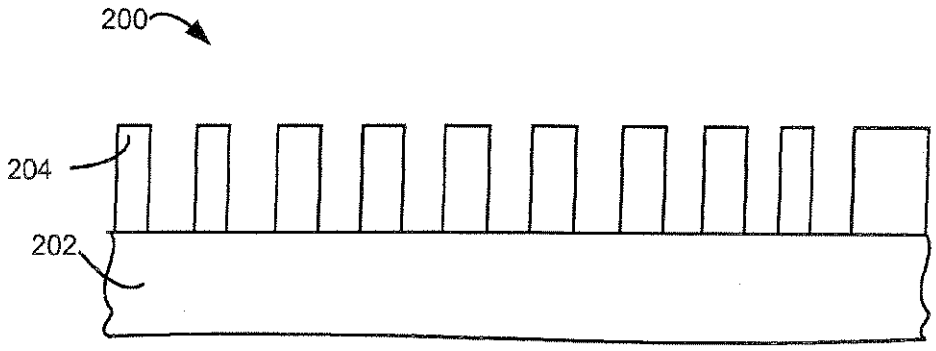


FIG. 2I

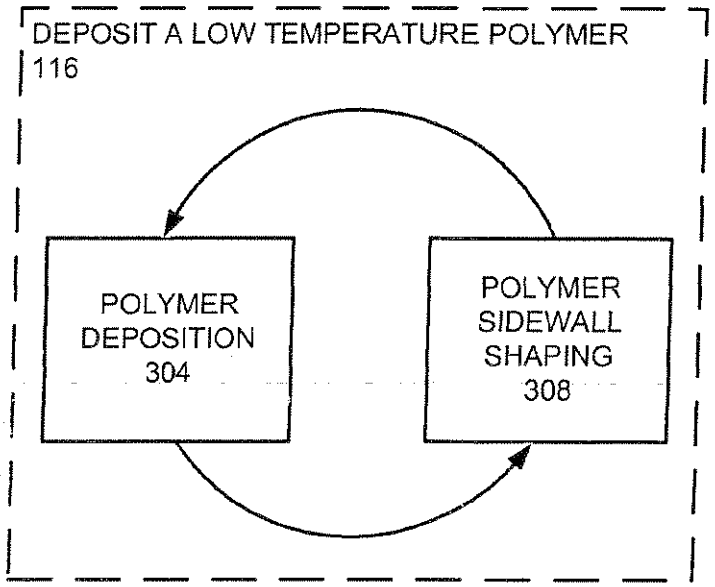

DEPOSIT A LOW TEMPERATURE POLYMER
116
POLYMER
DEPOSITION
304
POLYMER
SIDEWALL
SHAPING
308

FIG. 3

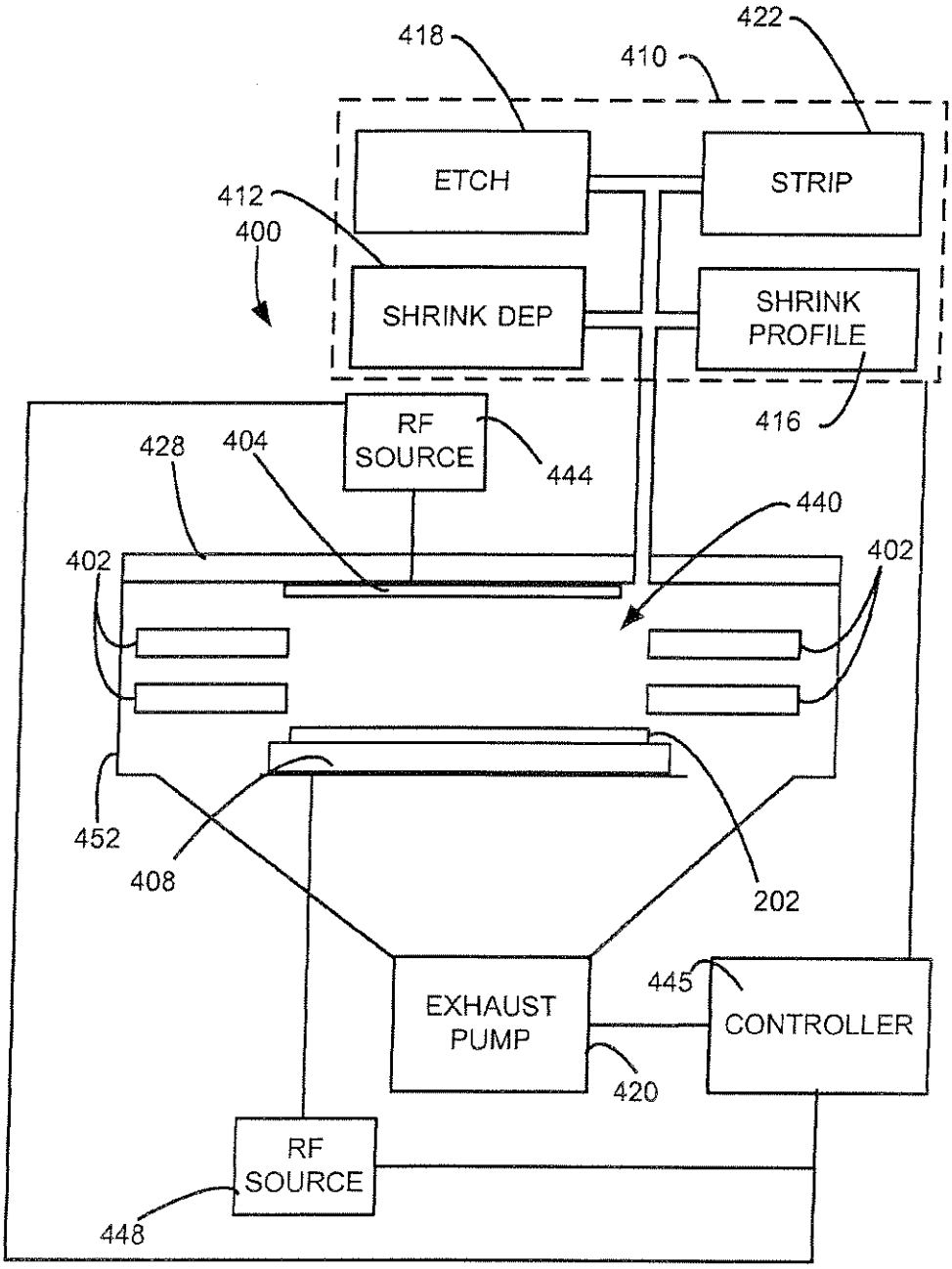

418
422
410
ETCH
STRIP
412
400
SHRINK DEP
SHRINK PROFILE
416
RF SOURCE
444
428
404
440
402
402
452
408
202
EXHAUST PUMP
445
CONTROLLER
420
RF SOURCE
448

FIG. 4

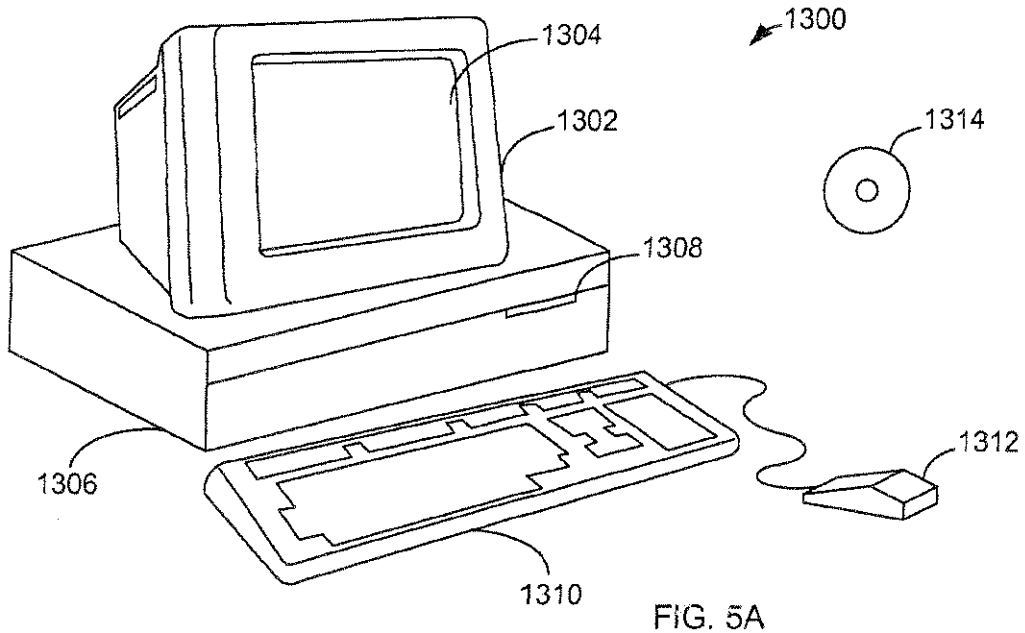

1300
1304
1302
1314
1308
1312
1306
1310

FIG. 5A

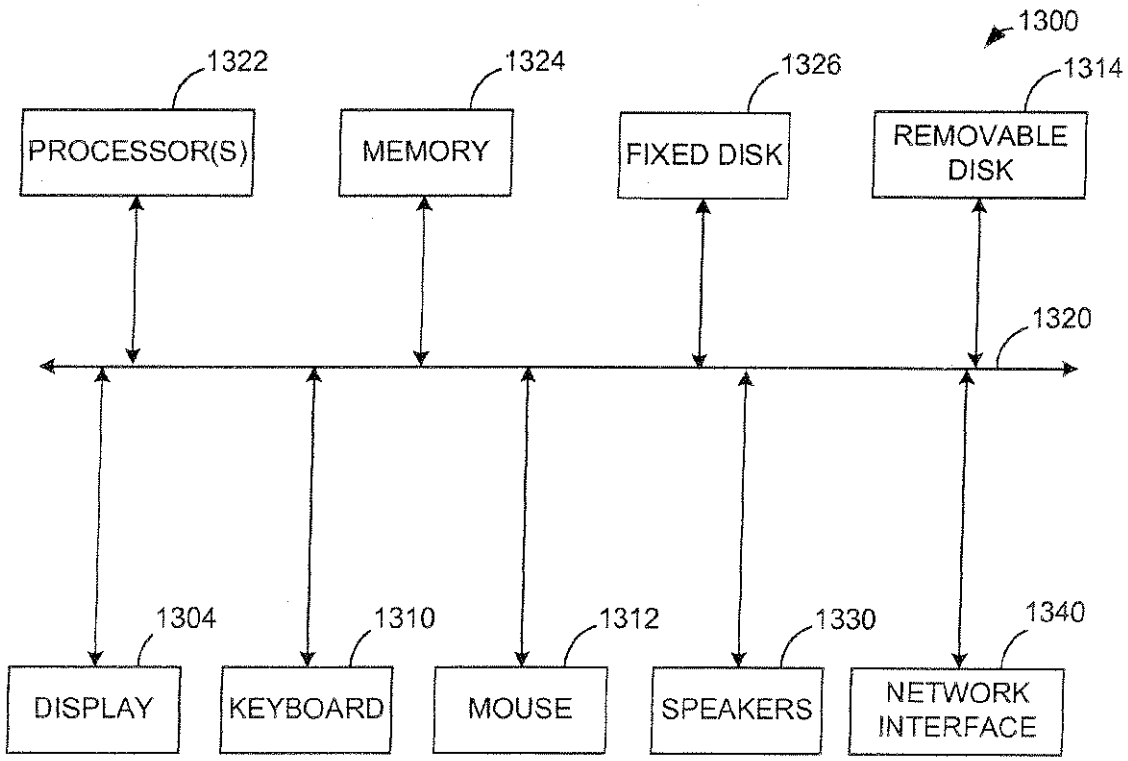

1300
1322
1324
1326
1314
PROCESSOR(S)
MEMORY
FIXED DISK
REMOVABLE DISK
1320
1304
1310
1312
1330
1340
DISPLAY
KEYBOARD
MOUSE
SPEAKERS
NETWORK INTERFACE

FIG. 5B

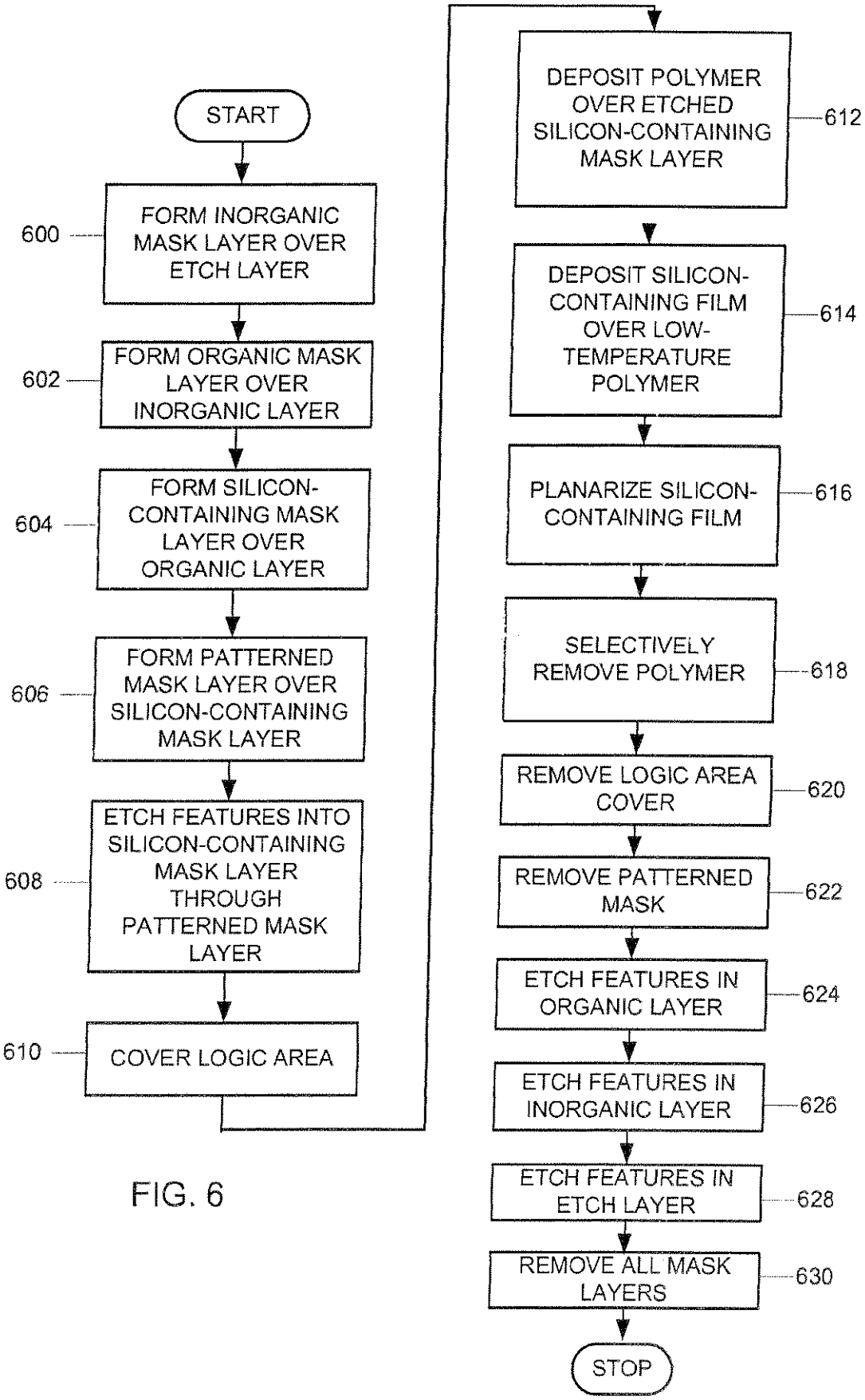

START
600
FORM INORGANIC MASK LAYER OVER ETCH LAYER
602
FORM ORGANIC MASK LAYER OVER INORGANIC LAYER
604
FORM SILICON-CONTAINING MASK LAYER OVER ORGANIC LAYER
606
FORM PATTERNED MASK LAYER OVER SILICON-CONTAINING MASK LAYER
608
ETCH FEATURES INTO SILICON-CONTAINING MASK LAYER THROUGH PATTERNED MASK LAYER
610
COVER LOGIC AREA
DEPOSIT POLYMER OVER ETCHED SILICON-CONTAINING MASK LAYER
612
DEPOSIT SILICON-CONTAINING FILM OVER LOW-TEMPERATURE POLYMER
614
PLANARIZE SILICON-CONTAINING FILM
616
SELECTIVELY REMOVE POLYMER
618
REMOVE LOGIC AREA COVER
620
REMOVE PATTERNED MASK
622
ETCH FEATURES IN ORGANIC LAYER
624
ETCH FEATURES IN INORGANIC LAYER
626
ETCH FEATURES IN ETCH LAYER
628
REMOVE ALL MASK LAYERS
630
STOP

FIG. 6

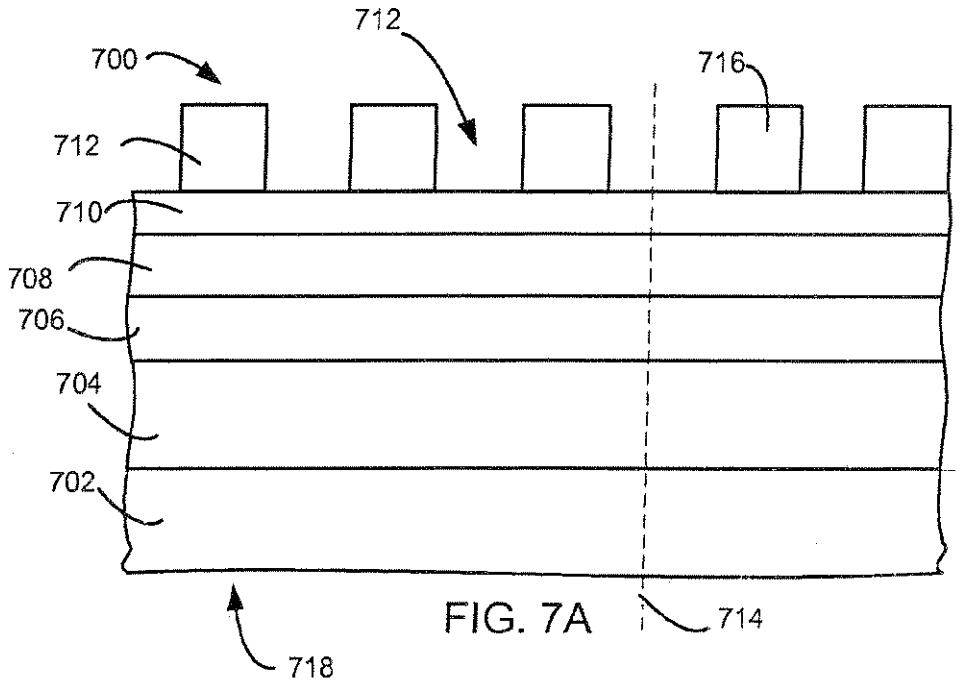

712
700
716
712
710
708
706
704
702
718
714

FIG. 7A

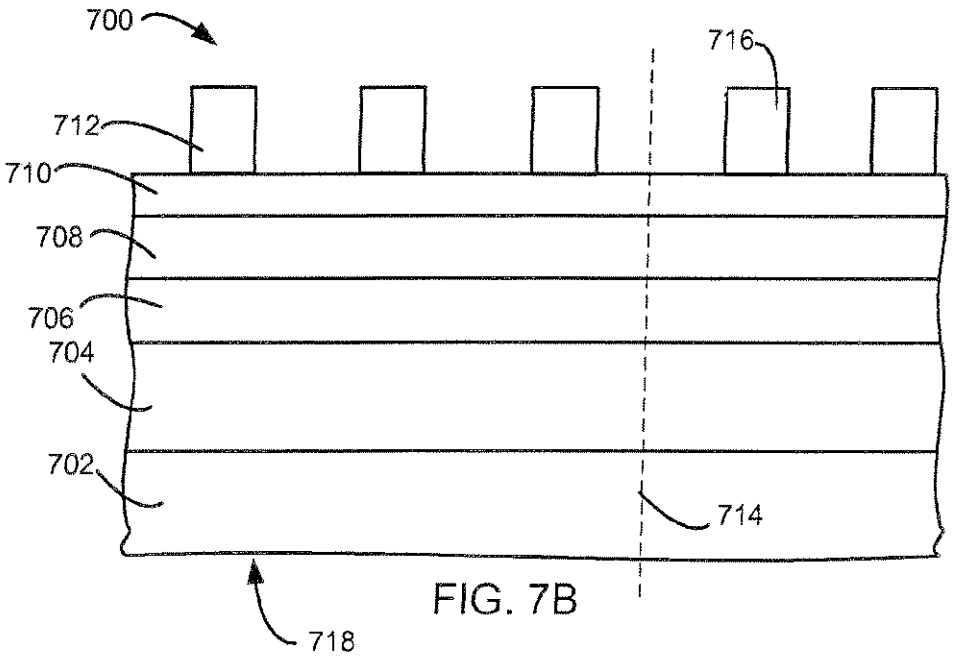

700
716
712
710
708
706
704
702
714
718

FIG. 7B

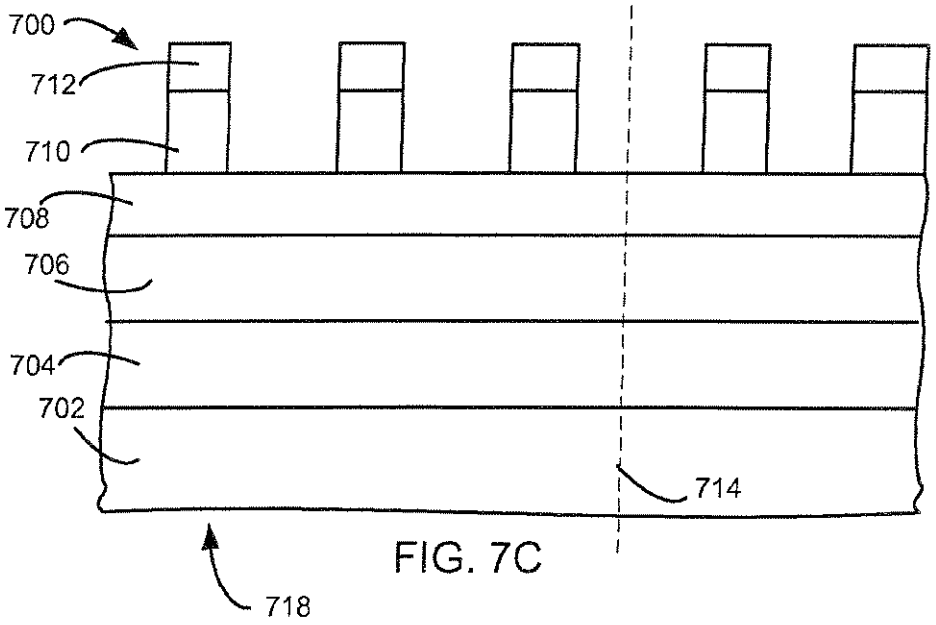

700
712
710
708
706
704
702
714
718

FIG. 7C

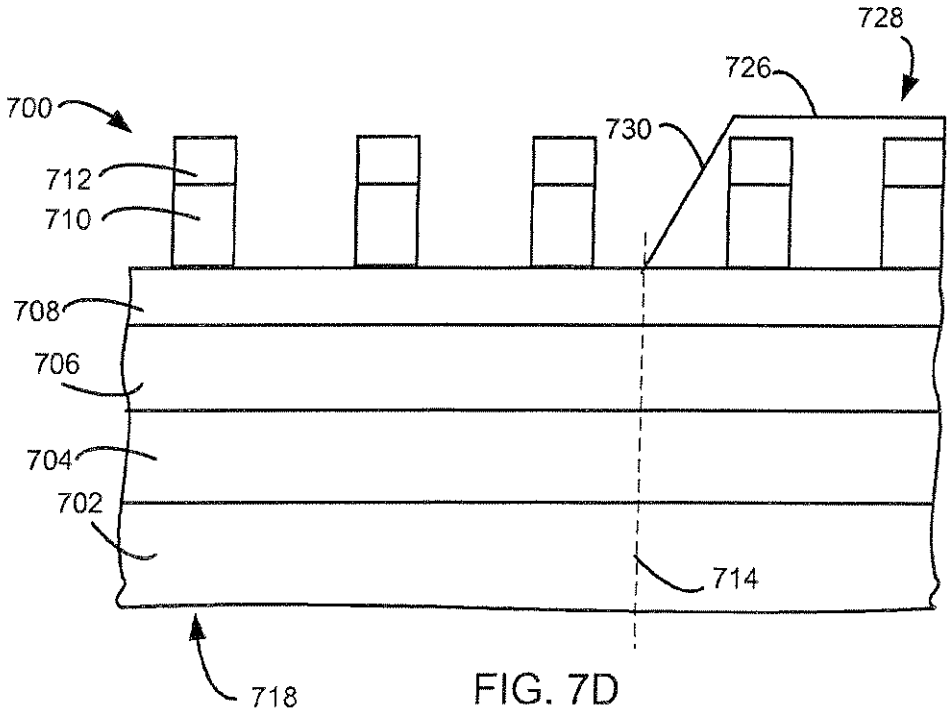

728
726
730
700
712
710
708
706
704
702
714
718

FIG. 7D

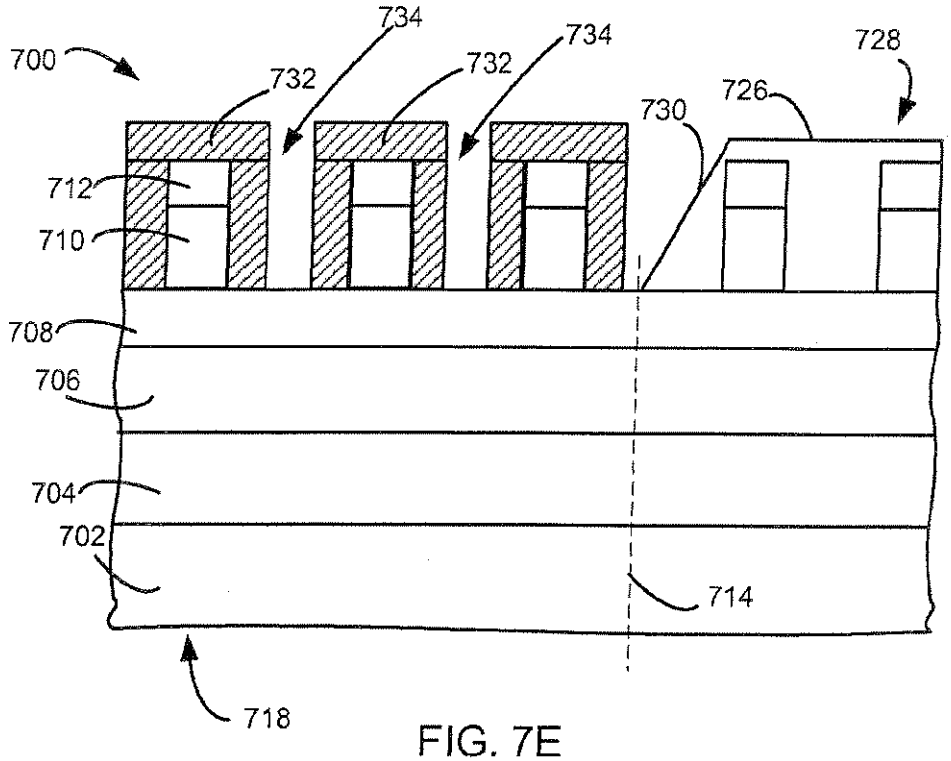

700
734
732
732
734
728
726
730
712
710
708
706
704
702
714
718

FIG. 7E

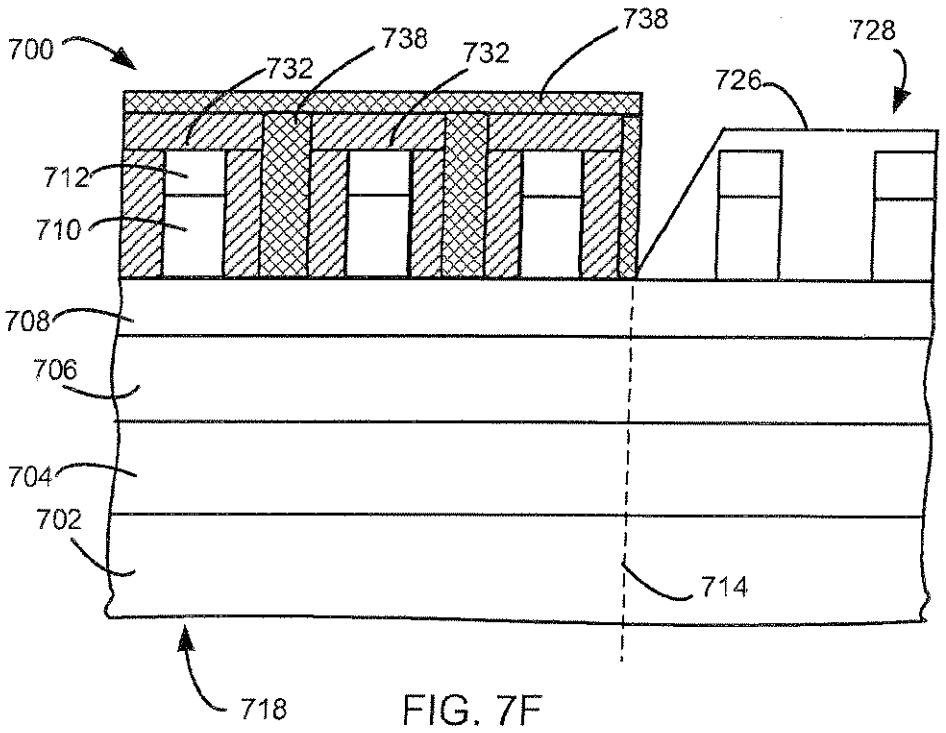

700
738
732
732
738
728
726
712
710
708
706
704
702
714
718

FIG. 7F

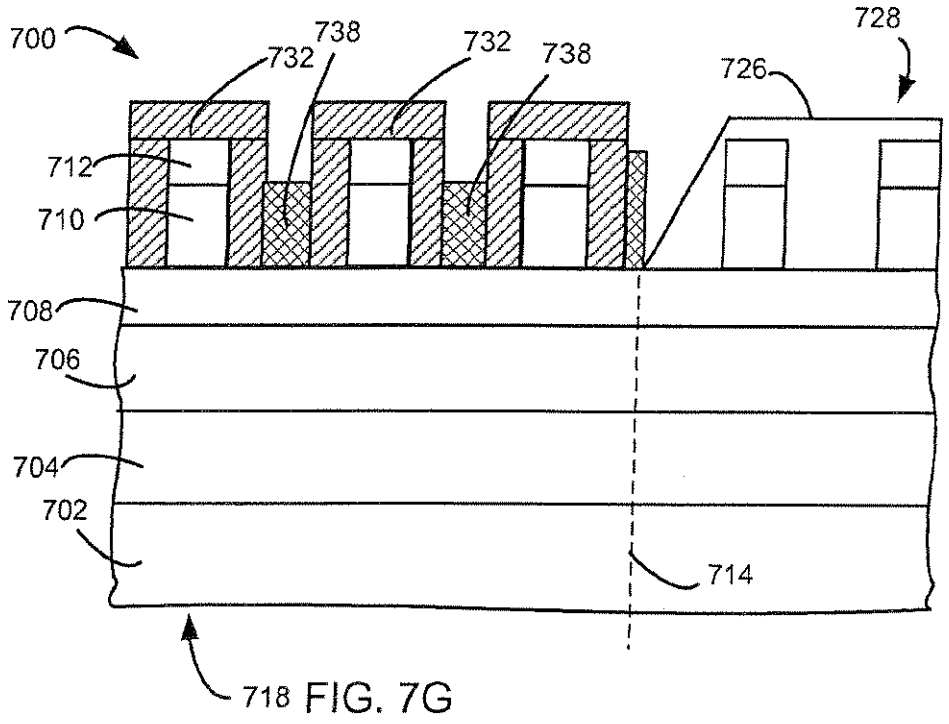

700
738
732
732
738
728
726
712
710
708
706
704
702
714
718

FIG. 7G

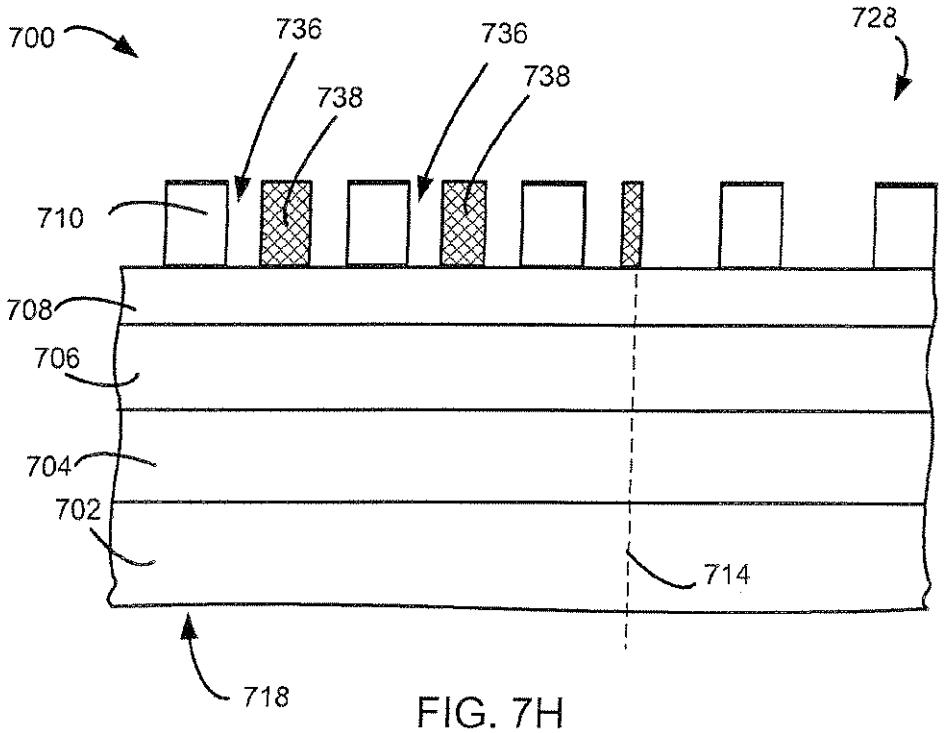

700
736
736
738
738
728
710
708
706
704
702
714
718

FIG. 7H

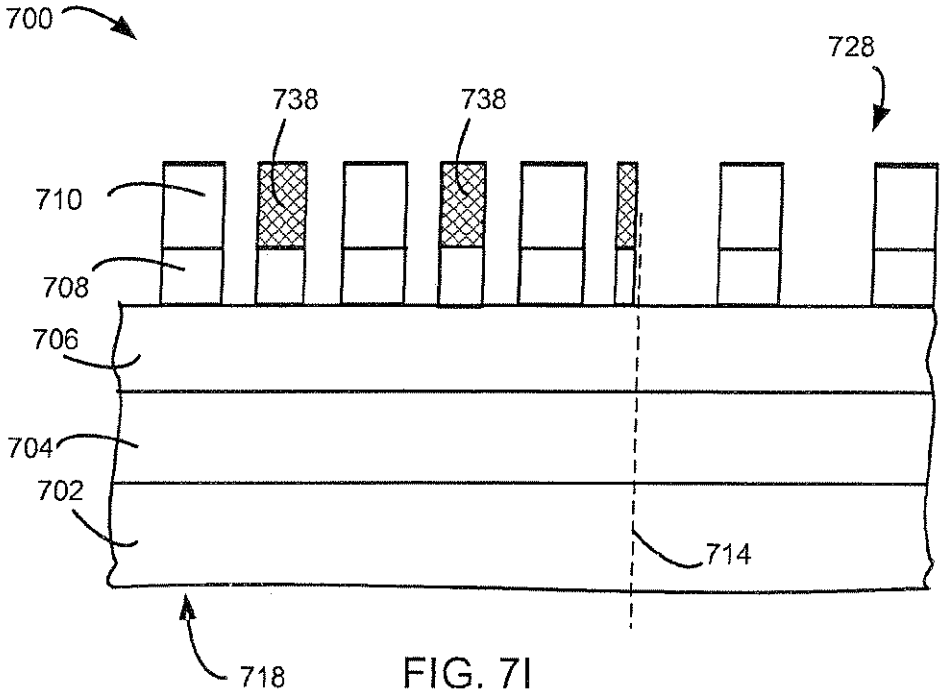

700
728
738
738
710
708
706
704
702
714
718

FIG. 7I

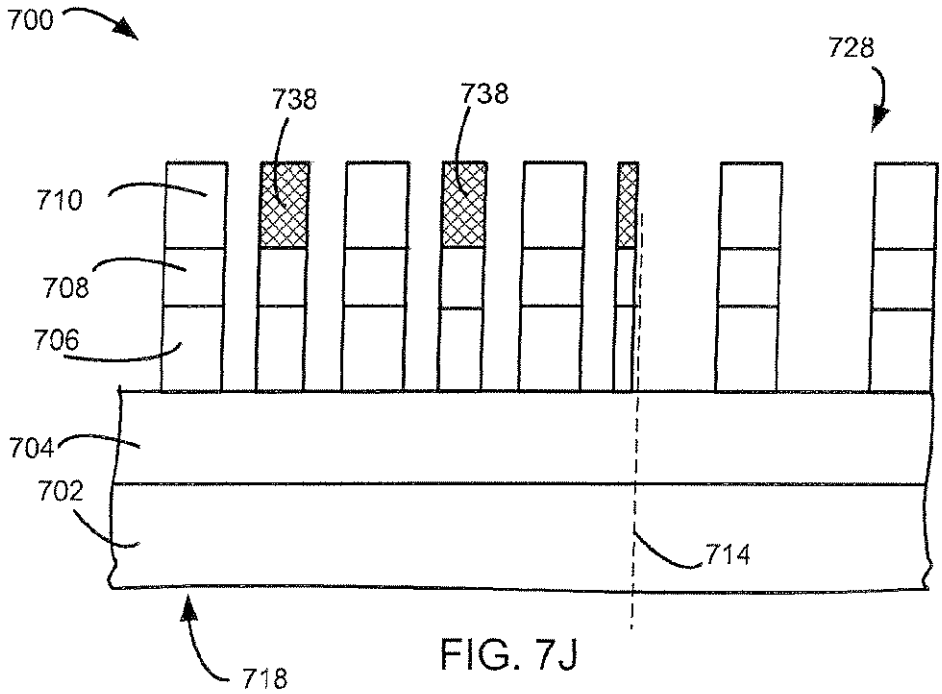

700
728
738
738
710
708
706
704
702
714
718

FIG. 7J

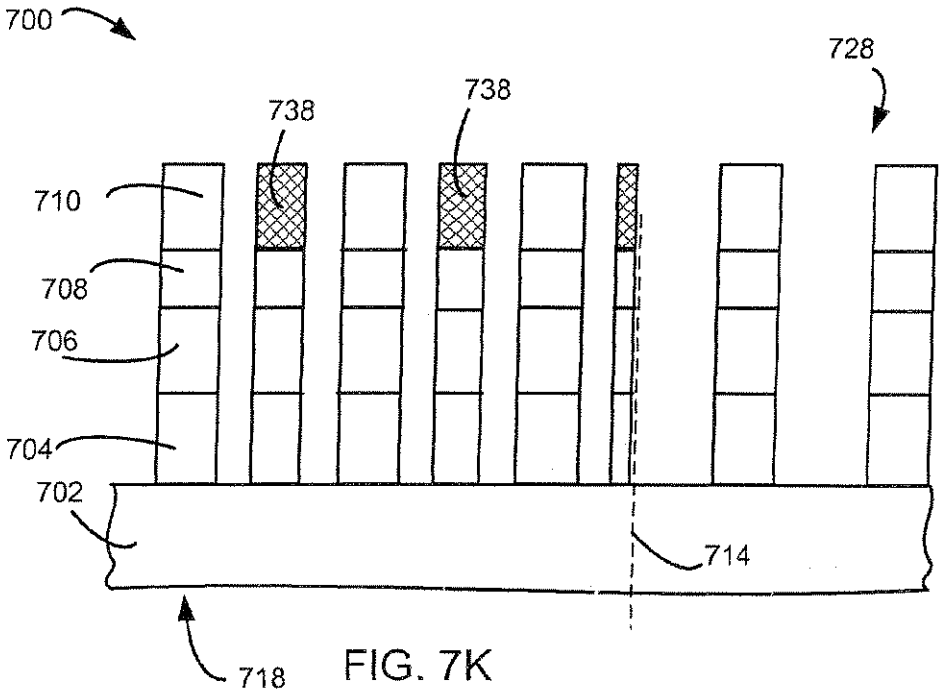


FIG. 7K

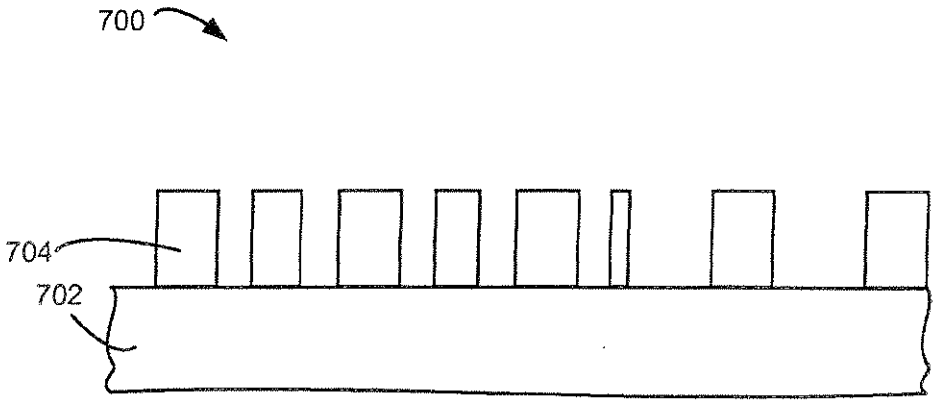


FIG. 7L