HIGH PERFORMANCE SILICON CONTACT FOR FLIP CHIP

FIELD OF THE INVENTION

This invention relates to integrated circuitry interconnect lines, in particular, to through-wafer, integrated circuitry interconnect lines.

DISCUSSION OF THE RELATED ART

Semiconductor devices are typically fabricated on a wafer which is subsequently tested and separated into individual dies or chips. Individual dies are then packaged. Packaged chips are then assembled together, typically on a printed circuit board (PCB), and electrically interconnected to perform a desired function. The electrical interconnection of separately fabricated chips generally takes place externally of the individual chips. While PCB techniques are useful for bringing together separately fabricated and assembled chips, doing so brings with it some problems which are not so easily overcome. For example, PCBs consume a large amount of physical space compared to the circuitry of the chips which are mounted to them. It is desirable to reduce the amount of physical space required by such PCBs. Further, assuring the

electrical integrity of interconnections between chips mounted on PCBs is a challenge. Moreover, in certain applications, it is desirable to reduce the physical length of electrical interconnections between devices because of concerns with signal loss or dissipation and interference with and by other integrated circuitry devices.

A continuing challenge in the semiconductor industry is to find new, innovative, and efficient ways of forming electrical connections with and between circuit devices which are fabricated on the same and on different dies. Relatedly, continuing challenges are posed to find and/or improve upon the packaging techniques utilized to package integrated circuitry devices, particularly as device dimensions continue to shrink.

SUMMARY OF THE INVENTION

The present invention provides coaxial interconnect lines which are more reliable and better accommodate reduced circuitry dimensions and a method of forming such coaxial interconnect lines.

A semiconductive substrate is provided which includes front and back surfaces, and a hole which extends through the substrate and between the front and back surfaces. The hole is defined in part by an interior wall portion. Conductive material is formed proximate at least some of the interior wall portion. This conductive material provides an outer coaxial line component. Subsequently, a layer of dielectric material is formed within the hole, over and radially inwardly of the conductive material. A second conductive material is then formed within the hole over and radially inwardly of the dielectric material layer. The latter conductive material constitutes an inner conductive coaxial line component.

In a preferred implementation, the inner conductive coaxial line component is formed by forming a first conductive material within the hole. A second material is formed over the first material, with at least the

second material being a seed layer. Subsequently, a metal-containing layer is electroplated onto the seed layer.

The substrate may be used as a chip carrier, or the substrate may have circuit components fabricated thereon and itself be formed an integrated circuit chip.

BRIEF DESCRIPTION OF THE DRAWINGS

The above advantages and features of the invention will be more clearly understood from the following detailed description which is provided in connection with the accompanying drawings.

Figure 1 is a cross-sectional view of a semiconductor wafer fragment at one processing step in accordance with the invention;

Figure 2 is a cross-sectional view of the semiconductor wafer fragment at a processing step subsequent to that shown by Figure 1;

Figure 3 is a cross-sectional view of the semiconductor wafer fragment at a processing step subsequent to that shown by Figure 1;

Figure 4 is a cross-sectional view of the semiconductor wafer fragment at a processing step subsequent to that shown by Figure 3;

Figure 5 is a cross-sectional view of the semiconductor wafer fragment at a processing step subsequent to that shown by Figure 4;

Figure 6 is a cross-sectional view of the semiconductor wafer fragment at an alternate processing step subsequent to that shown by Figure 5;

Figure 7 is a cross-sectional view of the semiconductor wafer fragment at a processing step subsequent to that shown by Figure 6;

Figure 8 is a cross-sectional view of the semiconductor wafer fragment at a processing step subsequent to that shown by Figure 7;

Figure 9 is a cross-sectional view of the semiconductor wafer fragment of Figure 8 including circuit devices fabricated on the wafer;

Figure 10 is a cross-sectional view of the semiconductor wafer fragment of Figure 8 including integrated circuit chips mounted on the wafer; and

Figure 11 is a processor based system employing the through-hole, coaxial interconnections in accordance with an exemplary embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Exemplary embodiment of the present invention will be described below in connection with the drawings. Other embodiments may be utilized and structural or logical changes may be made without departing from the spirit or scope of the present invention. Although exemplary process conditions for forming various material layers are described below, these are only representative and are not meant to be considered as limiting the invention. Like items are referred to by like reference numerals throughout the drawings.

The term "substrate" used in the following description may include any semiconductor-based structure that has an exposed semiconductor surface. Semiconductor-based structure must be understood to include silicon, silicon-on insulator (SOI), silicon-on sapphire (SOS), doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor structure foundation, and other

semiconductor structures. The semiconductor-based structures need not be silicon-based. The semiconductor could be silicon-germanium, germanium, or gallium arsenide. When reference is made to substrate in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor or foundation.

Referring to Figure 1, a semiconductor wafer fragment is indicated generally at 10 and includes a semiconductor substrate 12. Substrate 12 includes a first or front surface 14 and a second or back surface 16. In one aspect, substrate 12 is a semi-conductor structure having first and second outwardly-facing surfaces 14, 16, at least one of which is capable of supporting fabricated integrated circuitry. Substrate 12 may be formed of a monocrystalline silicon wafer.

Referring to Figure 2, a plurality of holes or passageways 18, 20, and 22 are formed within substrate 12 between front and back surfaces 14, 16. Each hole or passageway is defined, at least in part, by a respective interior wall portion 19, 21, and 23. The illustrated interior wall portions constitute interior hole surfaces which join with first and second surfaces 14, 16. Holes 18, 20, and 22 can be formed through any suitable

processing techniques, with one being described below with reference to Figures 3 and 4.

Referring to Figure 3, substrate 12 is shown at a processing step which is applied to the Figure 1 construction and which precedes the Figure 2 construction. A layer 24 of masking material, such as photoresist, is formed over front surface 14 and is suitably patterned to define a plurality of openings 26, 28, and 30. Openings 26, 28, and 30 are formed over a substrate area in which holes 18, 20, and 22 (Figure 2) are to be formed. An alkaline etch can be conducted which is effective to form a pattern of pre-defined etch pits 32, 34, and 36. Subsequently, masking material layer 24 is stripped away.

Referring to Figure 4, a through wafer silicon trench etch is next performed to form holes 18, 20 and 22, using a high density low pressure (HDLP) reactive ion etching (RIE) at a rate of about 2.2 μm/min. using SF_6/C_4F_8. A photoresist can be used as a mask for this etching. Continuous etching/passivation cycles are used to achieve anisotropic, high aspect ratio trenches. In one embodiment, exemplary aspect ratios can be

greater than about 100. More preferably, aspect ratios can be greater than about 200.

Referring to Figure 5, outer conductive sheaths 50 are formed within holes or passageways 18, 20, and 22 and over respective interior wall portions 19, 21, and 23. Sheaths 50 are preferably formed by depositing a layer 54 of metal-containing material over the substrate, within the holes and over the respective wall portions 19, 21, and 23 thereof. Any suitable method of providing such metal-containing layer can be utilized. An exemplary method includes a low-pressure chemical vapor deposition (LPCVD) of tungsten in a self-limiting process which provides a tungsten film by silicon reduction. Accordingly, silicon material within holes 18, 20, and 22 is replaced by tungsten atoms in a WF_6 reaction gas, with a reaction product SiF_4 being pumped out or otherwise removed from the deposition chamber. Subsequently, such can be followed by silane or polysilane reduction of the WF_6 until a desired conductor thickness is reached. In a preferred embodiment, the thickness of layer 54 is about 0.3 μm to about 0.5 μm. Deposition rates in accordance with the above are dependent upon the temperature and the reaction gas flow rate. Exemplary deposition

rates are 1 micron per minute, at temperatures of about 300°C. and with a flow rate of WF_6 at 4 sccm in a cold wall CVD reactor.

Referring to Figure 6, a dielectric material layer 56 is formed over layer 54 and within holes 18, 20, and 22. Portions of layer 56 are thereby formed radially inwardly of interior wall portions 19, 21, and 23 and outer conductive sheath 50. An exemplary dielectric material is SiO_2. Alternately, dielectric layer 56 can comprise a nitride-containing layer, such as Si_3N_4, which is disposed proximate respective interior wall portions 19, 21, and 23. An oxide-containing layer is formed over the nitride-containing layer to provide a dielectric SiON layer within the hole. In a preferred implementation, the nitride layer is formed by chemical vapor deposition, and the oxide layer by exposing the substrate to oxidizing conditions. Specifically, in the preferred implementation, dielectric layers 56 constitute a reoxidized LPCVD nitride film which forms the illustrated and preferred SiON dielectric layer. An exemplary processing implementation includes in-situ nitridation in an ammonia atmosphere at 950°C. Low pressure chemical vapor deposition of nitride at 700°C. takes place with dichlorosilane and ammonia until about two-thirds of the hole

diameter is filled. Subsequently, reoxidation of the nitride takes place at a temperature of between 900°C. to 950°C.

Referring to Figure 7, a first layer of conductive material 58 is formed over dielectric layer 56 and within each respective hole 18, 20, and 22. In a preferred aspect, such first conductive material constitutes polysilicon which is formed through suitable chemical vapor deposition techniques. Accordingly, such first conductive material is formed over and radially inwardly of dielectric material layer 56 within holes 18, 20, and 22. A second layer of conductive material 60 is formed over the substrate 12 and first material 58. In one aspect, second conductive material 60 comprises a metal material which is different from the first conductive material 58. In a preferred aspect, second conductive material 60 constitutes a copper seed layer which is formed over first conductive material 58. Such material or film can be deposited through suitable sputtering or evaporation techniques. Mechanical masks can be utilized to define with more particularity the area over which the preferred copper-seed layer is deposited. Second material 60 is preferably deposited over front and back surfaces 14, 16 to a thickness of about 20 to about 40 nm. Next, a metal layer, preferably a copper layer is electroplated onto seed-

layer 60 to form layer 62 which completely fills in holes 18, 20 and 22. Preferably, layer 62 is formed to a thickness of about 2-3 μm.

Referring to Figure 8, layers 54, 55, 58, 60 and 62 are planarized relative to substrate 12 and isolated within respective holes 18, 20, and 22. Such can be accomplished by any suitable processing techniques. Exemplary techniques include abrasion of the substrate as by chemical mechanical polishing.

Hence, a method of forming integrated circuitry lines such as coaxial integrated circuitry interconnect lines is described. A semiconductive substrate is provided which includes front and back surfaces, and a hole is formed which extends through the substrate and between the front and back surfaces. The hole is defined in part by an interior wall portion. Conductive material is formed proximate at least some of the interior wall portion to form an outer conductive layer. Subsequently, a layer of dielectric material is formed within the hole, over and radially inwardly of the conductive material. A second conductive material is then formed within the hole over and radially inwardly of the dielectric material layer. The latter conductive material constitutes an inner

conductive coaxial line component. In a preferred implementation, the inner conductive coaxial line component is formed by forming a first conductive material within the hole. A second conductive material is formed over the first conductive material, with at least the second material being a seed layer. Subsequently, a metal-containing layer is electroplated onto the seed layer.

Referring to Figures 9 and 10, substrate 12 may also support fabricated circuit devices 64 and multi-layer wiring patterns and may be encapsulated by encapsulant 68 in a single integrated package. In such an implementation multiple exterior terminals 70 are provided for connecting interior packaged conductors to an external circuit. In addition, substrate 12 may be a carrier which is used to mount, support and interconnect other integrated circuit chips 66 mounted over one or both of the surfaces 14, 16.

Figure 11 illustrates a processor system 102, including central processing unit (CPU) 112, RAM and ROM memory devices 108, 110, input/output (I/O) devices 104, 106, floppy disk drive 114 and CD ROM drive 116. All of the above components communicate with each other over one or more bus systems 118. One or more of the central processing unit

(CPU) 112, RAM and ROM memory devices 108, 110 are fabricated on substrate 12 or as IC chips which are mounted on a substrate 12 carrier, as illustrated in Figures 9 and 10, with through-hole, coaxial interconnections in accordance with the invention. In addition, RAM 108 may be constructed as one or more memory modules each containing one or more memory circuits containing coaxial interconnections fabricated in accordance with the invention.

Although the invention has been described above in connection with exemplary embodiments, it is apparent that many modifications and substitutions can be made without departing from the spirit or scope of the invention. Accordingly, the invention is not to be considered as limited by the foregoing description, but is only limited by the scope of the appended claims.

What is claimed is

1. A method of forming coaxial integrated circuitry interconnect lines comprising:

providing a substrate having front and back surfaces;

forming a hole with sidewalls extending through said substrate from said front to said back surface;

forming an outer conductive coaxial sheath on said sidewalls;

forming a coaxial dielectric layer radially inward and over said outer conductive coaxial sheath; and

forming an inner coaxial line radially inward and over said coaxial dielectric layer wherein forming an inner coaxial line further comprises forming an inner conductive layer, forming a seed layer over said inner conductive layer, and electroplating a metal on said seed layer.

2. The method of claim 1 wherein said outer conductive coaxial sheath is a tungsten sheath.

3. The method of claim 2 wherein said outer conductivecoaxial sheath is formed by low pressure chemical vapor deposition.

4. The method of claim 3 wherein said deposition is performed at a rate of about 1 micron per minute.

5. The method of claim 3 wherein said outer conductive coaxial sheath is formed to a thickness of about 0.3 μm to about 0.5 μm.

6. The method of claim 1 wherein said coaxial dielectric layer comprises silicon dioxide.

7. The method of claim 1 wherein said coaxial dielectric layer is formed to a thickness of about 0.5 μm to about 0.8 μm.

8. The method of claim 1 wherein said coaxial dielectric layer comprises a nitride containing layer.

9. The method of claim 8 wherein said nitride containing layer is formed by low pressure chemical vapor deposition.

10. The method of claim 1 wherein said inner conductive layer is a polysilicon layer.

11. The method of claim 1 wherein said seed layer is formed to a thickness of about 20 nm-40 nm.

12. The method of claim 1 wherein said metal is copper.

13. The method of claim 1 wherein said electroplated metal is about 2-3 μm thick.

14. The method of claim 1 further comprising the act

of fabricating circuit devices on said substrate.

15. The method of claim 1 further comprising the act of mounting integrated circuit chips on said substrate.

16. The method of claim 15 further comprising the act of encapsulating said integrated circuit chip and substrate.

17. An integrated circuitry interconnect line comprising:

a substrate having front and back surfaces;

a hole with sidewalls extending through said substrate from said front to said back surface;

an outer conductive coaxial sheath formed on said sidewalls;

a coaxial dielectric layer formed radially inward and over said outer coaxial sheath; and

an inner conductive coaxial line formed radially inward and over said coaxial dielectric layer, wherein said inner conductive coaxial line has electrical contacts on said front and back surfaces of said substrate.

18. An integrated circuitry interconnect line comprising:

a substrate having front and back surfaces;

a hole with sidewalls extending through said substrate from said front to said back surface;

an outer conductive coaxial sheath formed on said sidewalls;

a coaxial dielectric layer formed radially inward and over said outer coaxial sheath; and

an inner conductive coaxial line formed radially inward and over said coaxial dielectric layer, wherein said inner conductive coaxial line comprises an inner conductive layer, a seed layer provided over said inner conductive layer, and an electroplated metal layer on said seed layer.

19. The interconnect line of claim 18 wherein said outer conductive sheath comprises a tungsten layer.

20. The interconnect line of claim 18 wherein said outer conductive sheath is formed to a thickness of about 0.3 μm to about 0.5 μm.

21. The interconnect line of claim 18 wherein said dielectric layer comprises silicon dioxide.

22. The interconnect line of claim 18 wherein said dielectric layer is formed to a thickness of about 0.5 um to about 0.8 um.

23. The interconnect line of claim 18 wherein said dielectric layer comprises a nitride containing layer.

24. The interconnect line of claim 18 wherein said

dielectric layer comprises silicon nitride.

25. The interconnect line of claim 18 wherein said inner conductive layer is a polysilicon layer.

26. The interconnect line of claim 18 wherein said seed layer is formed to a thickness of about 20 nm-40 nm.

27. The interconnect line of claim 18 wherein said metal is copper.

28. The interconnect line of claim 18 wherein said electroplated layer is about 2-3 μm thick.

29. A processor system comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said integrated circuit and processor comprising:

a substrate having front and back surfaces and a hole with sidewalls extending through said substrate from said front to said back surface;

a conductive outer coaxial sheath formed on said sidewalls;

a coaxial dielectric layer formed radially inward and over said outer coaxial sheath; and

an inner conductive coaxial line formed radially inward and over said coaxial dielectric layer, said inner conductive coaxial line comprising an

inner conductive layer, a seed layer provided over said inner conductive layer, and an electroplated metal layer on said seed layer.

30. The system of claim 29 wherein said conductive outer coaxial sheath is a tungsten sheath.

31. The system of claim 29 wherein said conductive outer coaxial sheath is formed to a thickness of about 0.3 μm to about 0.5μm.

32. The system of claim 29 wherein said coaxial dielectric layer comprises silicon dioxide.

33. The system of claim 29 wherein said coaxial dielectric layer is formed to a thickness of about 0.5 μm to about 0.8 μm.

34. The system of claim 29 wherein said coaxial dielectric layer comprises a nitride containing layer.

35. The system of claim 29 wherein said coaxial dielectric layer comprises silicon nitride.

36. The system of claim 29 wherein said inner conductive layer is a polysilicon layer.

37. The system of claim 29 wherein said seed layer is formed to a thickness of about 20 nm-40 nm.

38. The system of claim 29 wherein said electroplated metal layer is copper.

39. The system of claim 29 wherein said electroplated metal

layer is about 2-3 μm thick.

40. An integrated circuit package comprising:

a substrate supporting at least one integrated circuit chip, said substrate having front and back surfaces and at least a hole with sidewalls extending through said substrate from said front to said back surface;

an outer conductive coaxial sheath formed on said sidewalls;

a coaxial dielectric layer formed radially inward and over said outer conductive coaxial sheath; and

an inner conductive coaxial line formed radially inward and over said coaxial dielectric layer; and

a package which encases said substrate and said at least one chip.

41. The integrated circuit of claim 40 wherein said inner coaxial line further comprises:

an inner conductive layer;

a seed layer provided over said inner conductive layer; and

an electroplated metal layer on said seed layer.

42. The integrated circuit of claim 40 wherein said conductive sheath is a tungsten sheath.

43. The integrated circuit of claim 40 wherein said sheath is formed to a thickness of about 0.3 μm to about 0.5 μm.

44. The integrated circuit of claim 40 wherein said dielectric

layer comprises silicon dioxide.

45. The integrated circuit of claim40 wherein said dielectric layer is formed to a thickness of about 0.5 μm to about 0.8 μm.

46. The integrated circuit of claim 40 wherein said dielectric layer comprises a nitride containing layer.

47. The integrated circuit of claim 40 wherein said dielectric layer comprises silicon nitride.

48. The integrated circuit of claim 41 wherein said inner conductive layer is a polysilicon layer.

49. The integrated circuit of claim 41 wherein said seed layer is formed to a thickness of about 20 nm-40 nm.

50. The integrated circuit of claim 41 wherein said metal is copper.

51. The integrated circuit of claim 41 wherein said electroplated layer is about 2-3 μm thick.