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(71) Applicant *(for all designated States except US)*: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **DOUGLAS, Jonathan, P.** [US/US]; 10500 NW Cornell Road, Portland, OR 97229 (US). **DELEGANES, Daniel, J.** [US/US]; 5264 NE Corral Court, Hillsboro, OR 97229 (US). **HADLEY, James, D.** [US/US]; 15474 NW Sweetgale Court, Portland, OR 97229 (US).

(74) Agents: **MALLIE, Michael, J.** et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

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ACTION

(54) Title: METHOD AND APPARATUS FOR MULTI-THREAD PIPELINED INSTRUCTION DECODER

(57) Abstract: A multithread pipelined instruction decoder to clock, clear and stall an instruction decode pipeline of a multi-threaded machine to maximize performance and minimize power. A shadow pipeline shadows the instruction decode pipeline maintaining at the thread-identification and instruction-valid bits for each pipestage of the instruction decoder. The thread-id and valid bits are used to control the clear, clock, and stall of each pipestage of the instruction decoder. Instructions of one thread can be cleared without impacting instructions of another thread in the decode pipeline. In some cases, instructions of one thread can be stalled without impacting instructions of another thread in the decode pipeline. In the present invention, pipestages are clocked only when a valid instruction needs to advance in order to conserve power and to minimize stalling.

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