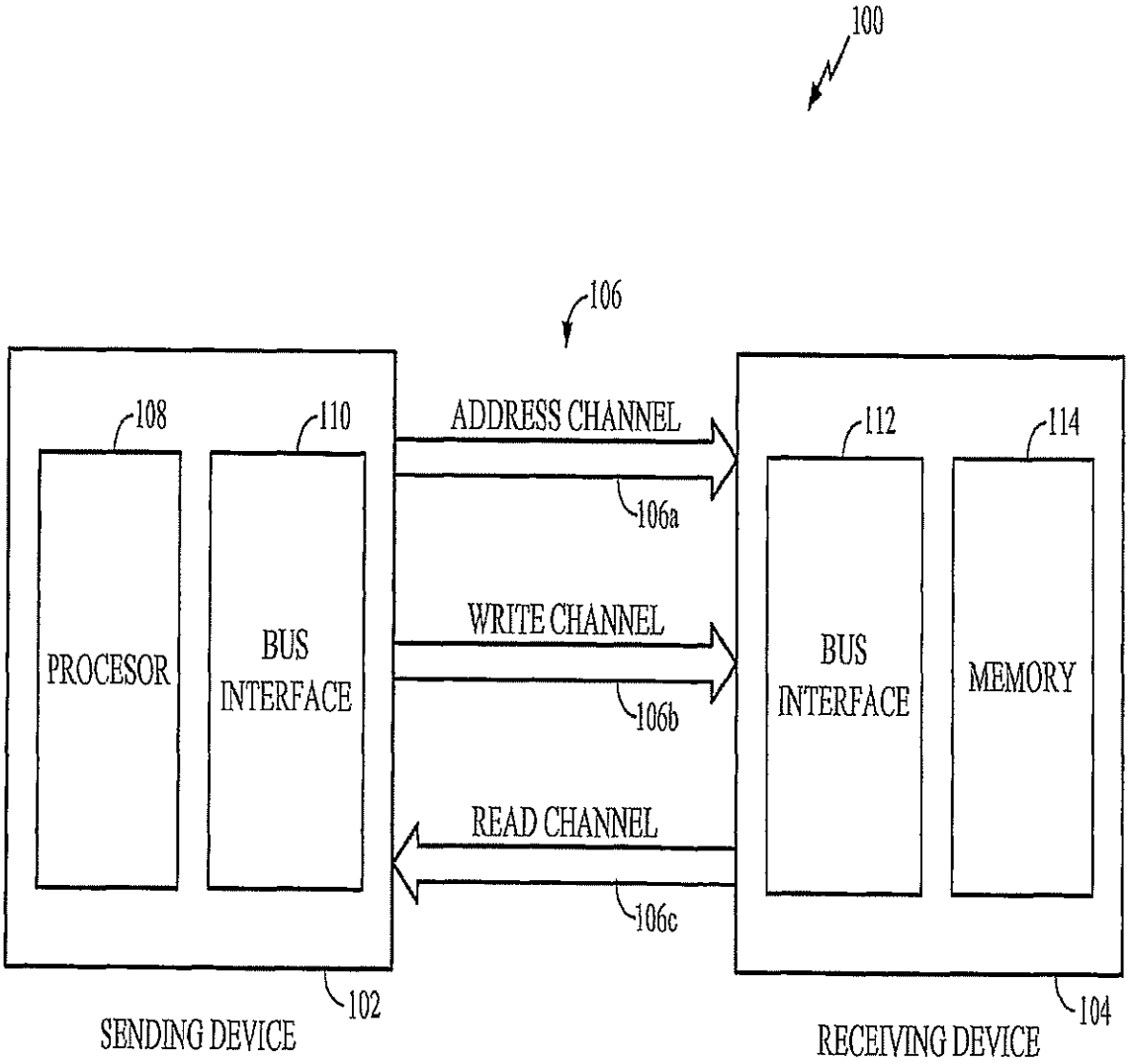

100
106
108
110
ADDRESS CHANNEL
112
114
106a
WRITE CHANNEL
PROCESOR
BUS INTERFACE
BUS INTERFACE
MEMORY
106b
READ CHANNEL
106c
102
104
SENDING DEVICE
RECEIVING DEVICE

FIG. 1

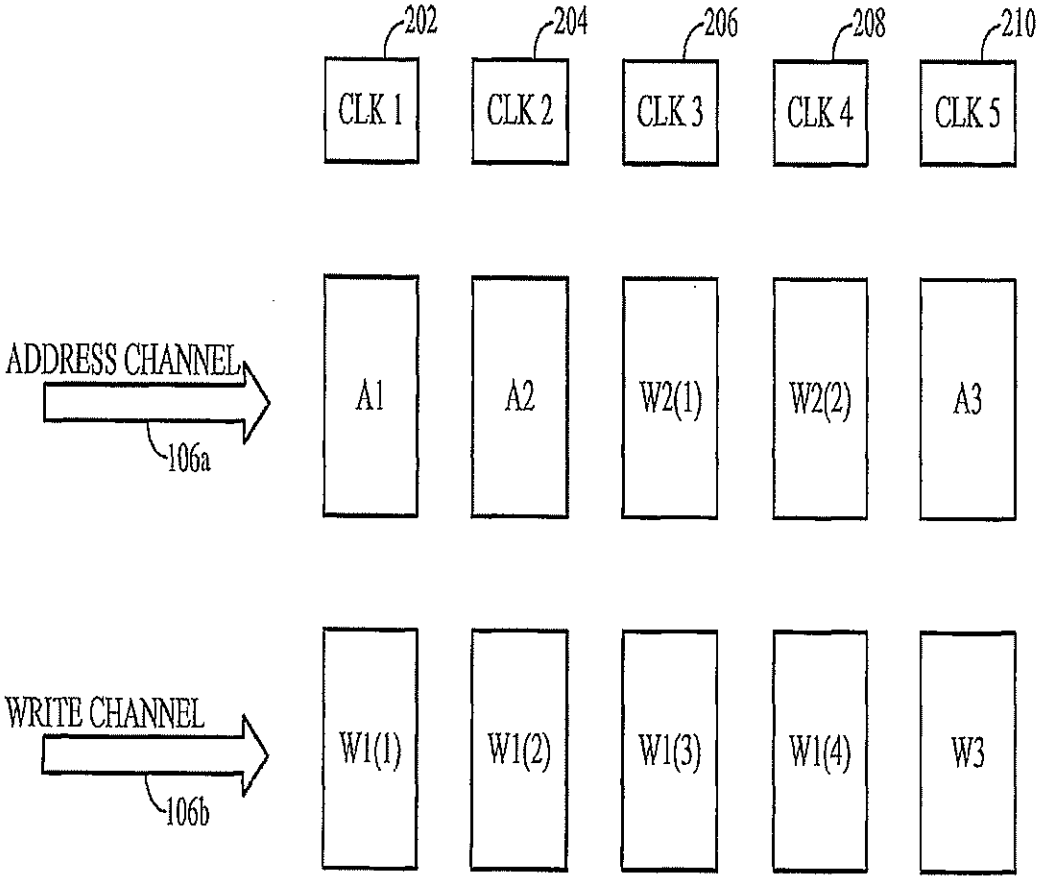

202
204
206
208
210
CLK 1
CLK 2
CLK 3
CLK 4
CLK 5
ADDRESS CHANNEL
106a
A1
A2
W2(1)
W2(2)
A3
WRITE CHANNEL
106b
W1(1)
W1(2)
W1(3)
W1(4)
W3

FIG. 2

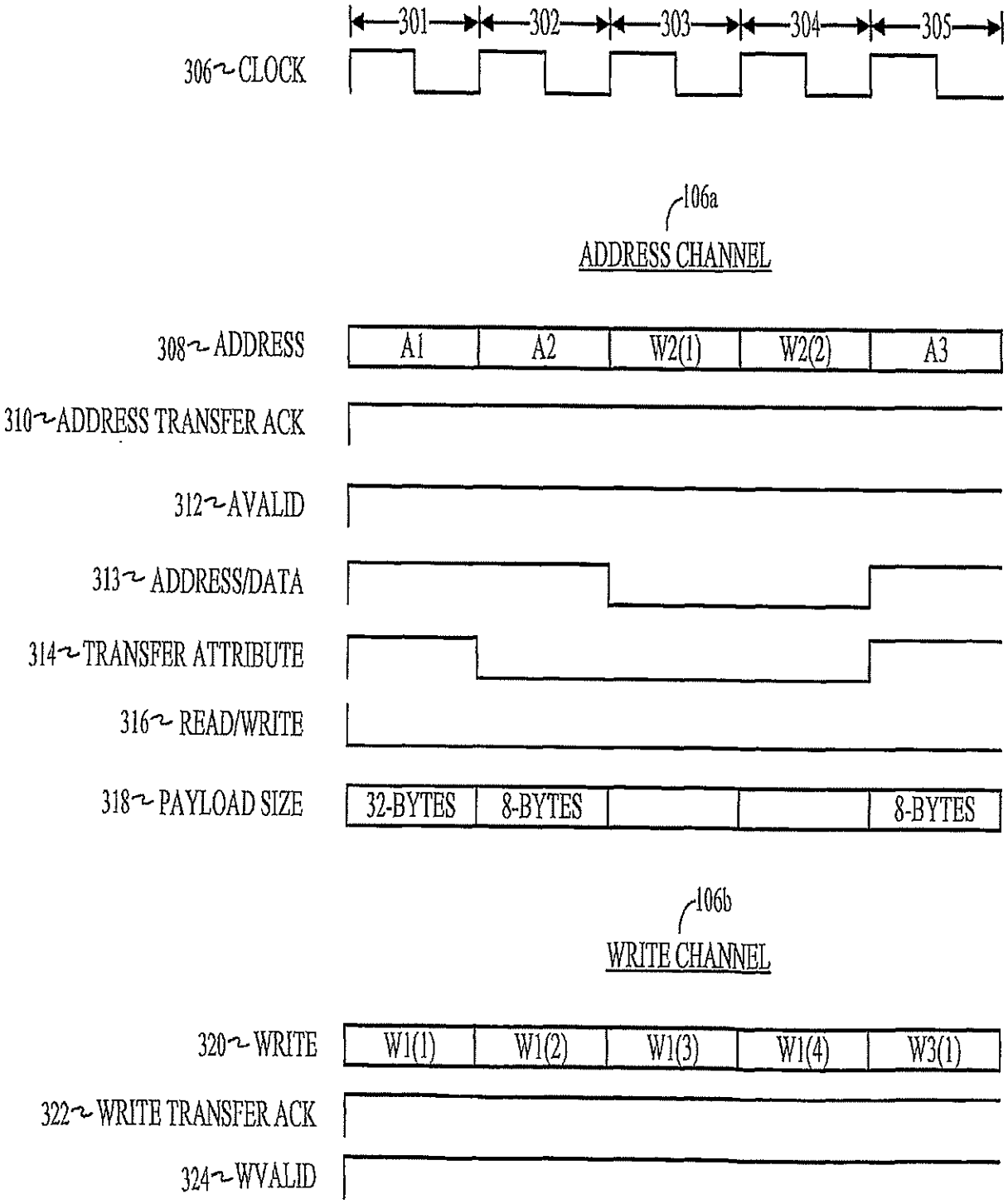

301
302
303
304
305
306 CLOCK
106a
ADDRESS CHANNEL
308 ADDRESS
A1
A2
W2(1)
W2(2)
A3
310 ADDRESS TRANSFER ACK
312 AVALID
313 ADDRESS/DATA
314 TRANSFER ATTRIBUTE
316 READ/WRITE
318 PAYLOAD SIZE
32-BYTES
8-BYTES
8-BYTES
106b
WRITE CHANNEL
320 WRITE
W1(1)
W1(2)
W1(3)
W1(4)
W3(1)
322 WRITE TRANSFER ACK
324 WVALID

FIG. 3

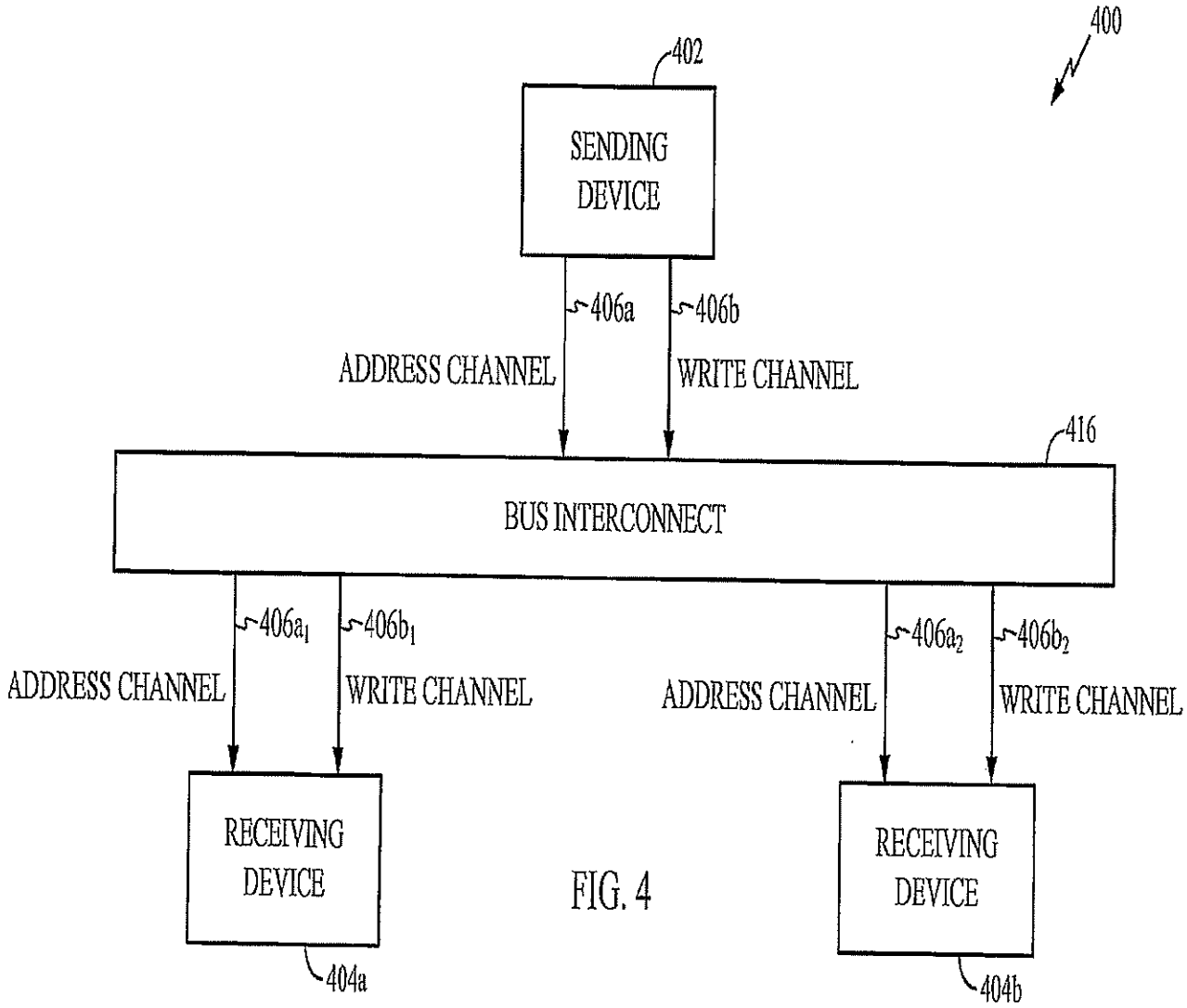

400
402
SENDING DEVICE
406a
406b
ADDRESS CHANNEL
WRITE CHANNEL
416
BUS INTERCONNECT
406a1
406b1
406a2
406b2
ADDRESS CHANNEL
WRITE CHANNEL
ADDRESS CHANNEL
WRITE CHANNEL
RECEIVING DEVICE
RECEIVING DEVICE
404a
404b

FIG. 4

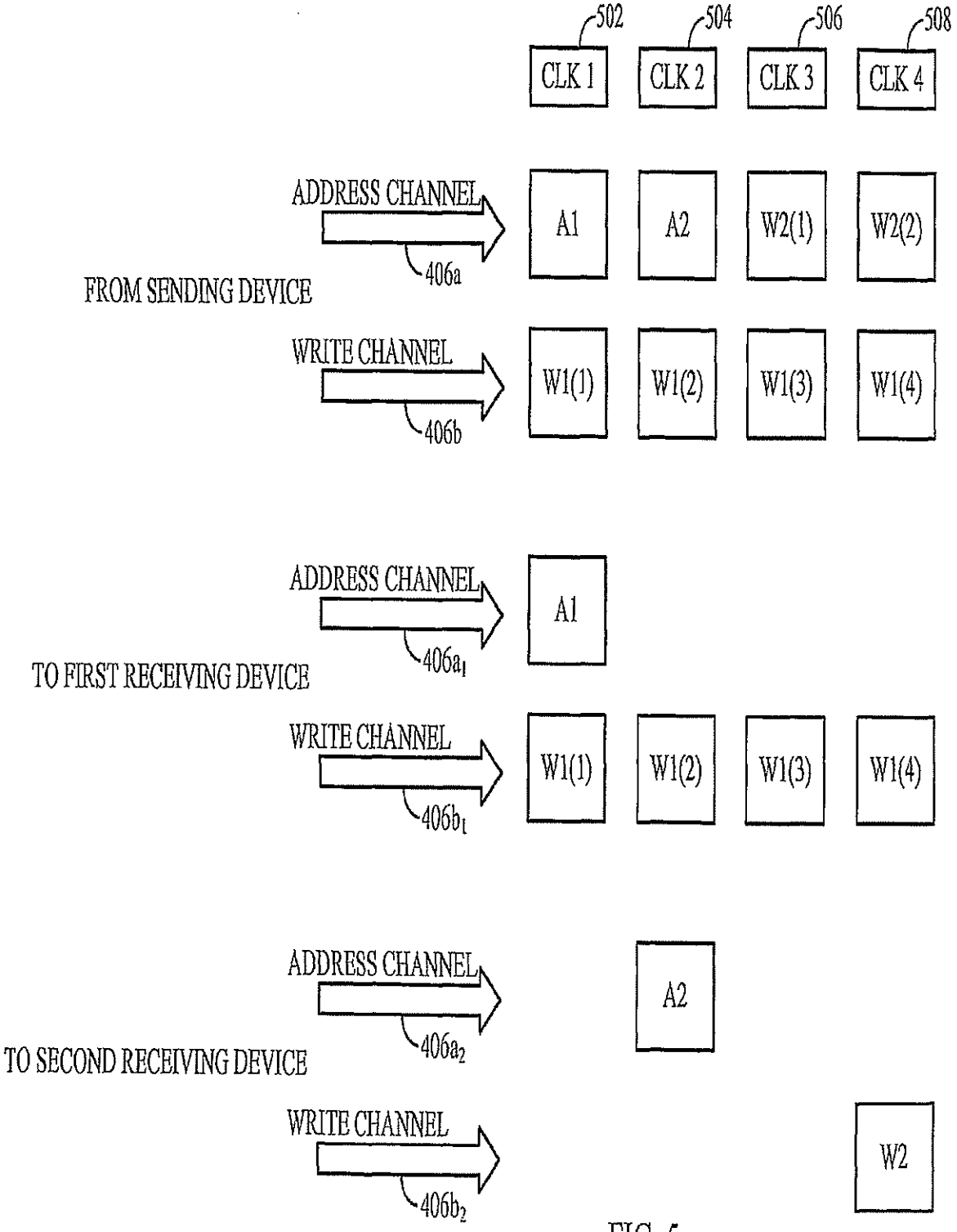

502
504
506
508
CLK 1
CLK 2
CLK 3
CLK 4
ADDRESS CHANNEL
406a
FROM SENDING DEVICE
A1
A2
W2(1)
W2(2)
WRITE CHANNEL
406b
W1(1)
W1(2)
W1(3)
W1(4)
ADDRESS CHANNEL
406a1
TO FIRST RECEIVING DEVICE
A1
WRITE CHANNEL
406b1
W1(1)
W1(2)
W1(3)
W1(4)
ADDRESS CHANNEL
406a2
TO SECOND RECEIVING DEVICE
A2
WRITE CHANNEL
406b2
W2

FIG. 5

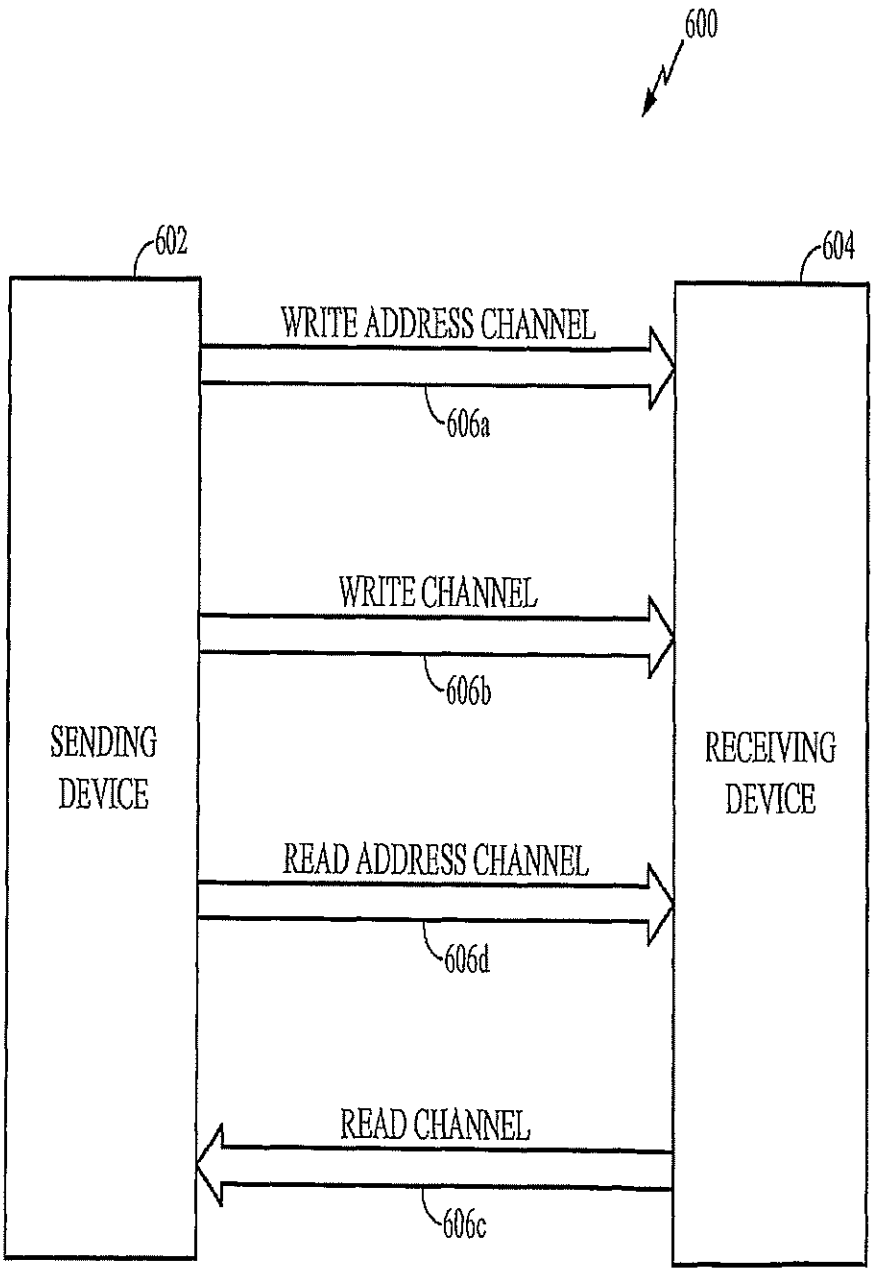

600
602
604
WRITE ADDRESS CHANNEL
606a
WRITE CHANNEL
606b
SENDING DEVICE
RECEIVING DEVICE
READ ADDRESS CHANNEL
606d
READ CHANNEL
606c

FIG. 6

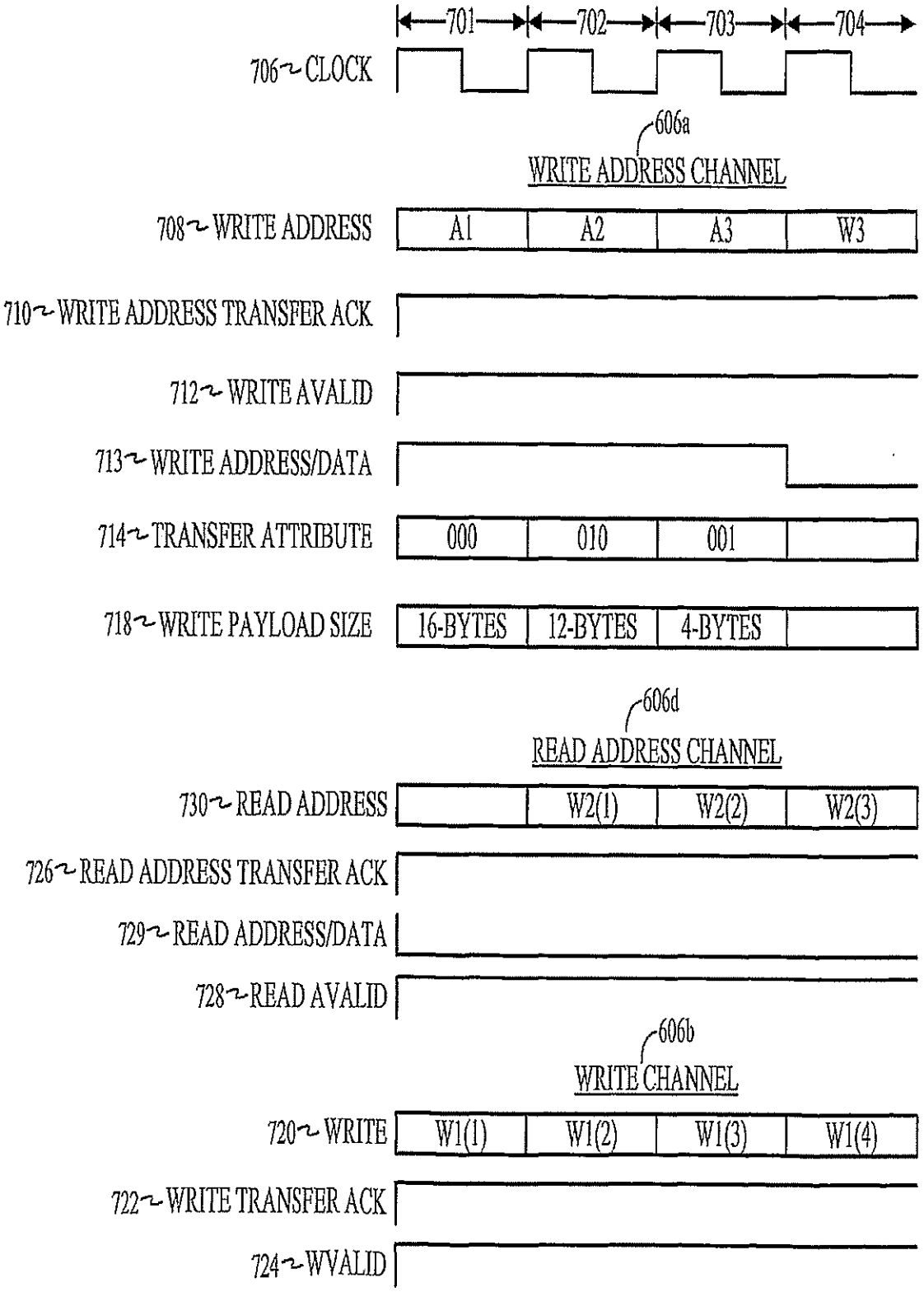

701
702
703
704
706 CLOCK
606a
WRITE ADDRESS CHANNEL
708 WRITE ADDRESS
A1
A2
A3
W3
710 WRITE ADDRESS TRANSFER ACK
712 WRITE AVALID
713 WRITE ADDRESS/DATA
714 TRANSFER ATTRIBUTE
000
010
001
718 WRITE PAYLOAD SIZE
16-BYTES
12-BYTES
4-BYTES
606d
READ ADDRESS CHANNEL
730 READ ADDRESS
W2(1)
W2(2)
W2(3)
726 READ ADDRESS TRANSFER ACK
729 READ ADDRESS/DATA
728 READ AVALID
606b
WRITE CHANNEL
720 WRITE
W1(1)
W1(2)
W1(3)
W1(4)
722 WRITE TRANSFER ACK
724 WVALID

FIG. 7

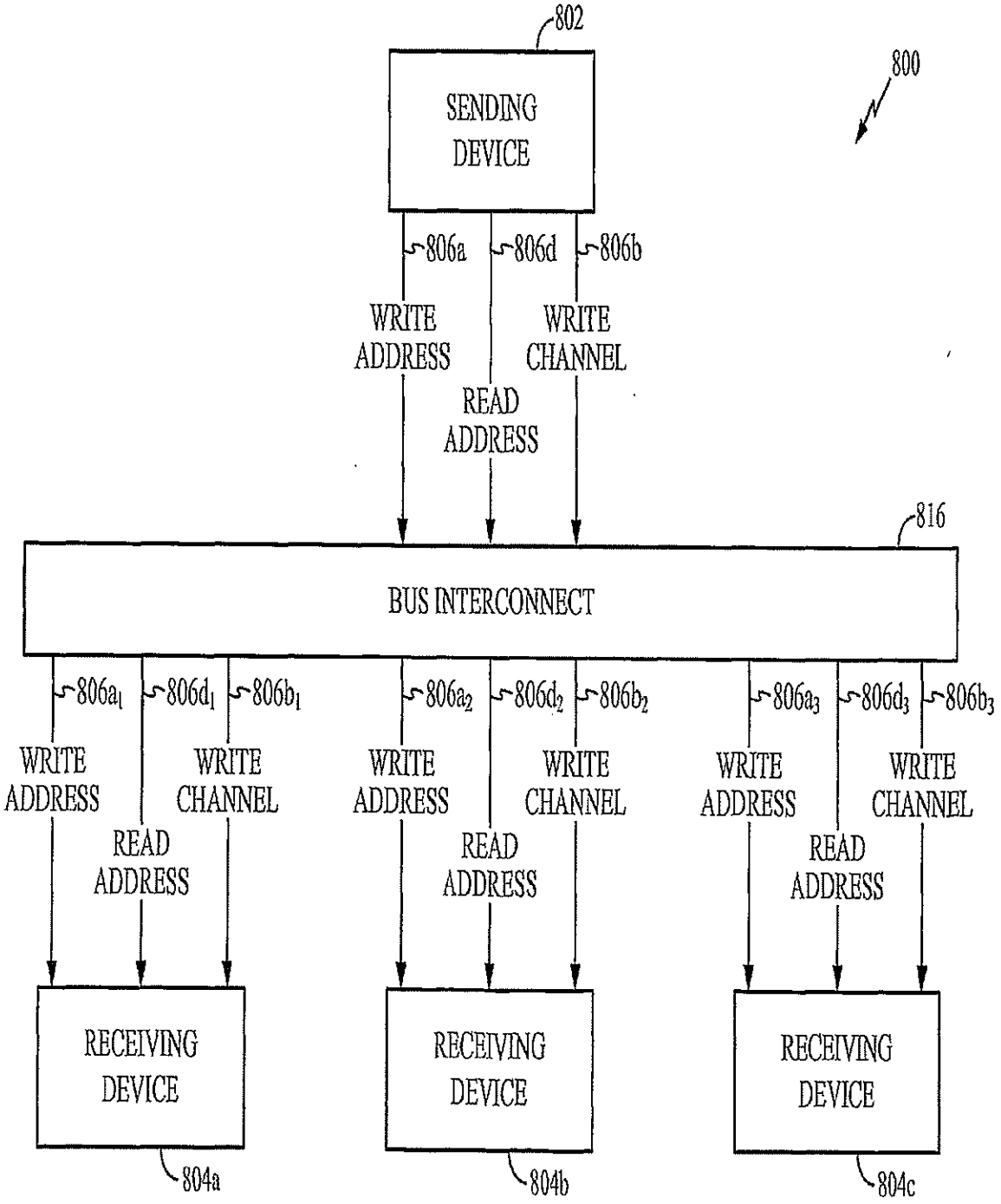

802
800
SENDING DEVICE
806a
806d
806b
WRITE ADDRESS
READ ADDRESS
WRITE CHANNEL
816
BUS INTERCONNECT
806a1
806d1
806b1
806a2
806d2
806b2
806a3
806d3
806b3
WRITE ADDRESS
READ ADDRESS
WRITE CHANNEL
RECEIVING DEVICE
804a
804b
804c

FIG. 8

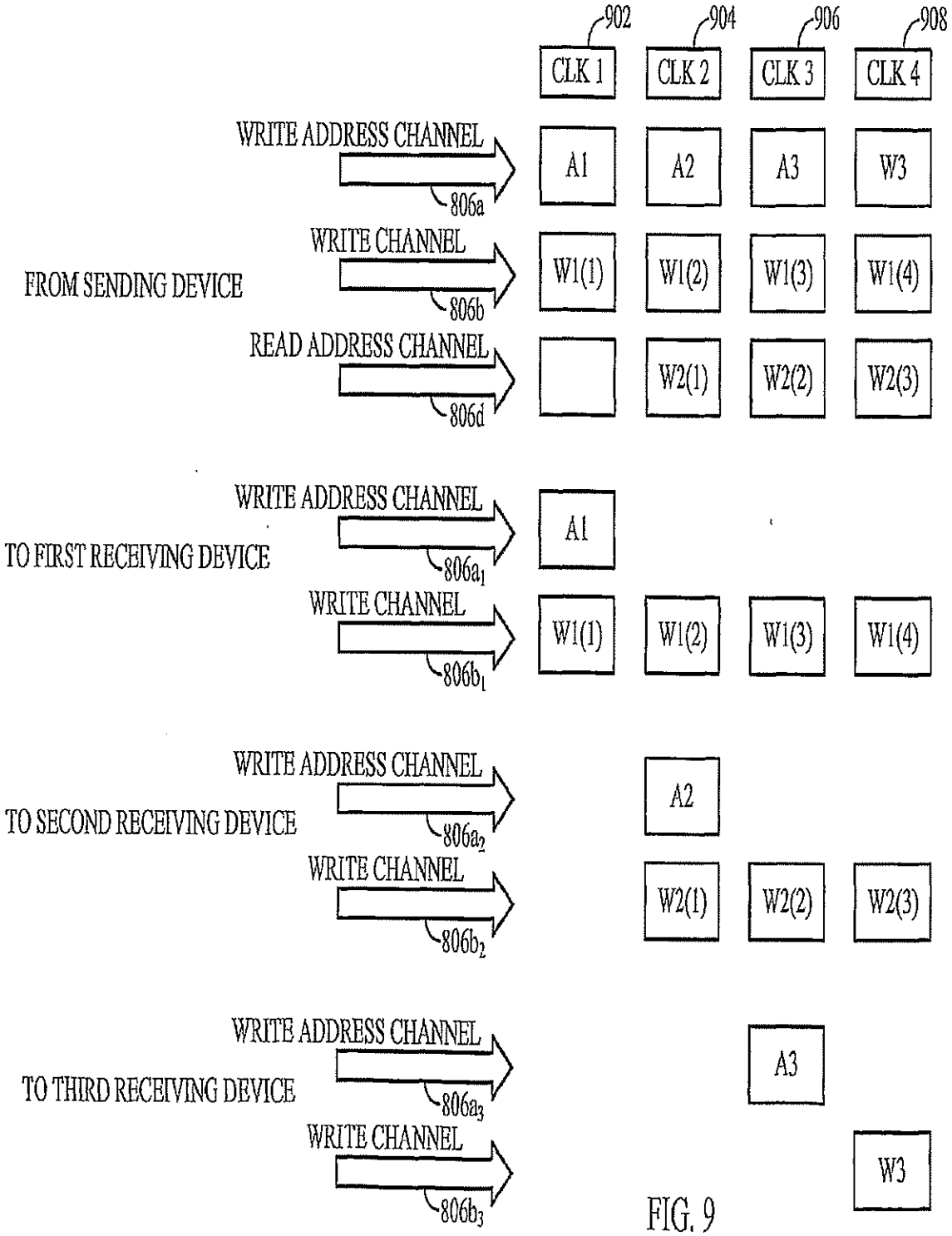

902
904
906
908
CLK 1
CLK 2
CLK 3
CLK 4
WRITE ADDRESS CHANNEL
806a
A1
A2
A3
W3
WRITE CHANNEL
FROM SENDING DEVICE
806b
W1(1)
W1(2)
W1(3)
W1(4)
READ ADDRESS CHANNEL
806d
W2(1)
W2(2)
W2(3)
WRITE ADDRESS CHANNEL
TO FIRST RECEIVING DEVICE
806a1
A1
WRITE CHANNEL
806b1
W1(1)
W1(2)
W1(3)
W1(4)
WRITE ADDRESS CHANNEL
TO SECOND RECEIVING DEVICE
806a2
A2
WRITE CHANNEL
806b2
W2(1)
W2(2)
W2(3)
WRITE ADDRESS CHANNEL
TO THIRD RECEIVING DEVICE
806a3
A3
WRITE CHANNEL
806b3
W3

FIG. 9