

CLAIMS

What is claimed is:

- 1 1. A method, comprising:
2 applying a first voltage to a ferroelectric memory cell of a memory array
3 during each cycle of a plurality of access cycles;
4 determining that the ferroelectric memory cell has reached a fatigue threshold
5 based at least in part on applying the first voltage for the plurality of access cycles; and
6 applying a second voltage to the ferroelectric memory cell based at least in
7 part on determining that the ferroelectric memory cell has reached the fatigue threshold,
8 wherein an amplitude of the second voltage is greater than an amplitude of the first voltage,
9 and wherein the second voltage is applied for a time period or a number of repetitions that is
10 based at least in part on the fatigue threshold of the ferroelectric memory cell.
- 1 2. The method of claim 1, further comprising:
2 determining a logic state of the ferroelectric memory cell based at least in part
3 on determining that the ferroelectric memory cell has reached the fatigue threshold; and
4 storing the logic state of the ferroelectric memory cell in another memory cell,
5 wherein the second voltage is applied to the ferroelectric memory cell after storing the logic
6 state of the ferroelectric memory cell in the other memory cell.
- 1 3. The method of claim 2, further comprising:
2 determining a logic state of the other memory cell after applying the second
3 voltage; and
4 writing the logic state of the other memory cell to the ferroelectric memory
5 cell.
- 1 4. The method of claim 1, wherein determining that the ferroelectric
2 memory cell has reached the fatigue threshold comprises:
3 detecting at least one of:
4 a timer exceeding a threshold time period, wherein the threshold time
5 period is based at least in part on a time to reach the fatigue threshold;

6 a counter exceeding a threshold number of counts, wherein the counter
7 is incremented for each access cycle of the plurality of access cycles;
8 a failure to sense the ferroelectric memory cell based at least in part on
9 applying a test access voltage with an amplitude less than the amplitude of the first
10 voltage;
11 a failure to sense the ferroelectric memory cell based at least in part on
12 a test sense window that is less than a sense window used for each cycle of the
13 plurality of access cycles, wherein the test sense window is based at least in part on a
14 reference voltage; or
15 an error correction code detecting a corrupted logic value of the
16 ferroelectric memory cell.

1 5. The method of claim 1, wherein determining that the ferroelectric
2 memory cell has reached the fatigue threshold comprises:
3 receiving a command to perform a fatigue recovery operation.

1 6. The method of claim 1, wherein the memory array comprises an
2 element of a device, and wherein applying the second voltage to the ferroelectric memory cell
3 comprises:
4 applying the second voltage to the ferroelectric memory cell during an event
5 that comprises at least one of:
6 the device powering on;
7 the device powering off; or
8 the device being connected to an external power supply.

1 7. The method of claim 1, wherein applying the second voltage for the
2 time period or the number of repetitions comprises:
3 applying the second voltage during a plurality of instances of an event,
4 wherein a subset of the time period or a subset of the number of repetitions is associated with
5 each instance of the event.

1 8. The method of claim 1, further comprising:

2 suspending the application of the second voltage based at least in part on
3 receiving a request to access the memory array; and
4 resuming the application of the second voltage based at least in part on
5 completing the request.

1 9. The method of claim 1, further comprising:
2 incrementing a counter each time the second voltage is applied.

1 10. The method of claim 1, further comprising:
2 applying the second voltage during a refresh operation that restores a logic
3 state to the ferroelectric memory cell, wherein the logic state is determined based at least in
4 part on applying the first voltage.

1 11. The method of claim 1, wherein the memory array comprises a
2 plurality of rows, wherein each row of the plurality of rows comprises a plate line in
3 electronic communication with a plurality of ferroelectric memory cells, and wherein
4 applying the second voltage comprises:
5 applying the second voltage to at least one plate line, wherein the second
6 voltage is applied to each ferroelectric memory cell that is in electronic communication with
7 the plate line based at least in part on applying the second voltage to the at least one plate
8 line.

1 12. The method of claim 11, wherein applying the second voltage to the
2 plate line comprises:
3 applying the second voltage to a plurality of plate lines.

1 13. The method of claim 1, wherein the fatigue threshold of the
2 ferroelectric memory cell is based at least in part on a relationship between a charge stored in
3 the ferroelectric memory cell and a capacitance of a digit line in electronic communication
4 with the ferroelectric memory cell and a sense component.

1 14. The method of claim 13, wherein the fatigue threshold of the
2 ferroelectric memory cell is based at least in part on a total number of access cycles in which
3 the ferroelectric memory cell reaches a remnant polarization threshold.

- 1 15. The method of claim 1, further comprising:
2 determining that a charge stored in the ferroelectric memory cell after
3 applying the second voltage is greater than a charge stored in the ferroelectric memory cell
4 before applying the second voltage, wherein the determination is based at least in part on a
5 sense voltage produced by the ferroelectric memory cell.
- 1 16. The method of claim 1, wherein the time period or the number of
2 repetitions of the second voltage is based at least in part on the amplitude of the second
3 voltage.
- 1 17. The method of claim 1, wherein applying the first voltage to access the
2 ferroelectric memory cell comprises:
3 reading the ferroelectric memory cell or writing the ferroelectric memory cell.
- 1 18. The method of claim 1, wherein the second voltage comprises at least
2 one of:
3 a plurality of bipolar voltage pulses;
4 a plurality of unipolar voltage pulses; or
5 a voltage with a constant amplitude.
- 1 19. A memory device, comprising:
2 a memory array comprising a plurality of ferroelectric memory cells; and
3 a counter that is resettable based at least in part on a fatigue recovery operation
4 performed on at least one ferroelectric memory cell of the plurality of ferroelectric memory
5 cells.
- 1 20. The memory device of claim 19, wherein the memory array comprises
2 a plurality of memory blocks that comprise a subset of the memory array, and wherein each
3 memory block of the plurality is associated with at least one counter.
- 1 21. The memory device of claim 19, further comprising:
2 a controller configured to perform the fatigue recovery operation, wherein the
3 fatigue recovery operation comprises:

4 a determination that the at least one ferroelectric memory cell has
5 reached a fatigue threshold based at least in part on applying a first voltage to the at
6 least one ferroelectric memory cell for a plurality of access cycles; and

7 a second voltage applied to the at least one ferroelectric memory cell
8 based at least in part on the determination that the at least one ferroelectric memory
9 cell has reached the fatigue threshold, wherein an amplitude of the second voltage is
10 greater than an amplitude of the first voltage, and wherein the second voltage is
11 applied for a time period or a number of repetitions that is based at least in part on the
12 fatigue threshold of the at least one ferroelectric memory cell.

1 22. The memory device of claim 19, further comprising:

2 a controller configured to:

3 perform the fatigue recovery operation on a first ferroelectric memory
4 cell of the plurality of ferroelectric memory cells; and

5 perform an access operation on a second ferroelectric memory cell of
6 the plurality during the fatigue recovery operation of the first ferroelectric memory
7 cell.

1 23. An electronic circuit, comprising:

2 a memory array comprising a plurality of ferroelectric memory cells;

3 a plurality of conductive terminals in electronic communication with the
4 memory array; and

5 a recovery terminal that supports a fatigue recovery operation of the plurality
6 of ferroelectric memory cells, wherein the plurality of conductive terminals comprises the
7 recovery terminal, and wherein the fatigue recovery operation comprises:

8 a recovery voltage applied to at least one ferroelectric memory cell of
9 the plurality based at least in part on a determination that the at least one ferroelectric
10 memory cell has reached a fatigue threshold, wherein an amplitude of the recovery
11 voltage is greater than an amplitude of an access voltage, and wherein the recovery
12 voltage is applied for a time period or a number of repetitions that is based at least in
13 part on the fatigue threshold.

1 24. The electronic circuit of claim 23, wherein the plurality of conductive
2 terminals comprise:

3 a first power terminal in electronic communication with a first voltage supply
4 that comprises the access voltage and is applicable to a ferroelectric memory cell of the
5 memory array during an access operation of the ferroelectric memory cell; and

6 a second power terminal in electronic communication with a second voltage
7 supply that comprises the recovery voltage and is applicable to the ferroelectric memory cell
8 of the memory array during the fatigue recovery operation of the ferroelectric memory cell.

1 25. The electronic circuit of claim 23, wherein the fatigue recovery
2 operation comprises:

3 a signal to initiate the fatigue recovery operation of the plurality of
4 ferroelectric memory cells via the recovery terminal.

1 26. The electronic circuit of claim 23, wherein the fatigue recovery
2 operation comprises parameters that are programmable by a user.

1 27. An electronic memory apparatus, comprising:

2 means for applying a first voltage to a ferroelectric memory cell of a memory
3 array during each cycle of a plurality of access cycles;

4 means for determining that the ferroelectric memory cell has reached a fatigue
5 threshold based at least in part on applying the first voltage for the plurality of access cycles;
6 and

7 means for applying a second voltage to the ferroelectric memory cell based at
8 least in part on determining that the ferroelectric memory cell has reached the fatigue
9 threshold, wherein an amplitude of the second voltage is greater than an amplitude of the first
10 voltage, and wherein the second voltage is applied for a time period or a number of
11 repetitions that is based at least in part on the fatigue threshold of the ferroelectric memory
12 cell.

1 28. The electronic memory apparatus of claim 27, further comprising:

2 means for determining a logic state of the ferroelectric memory cell based at
3 least in part on determining that the ferroelectric memory cell has reached the fatigue
4 threshold; and
5 means for storing the logic state of the ferroelectric memory cell in another
6 memory cell, wherein the second voltage is applied to the ferroelectric memory cell after
7 storing the logic state of the ferroelectric memory cell in the other memory cell.

1 29. The electronic memory apparatus of claim 28, further comprising:
2 means for determining a logic state of the other memory cell after applying the
3 second voltage; and
4 means for writing the logic state of the other memory cell to the ferroelectric
5 memory cell.

1 30. The electronic memory apparatus of claim 27, wherein means for
2 determining that the ferroelectric memory cell has reached the fatigue threshold comprises:
3 means for detecting at least one of:
4 a timer exceeding a threshold time period, wherein the threshold time
5 period is based at least in part on a time to reach the fatigue threshold;
6 a counter exceeding a threshold number of counts, wherein the counter
7 is incremented for each access cycle of the plurality of access cycles;
8 a failure to sense the ferroelectric memory cell based at least in part on
9 applying a test access voltage with an amplitude less than the amplitude of the first
10 voltage;
11 a failure to sense the ferroelectric memory cell based at least in part on
12 a test sense window that is less than a sense window used for each cycle of the
13 plurality of access cycles, wherein the test sense window is based at least in part on a
14 reference voltage; or
15 an error correction code detecting a corrupted logic value of the ferroelectric
16 memory cell.

1 31. The electronic memory apparatus of claim 27, wherein means for
2 applying the second voltage for the time period or the number of repetitions comprises:
3 means for applying the second voltage during a plurality of instances of an
4 event, wherein a subset of the time period or a subset of the number of repetitions is
5 associated with each instance of the event.

1 32. The electronic memory apparatus of claim 27, further comprising:
2 means for suspending the application of the second voltage based at least in
3 part on receiving a request to access the memory array; and
4 means for resuming the application of the second voltage based at least in part
5 on completing the request.

1 33. The electronic memory apparatus of claim 27, further comprising:
2 means for incrementing a counter each time the second voltage is applied.

1 34. The electronic memory apparatus of claim 27, further comprising:
2 means for applying the second voltage during a refresh operation that restores
3 a logic state to the ferroelectric memory cell, wherein the logic state is determined based at
4 least in part on applying the first voltage.

1 35. The electronic memory apparatus of claim 27, further comprising:
2 means for determining that a charge stored in the ferroelectric memory cell
3 after applying the second voltage is greater than a charge stored in the ferroelectric memory
4 cell before applying the second voltage, wherein the determination is based at least in part on
5 a sense voltage produced by the ferroelectric memory cell.