An object of the present invention is a light detection circuit which can be used to detect exposure to light. The circuit may preferably be used in the field of integrated electronic circuits where, if it is integrated on the same substrate as an integrated circuit to be protected, it may detect illumination to which the circuit might be subjected.

Some integrated electronic circuits are of a confidential kind, either because the data which they store should remain secret or because their method of operation should remain hidden. The latter is the case in general when it is desired to prevent fraudulent use or, in particular, in the field of memory cards to prevent reconstruction of secret algorithms. In practice, one must realise that it is possible to discover and understand by deduction the operation of an integrated circuit when the passivation layer which covers the said circuit at the end of its manufacture has been removed. In order to do this, after depassivation, functions of the circuit are selected while observing with an electron microscope the passage of current through connections in the circuit. The passage of current causes localized mechanical stresses in the semiconductive parts. It is possible to deduce from them information relating to the functioning of the integrated circuit.

In the field of memory cards the integrated circuits employed are generally of the non-volatile type, the memory locations of which comprise floating gate transistors. Some of them are programmable and erasable by subjecting the chip to ultraviolet radiation. This radiation is located outside the visible band of the spectrum. At the end of manufacture of these circuits the chips are covered with a transparent passivation layer which makes it possible, after a preliminary test of the correct functioning of the integrated circuit, to erase test data stored in it and to restore the memory to a blank condition for use as desired by the purchaser. After this test operation is completed, the integrated circuits thus passivated are embedded in opaque carrier supports. In the field of memory cards, in particular those of the bank card type, this opaque support may be formed of the plastic material of

the card itself. The problem to be overcome is that of preventing a fraudster from being able to remove the semiconductor chip from a card, after it has been programmed by the user, in order to examine it with an electron microscope and to attempt to deduce how it functions or at least to neutralise its access codes.

Some integrated circuits, in particular those including electrically erasable memories or memories designed to be programmed only once, have opaque passivation layers. In the case of these circuits, through the measurement of illumination, it is essentially the operation of depassivation which it is desired to control.

An aim of the invention is to detect, and if necessary to counter, the exposure of such circuits to light. For this purpose, use is made of the fact that reverse polarised junctions of diodes or of transistor drain-channel regions react differently to light. In fact light increases the leakage current of reverse polarised junctions by a factor of about 1000. The invention is therefore based on accentuating this principle as much as possible. In this manner a detector sensitive to direct or ambient light is obtained.

An object of the invention is, therefore, an integrated electronic circuit for protection against exposure to light as defined in claim 1.

The invention will be better understood on reading the following description and examining the Figures which accompany it. These are given solely by way of non-limiting illustration of the invention. The Figures show :

- Figure 1 : a light detection circuit in accordance with the invention,
- Figure 2 : a voltage-current diagram showing the change in the characteristic of a junction subjected to illumination,
- Figure 3 : a schematic representation of a simple example of a detector in accordance with the invention, integrated on a substrate of an integrated electronic circuit to be protected.

Figure 1 shows a light detection circuit in accordance with the invention. This circuit substantially comprises a junction in a diode 1 which is reverse polarised by a current generator 2. In a preferred example the current generator comprises a transistor 2 maintained at the conduction limit by a control voltage applied to its gate 3 by a control circuit 17. So as to ensure the correct polarisation of the transistor 2 the latter is connected in series between a supply Vcc and a blocked transistor 4. In the example shown, the transistor 2 is a P channel transistor and the transistor 4 is an N channel transistor. The transistor 4 is blocked by the connection of its gate 5 to the same ground potential as its drain 6. The operation of the detector is as follows. When the junction 1 is not subjected to illumination, its characteristic voltage-current curve V-I is the curve 7 in Figure 2. the third quadrant of the characteristic curve of this junction is used because the junction is reverse polarised. The transistor 2, brought to its conduction limit, can supply only a current Im. This current Im is however greater than a reverse saturation current Is in the junction 1. Under these conditions said junction is subjected to a potential difference DV substantially equal to the supply voltage Vcc less the drain-source voltage drop in the transistor 2.

When the junction 1 is exposed to light (shown by the arrows L) the characteristic curve 7 is displaced to 8 (shown by the arrows D). This means that the reverse saturation current becomes much greater. In practice it even becomes about 1000 times greater although the drawing does not show this. Under these conditions the transistor 2 which, because it is at its conduction limit, is only able to supply a current of limited size Im causes a different drop in voltage CV at the terminals of the junction 1. In practice, from one state of illumination to the other, the current Im is not quite constant. Nevertheless, in view of the very large change in the saturation current of the junction this approximation is justified. Consequently the potential at a midpoint 9 between the transistors 2 and 4, to which the junction 1 is connected, decreases as a result of the illumination by (DV-CV). This drop in potential is used in a shaping and processing circuit 10 as a light detection signal.

In an example, the circuit 17 for polarizing the current generator comprising the transistor 2 includes two transistors in series and in a conductive state. The first transistor 11 is for example a P channel transistor with its source connected to the supply voltage Vcc and its drain connected to the gate 3 of the transistor 2. The gate 12 of the P channel transistor 11 is also connected to the gate 3. The second transistor 13 is an N channel transistor with its drain connected to the gate 3 and its source connected to ground. The gate 14 of the transistor 13 is connected to the supply voltage Vcc. Taking into account the polarities of these transistors, this connection arrangement makes both of them conductive. They form a voltage divider by means of their electrical resistances connected in series.

In a preferred embodiment, a semiconductor substrate used to produce an integrated circuit is a P type semiconductor substrate. The P channel transistor 11 must then be formed in an N- doped well 15. To eliminate an effect called a substrate effect, the well 15 of the transistor 11 is connected by a contact 16 on the well to the source of the transistor 11. The voltage present on the gate 3 of the transistor 2 depends on the relative dimensions of the transistors 11 and 13. In practice the transistor 11 is much larger than the transistor 13 so that its electrical resistance is much smaller than the resistance of the transistor 13. Consequently the voltage on the gate 3 is substantially equal to Vcc - Vds. The value Vds represents the voltage drop in the transistor 2 when it is conductive. The transistor 2 is permanently conductive. However it behaves as a generator of substantially constant current. Thus, when the junction 1 is exposed to light, it is unable to supply sufficient current to inversely saturate this junction. The latter causes only a small drop in the potential CV.

When the junction 1 is exposed to light the transistor 4, which is an N channel transistor, forms an N+P- type diode between its drain region 18 and the substrate 19 of the integrated circuit semiconductor (Figure 3). This diode 18-19 is likewise reverse polarised. It therefore also undergoes a similar type of modification of its voltage-current characteristic when it is subjected to illumination. In practice only one

of these junctions, either the diode 1 or the junction 18-19 of the transistor 4, is used. In practice the junction showing the greatest displacement of its voltage-reverse current characteristic as a result of the illumination imposes the corresponding shift of the voltage available at the midpoint of the assembly. In other words, one of the two junctions is useless from this point of view. This dual embodiment has nevertheless made it possible to show, and it can be verified by calculation, that among the junctions which show a greater sensitivity to light, those having the lowest concentrations of impurities on either side of the junction are also the most effective. Thus an N+P- or N-P+ type of junction will be less effective than an N-P- type junction.

Figure 3 shows a schematic cross-section of the detector assembly in accordance with the invention. A well 20 having an N- impurity concentration is formed in a P- semiconductor substrate 19, which well contains the current generating transistor 2. The source 21 of the transistor 2 is connected to the supply voltage Vcc. The gate 3 of the transistor 2 is connected to the control circuit 17, and the drain 22 of the transistor 2 is connected on the one hand to the drain 18 of the transistor 4 and on the other hand to the cathode 23 of the diode 1. This diode 1 may be formed in practice in the same manner and at the same time as the well 20. It has a concentration of N- impurities in its cathode region, its anode being formed by the P- doped substrate itself. To improve the connection an N+ doped contact 24 for the well may even be formed if a subsequent process stage allows this. In the same manner the connection to ground of the substrate and of the source 6 of the transistor 4 may be obtained by forming a connection 25 for the substrate. Depending on whether the junction 1 or the junction 18-19 will have the preponderant effect, the other junction may be omitted.

The shaping circuit 10, Figure 1, includes in a preferred embodiment at least two inverters. Preferably it even comprises three of them so as to supply a signal of a given polarity and a complementary signal after the detection of illumination. The first inverter, which comprises a P channel transistor 26 in series with an N channel

transistor 27 between the supply voltage and ground, is preferably desymmetrized in order to supply a high level at its output 28 easily when it receives a low level at its input 29; that is to say when there is exposure to light (CV). The purpose of this dissymmetry is to reduce current consumption in the inverter in steady state conditions. Another aim of the dissymmetry is to increase the sensitivity to switching of the inverter when light is applied. In practice the voltage CV present at the terminals of the junction 1 is not strictly zero. Consequently, to prevent this non-zero voltage not switching over the inverter 26-27, this inverter is desymmetrized so that it is more sensitive. The second inverter, constructed on the same principle, comprises two transistors 30-31. It is connected in cascade with the inverter 26-27. It is a conventional inverter: it acts in short as a signal amplifier. This inverter supplies a signal S representative of the illumination. Preferably the inverter 30-31 is itself connected in cascade with a third inverter 32-33 for supplying a signal $\overline{S}$ complementary to the signal S. It is possible to employ one of these two signals to neutralize use of a semiconductor integrated circuit when it is desired to protect it against attack after removal from a card or after depassivation.

CLAIMS

1. An integrated electronic circuit for protecting against exposure to light resulting from a depassivation, comprising a light sensor consisting of a junction (1) which receives the light (L) to be detected, the junction being reverse polarised by a generator of constant current comprising a transistor (2) polarised to the conduction limit so as to supply to the junction a current of limited intensity (Im), slightly greater than the reverse saturation current of the junction when it does not receive light, in order to change the voltage at the terminals of the junction in dependence on the intensity of the light received and to supply a signal for neutralizing the integrated circuit.

2. An integrated circuit as claimed in claim 1, characterized in that the junction comprises a diode (1).

3. An integrated circuit as claimed in claim 1, characterized in that the junction is contained in a transistor (4).

4. An integrated circuit as claimed in any one of claims 1 to 3, characterized in that the junction is of the N-P- type.

5. An integrated circuit as claimed in claim 4, characterized in that the N-P- junction consists of an N- type well (20) in a P- semiconductor substrate.

6. An integrated circuit as claimed in any one of claims 1 to 5, characterized in that it comprises a signal shaping circuit (10) comprising at least two bistable inverters in series, a first asymmetric bistable inverter (26-29) for detecting, by switching, an exposure of the sensing circuit to light and a second inverter (30-31) for amplifying the switching signal supplied by the first inverter.